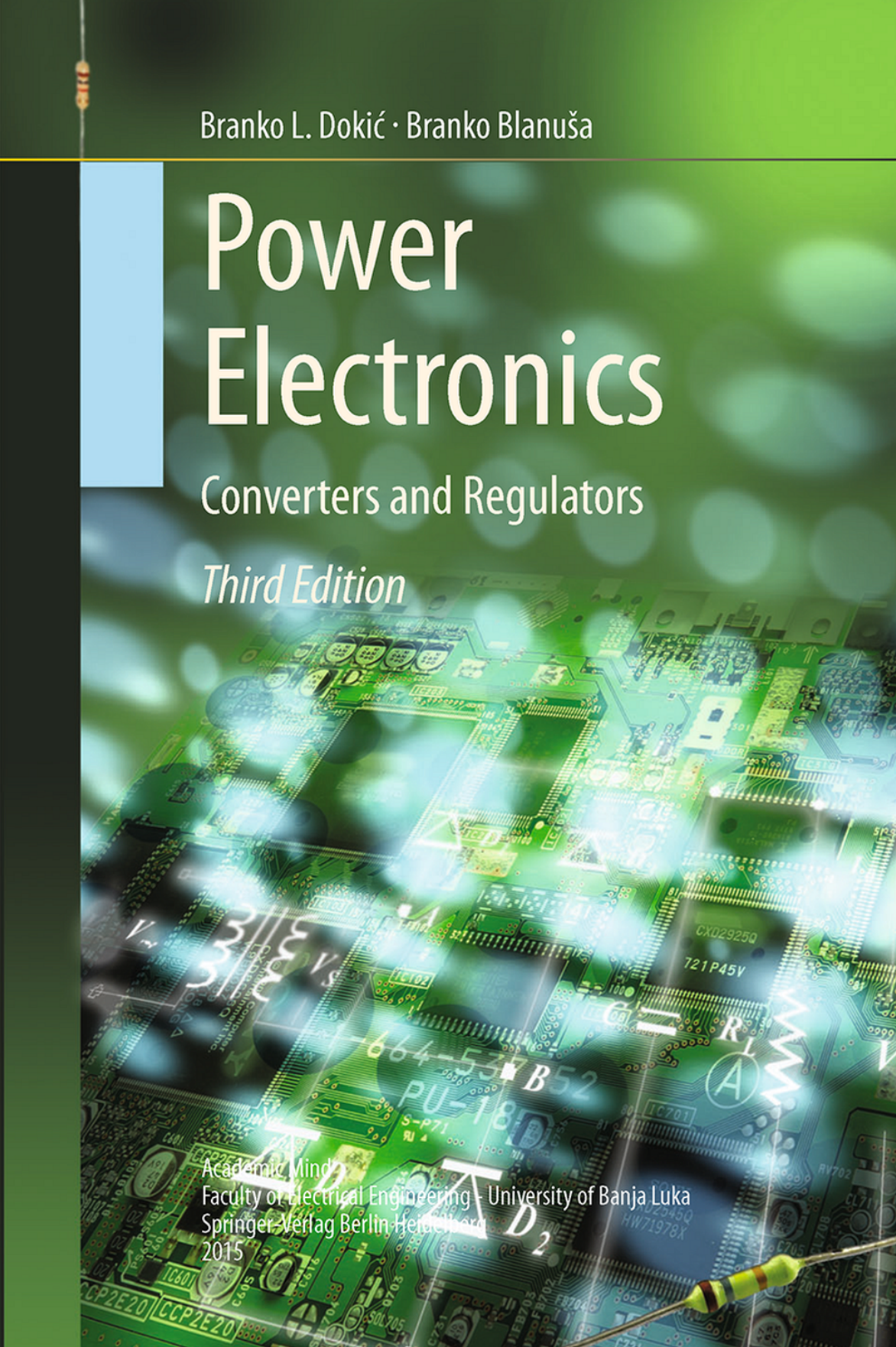




Branko L. Dokić · Branko Blanuša

Power Electronics

Converters and Regulators

Third Edition

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Branko L. Dokić · Branko Blanuša

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Converters and Regulators

Third Edition



 Springer

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Foreword

Review of the Book “Power Electronics” by Branko L. Dokić and Branko Blanuša

The book “Power Electronics” by Branko L. Dokić and Branko Blanuša contains ten chapters, and deals with the most significant items of power electronics. It is well organized with lot of examples, figures, and tables.

The first chapter is “Introduction.” In this chapter basic elements, as well as some circuits and components used in power electronics are briefly presented. Chapter 2 covers basic semiconductor components, “Diodes and Transistors,” and particularly covers their use as switches in power electronics circuits. Chapter 3 is focused on “Regenerative Switches.” The description is wide and detailed and this chapter may be of interest not only for students, but also for professionals who use these components in practice.

Chapter 4 is “PWM DC/DC Converters.” The converters are classified. All basic topologies of these converters are analyzed in detail in both continuous current mode (CCM) and discontinuous current mode (DCM).

“Control Modules” are presented in Chap. 5. This chapter contains a number of control circuits used in power electronics. This chapter may be of interest not only for professionals in the field of power electronics, but also in related fields such as automotive control, pulse electronics, etc.

Chapter 6 covers “DC/AC Converters–Inverters”. This chapter is comprehensive and covers the most important converter topologies and the most common used control techniques, such as selective harmonic elimination, unipolar and bipolar PWM technique, and space vector modulation.

The next chapter is AC/DC converters, i.e., rectifiers. This chapter contains all basic topologies from uncontrolled half bridge and full bridge rectifiers to controlled thyristor and transistor ones. Also, some commonly used control techniques are presented. PWM rectifiers and their applications are also discussed.

Two previous chapters are followed by the eighth chapter, which covers “AC/AC Converters.” The chapter describes single-phase and three-phase AC/AC

voltage converters and both direct and indirect frequency AC/AC converters. Also, an overview of matrix converters and their applications is presented in this chapter.

Chapter 9 contains a comprehensive description of “Resonant Converters.” Basic topologies are covered; series resonant converters, parallel resonant converters, series–parallel converters, class E resonant converters, zero voltage and zero current switching converters, and some control circuits used in resonant converters.

Finally, Chap. 10 covers multilevel converters. Basic topologies of DC/DC and DC/AC multilevel converters are presented. Also, some widely used control techniques, such as multilevel PWM, space vector modulation, space vector control, and selective harmonic elimination, are briefly discussed in this chapter.

Every chapter contains a set of solved problems that facilitate understanding of the related field. Also, every chapter is concluded with a list of problems from the presented topics.

Overall, the impression is that the book presents a comprehensive coverage of power electronics. It covers a wide range of topics relevant to power electronics. So, it might be used both as a textbook for students and as a reference book for practicing engineers.

In my opinion, there is a significant academic and theoretical contribution made by this book.

Therefore, I am glad to recommend the book “Power Electronics” by Branko L. Dokić and Branko Blanuša to be published.



November 2013
Novi Sad

Vladimir Katić
Faculty of Technical Sciences
University of Novi Sad
Novi Sad
Serbia

Review of the Book “Power Electronics,” Authored by Branko L. Dokić and Branko Blanuša

The book “Power Electronics” by Branko L. Dokić and Branko Blanuša is structured into ten chapters, and covers wide area of power electronics.

The first chapter is “Introduction”, and briefly reviews parts of signals and systems theory as used in power electronics, as well as some circuit theory and basic components used in power electronics. Chapter 2 covers “Diodes and Transistors,” with emphasis on their application in power electronics. This chapter presents a wide and detailed coverage of the topic, which might be of interest in areas other than power electronics. Chapter 3 is still focused on components, “Regenerative Switches.” The coverage is detailed again, and might be used as a reference in the area.

Coverage of topics specific to power electronics starts with Chap. 4, “PWM DC/DC Converters.” The converters are classified, and their steady-state operation is analyzed in detail and includes a discussion of loss mechanisms.

Chapter 5, “Control Modules,” is again a chapter that might be a reference both in power electronics and in related fields. The chapter describes a number of circuits used to control power electronic systems, and illustrates their application. The presentation is general enough to be used even outside power electronics.

Chapter 6 covers “DC/AC Converters–Inverters”, i.e., inverters. The coverage is comprehensive, covers both inverter topologies and their control, including space vector modulation. The chapter is followed by its natural complement, AC/DC converters, i.e., rectifiers. Again, the coverage is complete, starting from uncontrolled rectifiers, progressing toward phase controlled rectifiers and high power factor PWM rectifiers. Besides, bidirectional converters based on inverters are covered. Operation of rectifiers is illustrated by numerous simulation output diagrams.

The previous two chapters are naturally followed by a chapter that covers “AC/AC Converters,” i.e., cycloconverters. The chapter covers both naturally commutated converters and converters with forced switching, and discusses a problem of bidirectional switch realization and commutation of unidirectional switches in an assembly that results in a bidirectional switch.

Chapter 9 covers “Resonant Converters”. Many topologies are covered: series resonant converter, parallel resonant converter, class E resonant converters, zero voltage switching, and zero current switching. The coverage is comprehensive.

Finally, Chap. 10 presents multilevel converters, and besides being labeled as “introduction” the presentation covers the most important topics: converter structures, operation, and control topics including selective harmonic elimination.

Overall, the impression is that the book presents a complete view and comprehensive coverage of power electronics, and that it might be used both as a textbook for students and as a reference book for practicing engineers. It is worth to mention that the chapters are accompanied by a list of problems that address presented topics.

Based on the facts listed above, I can recommend the book “Power Electronics” by Branko L. Dokić and Branko Blanuša, to be published.



August 2013
Belgrade

Predrag Pejović

Preface

Nowadays, “Power Electronics,” basically deals with conversion and control of electrical power using electronic converters based on semiconductor power switches. Historically, the evolution of power electronics has generally followed the semiconductor power device evolution. Power solid-state devices are the heart and soul of modern power electronics equipment. Therefore, the age of power solid-state electronics is often called the second electronics revolution. Development of microelectronic controllers has made revolutionary advances in power electronics.

Power electronics circuits are an integral part of all electronics equipments. Power supply is the heart of all electronic circuits. For low-power consumption units or for portable operation, a battery is often used. For example, in a power supply system for a laptop computer, DC/DC converter converts lithium battery voltage into the output voltages required by the load. AC mains supply is generally used as a primary power supply for high power circuits. In almost all cases, this power requires conversion to the appropriate DC voltage by AC to DC converters. Besides DC to DC and AC to DC converters, typical applications of power electronics include conversion of an unregulated DC voltage to a regulated one, conversion of DC to AC, and conversion of an AC power source from one amplitude and/or frequency to another amplitude and/or frequency.

DC to DC converters and DC to AC inverters provide natural interfaces with direct energy sources such as solar cells, thermoelectric generators, fuel cell uninterruptible power sources. Commercial applications of power electronics include industrial motor drives, electrical vehicle power and drive system, as communications equipment, off-line power systems for computers, robotic technology, inverter systems for renewable energy generation applications, etc. In the twenty-first century, power electronics will have a large impact on industrial automation, energy conservation, utility systems, transportation, and environmental protection.

Power electronics includes application from ranges less than one watt (battery-operated portable equipment) to more than a few 100 or 1,000 W in motor drives or in rectifiers and inverters that interface DC transmission lines to the AC utility power system. In view of the fact that high efficiency is essential in all power processing applications, the key element is the switching converter. A small power

loss and hence high energy efficiency cannot be met by linear electronics where the semiconductor devices are operated in their active (linear) region. That is the reason that switched mode of semiconductor devices (transistors or thyristors) are used in switching converters. When a switch operates in the off state, its current is close to zero, and when it operates in the on state, its voltage drop is very small. In either state, its power dissipation is low. If the switching device is ideal, either the device voltage in on state or the device current in off state is zero so that power dissipation is also zero. Efficiency depends on switching frequency because real devices absorb some power when transition between on and off states and vice versa. Efficiency is improved by use of new switching devices, new circuit topologies, modern control techniques, and new ways of manufacture.

The book “Power Electronics: Converters and Regulators” is structured into ten chapters.

Chapter 1 is “Introduction,” and briefly reviews parts of signals and systems theory as used in power electronics, as well as some circuit theory and basic components used in power electronics.

Chapter 2 covers “Diodes and Transistors,” and particularly covers their use as switches in power electronics circuits. Power MOS transistors, IGBT and some standard driver and snubber circuits are also described in this chapter.

Chapter 3 is still focused on devices, “Regenerative Switches.” The most important regenerative switches are covered including new powerful devices such as the Emitter Turn-Off Thyristor (ETO) and Insulated Gate Bipolar Thyristor (IGCT).

Coverage of topics specific to power electronics starts with Chap. 4, “PWM DC/DC Converters.” All basic topologies are analyzed in both Continuous (CCM) and Discontinuous Current Mode (DCM). This chapter also includes discussion of loss mechanisms in these converters.

“Control Modules” are presented in Chap. 5. Basic principles and characteristics of PWM control modules are covered. The chapter describes a number of circuits used to control power electronic systems, and illustrates their application.

Chapter 6 covers “DC/AC Converters,” i.e., inverters. One-phase and three-phase bridge inverters are presented. Also, the most used control techniques are discussed, unipolar and bipolar PWM and space vector modulation.

Chapter 7 is followed by its natural complement, AC/DC Converters, i.e., rectifiers. The coverage starts from uncontrolled rectifiers, progressing toward phase controlled rectifiers and high power factor PWM rectifiers. The most commonly used control techniques are presented, as well as some application with the PWM rectifiers.

Chapter 8 covers “AC/AC Converters.” This chapter describes single-phase and three-phase AC/AC voltage converters and both direct and indirect frequency converters. Also, an overview of matrix converters and their applications is presented in this chapter.

Chapter 9 contains description of “Resonant Converters.” Many topologies are covered: series resonant converter, parallel resonant converter, class E resonant

converters, zero voltage and zero current switching converters, and some control circuits used in resonant converters.

Chapter 10 covers “Multilevel Converters.” Basic topologies of DC/DC and DC/AC multilevel converters are presented. Also, some widely used control techniques, such as multilevel PWM, space vector modulation and selective harmonic elimination, are briefly discussed in this chapter.

The book “Power Electronics: Converters and Regulators” is primarily intended for students of electrical engineering. A significant part of the book was created from authors’ teaching materials for the subjects *Pulse Electronics* and *Power Electronics* at the Faculty of Electrical Engineering, University of Banja Luka in the last 15 years. This is third revised and updated edition. In relation to the two previous issues from 2000 and 2007, which were intended for Serbian and Croatian language readers (ex-Yugoslavia countries), this issue has have more than one third of the content altered. The alterations are in the form of: completely or partially new chapters, such as Multilevel Converters, Space Vector Modulation, Active Rectifier, PWM Rectifiers, Matrix Converters, Power Factor Correction, and number of problems at the end of every chapter.

For the design of power electronic converters, different knowledge from electrical engineering fields is required, such as theory of electrical circuits, electronics, electromagnetics, theory of control systems, and heat transfer. In addition, semiconductor elements in switched mode are highly nonlinear, and analysis of the circuits is quite complex. Therefore, simplified models are used in this book with explanation of the basic processes and essential phenomena. This is followed by waveforms of characteristic voltages and currents, which should complete understanding of electrical circuits operation. Numerous solved examples in each chapter should help students better understand the book material. Besides, we used examples to introduce ways of thinking about the problems, methods of analysis, and use of approximations. For some problems the results obtained by PSPICE simulation are presented. At the end of each chapter, unsolved problems are given, which should help the students to test their knowledge and stimulate thinking about the material presented in the chapter.

The authors thank their colleagues Prof. Predrag Pejović from the Faculty of Electrical Engineering in Belgrade and Prof. Vladimir Katić from the Faculty of Technical Sciences in Novi Sad, whose suggestions significantly contributed to the content of this book. Also, we thank Dr. Vojislav Arandelović from the Institute of Nuclear Physics Vinča—Belgrade and Dr. Zoran Jakšić from the Institute of Physics—Belgrade, who with content and linguistic corrections improved the intelligibility of the text as a whole.

Branko L. Dokić
Branko Blanuša

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Chapter 1

Introduction

Power electronics in a broader sense implies the part of electronics that is used in electric power. This is the equipment utilized in systems for control and regulation of electric power supplies and in systems for the regulation of electric drives. Power electronics includes various types of electric power converters, such as converters of AC to DC current, DC to AC, DC to DC, converters of different types of energy (thermal, nuclear, and light) into electric energy, etc. Since most of the equipment based on power electronics contains converters of some type, very often the concept of power electronics is understood as converter electronics.

In essence, a power electronics apparatus consists of a power part and a control part. The power component, serving for the transfer of energy from the source to the load, consists of power electronic switches, electric chokes, transformers, capacitors, fuses, and sometimes resistors. A combination of these elements is used to make different converter circuits adjusted to the mode of the primary supply and the character of the load. Energy losses within a converter should be as small as possible. Consequently, the semiconductor elements of the converter are mainly operated in the pulse (switching) mode. They may be either controllable (transistors, thyristors) or noncontrollable (diodes). The control or information block controls the regulating (mostly switching) elements of the converter. The control, or regulation, is accomplished on the basis of the information the control block has collected from the power part of the apparatus. Mostly the information concerns the output voltage, load current or current/voltage of a critical element of the converter (e.g. transistor). The control block can functionally be a very complex electronic assembly consisting of either analogue or digital elementary assemblies.

1.1 Types of Signals

There are various types of signals (voltage/current) used in the transferring of energy from the primary source to the load and in the control of this transfer (Fig. 1.1).

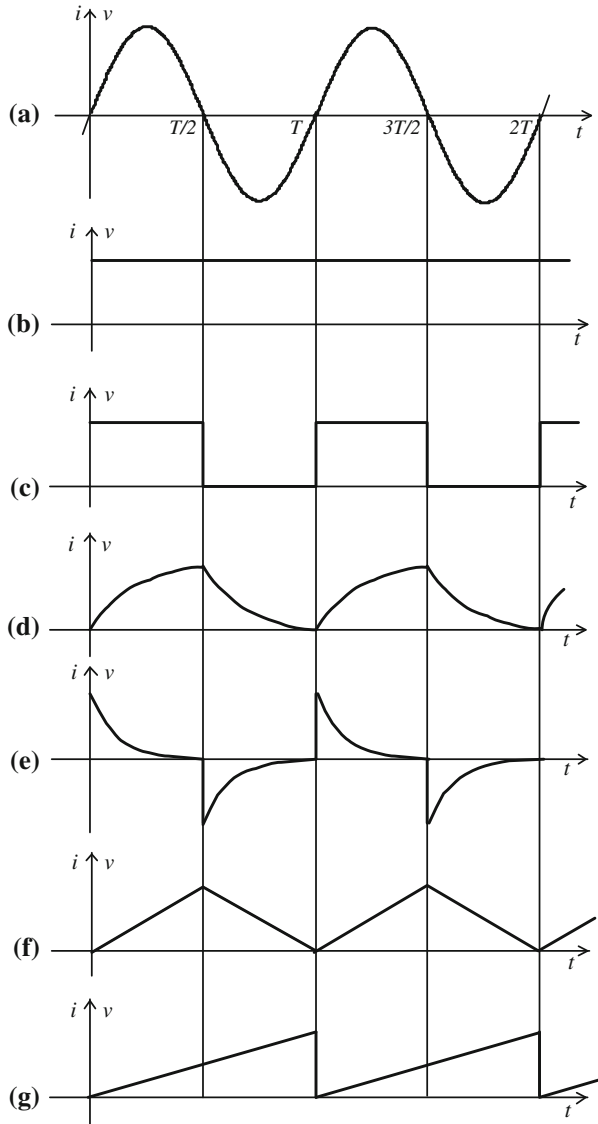


Fig. 1.1 The most frequent voltage and current waveforms in power electronics circuits

Input and output voltages or currents are mainly either harmonic functions of time (Fig. 1.1a) or time-independent. The time-independent signals (Fig. 1.1b) are called direct current signals as they act in only one direction. The most frequent forms of signals inside power electronics equipment are rectangular (Fig. 1.1c). These signals are obtained at the outputs of the DC voltage supplied switching circuits as a consequence of the operation of the ON/OFF switch. A rectangular

excitation of a circuit within the equipment results in responses that may be exponential (Fig. 1.1d, e), triangular (Fig. 1.1f), sawtooth (Fig. 1.1g) or harmonic functions of time. They are mostly periodic functions of time. Their values and directions are repeated after a precisely determined time interval T which is called the cycle, so that:

$$f(t + kT) = f(t), k = \pm 1, \pm 2, \dots \quad (1.1)$$

On the basis of the Fourier analysis, arbitrary periodic functions can be expanded in a series of harmonic functions with different amplitudes and frequencies. A Fourier series of any periodic function can be represented in the form of a sum of a DC component and harmonic cosine and sine functions, i.e.

$$f(t) = F_0 + \sum_{n=1}^{\infty} f_n(t) = a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \quad (1.2)$$

where a_0 , a_n and b_n are the Fourier coefficients determined by:

$$F_0 = a_0 = \frac{1}{T} \int_0^T f(t) dt, \quad (1.3)$$

$$a_n = \frac{2}{T} \int_0^T f(t) \cos(n\omega t) dt, \quad (1.4)$$

$$b_n = \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt. \quad (1.5)$$

The coefficient $F_0 = a_0$ is the average value of a complex-periodic function, or its DC component. By using the basic trigonometric relations, the Fourier series (1.2) can be expressed in terms of cosine only or sine only, namely

$$f(t) = a_0 + \sum_{n=1}^{\infty} C_n \cos(n\omega t + \theta_n), \quad (1.6)$$

where

$$C_n = \sqrt{a_n^2 + b_n^2} \quad \text{and} \quad \theta_n = \tan^{-1}(-b_n/a_n), \quad (1.7)$$

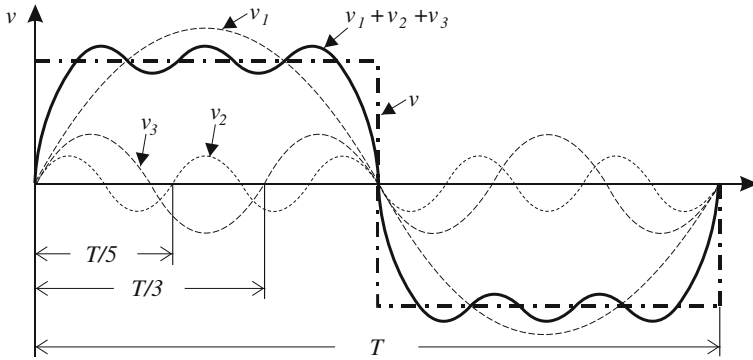


Fig. 1.2 A symmetric rectangular signal (dash-dot line) and its Fourier equivalent (full line) consisting of only the first three terms of the Fourier series

i.e.

$$f(t) = a_0 + \sum_{n=1}^{\infty} C_n \sin(n\omega t + \theta_n), \quad (1.8)$$

where

$$C_n = \sqrt{a_n^2 + b_n^2} \quad \text{and} \quad \theta_n = \tan^{-1}(a_n/b_n). \quad (1.9)$$

The coefficient C_1 is the amplitude of the first or the basic harmonic whose circular frequency $\omega = 2\pi/T$ is equal to the frequency of the complex-periodic function. The higher frequency terms ($2\omega, 3\omega, 4\omega, \dots$) are called higher harmonics. In Fig. 1.2a symmetric rectangular signal (dash-dot line) is represented by the sum of only the first three members of the Fourier series (full line). This rectangular signal contains only odd harmonics. Its Fourier series is:

$$f(t) = F \sin(\omega t) + \frac{F}{3} \sin(3\omega) + \frac{F}{5} \sin(5\omega t) + \frac{F}{7} \sin(7\omega t) + \dots, \quad (1.10)$$

where F is the amplitude of the basic harmonic. With a higher number of harmonics the sum would come closer to the rectangular function, while the infinite sum would produce a complete rectangular form of the signal.

1.2 Root-Mean-Square and Average Values of Periodic Signals

The root-mean-square (RMS) value of a variable periodic current is equal to the value of a DC current which would develop the same amount of heat during the same time interval within the same resistor, i.e. which does the same amount of work. The work of the periodic current through a resistor R over a period T is determined by:

$$W_1 = \int_0^T v(t)i(t)dt = \int_0^T [Ri(t)]i(t)dt = R \int_0^T i^2(t)dt, \quad (1.11)$$

whereas the work of the DC current equal to the RMS value of the variable current in the same resistor over the same period T is

$$W_2 = RI_{\text{rms}}^2 T. \quad (1.12)$$

By equating these two works, i.e. $W_1 = W_2$, it follows that the RMS value of a periodic current is

$$I_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T i^2(t)dt}. \quad (1.13)$$

Similarly, the RMS value of a periodic voltage is obtained as:

$$V_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T v^2(t)dt}. \quad (1.14)$$

For example, for a harmonic voltage $v(t) = V_M \sin(\omega t)$ the RMS value is:

$$V_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T V_M^2 \sin^2(\omega t)dt} = \sqrt{\frac{V_M^2}{T} \int_0^T [1 - \cos(2\omega t)]dt} = \frac{V_M}{\sqrt{2}} = 0.707 V_M, \quad (1.15)$$

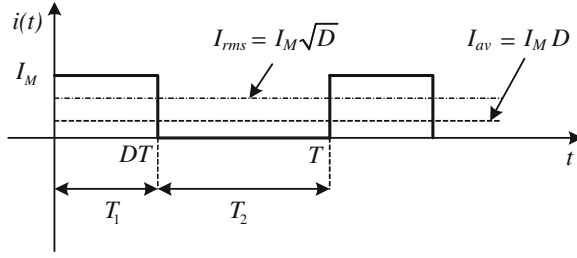


Fig. 1.3 A current of a rectangular form of duty cycle $0 < D < 1$, its RMS and average vales

and the RMS value of a harmonic current of the form $i(t) = I_M \sin(\omega t)$ is:

$$I_{rms} = I_M / \sqrt{2} = 0.707 I_M. \quad (1.16)$$

The RMS value denotes the real influence of a harmonic current or voltage. For this reason it is mostly used without the index rms and is shortly denoted by I or V . For example, $V = 220$ V is the rms value of the mains voltage. Its amplitude is $V_M = \sqrt{2} \times 220 = 310$ V.

For a periodic function of a rectangular form (Fig. 1.3), determined by (1.17),

$$i(t) = \begin{cases} I_M, & 0 \leq t < T_1 = DT \\ 0, & DT < t < T, \end{cases} \quad (1.17)$$

the rms value is

$$I_{rms} = \sqrt{\frac{1}{T} \left\{ \int_0^{DT} I_M^2 dt + \int_{DT}^T 0^2 dt \right\}} = \sqrt{\frac{1}{T} I_M^2 (DT)} = I_M \sqrt{D}, \quad (1.18)$$

where $D = T_1/T$ is the duty cycle of the rectangular pulse.

The average value of a periodic signal within one period is defined as:

$$f_{av} = \frac{1}{T} \int_0^T f(t) dt. \quad (1.19)$$

For a current of a rectangular form, according to Fig. 1.3, it is

$$I_{av} = \frac{1}{T} \int_0^{DT} I_M dt = DI_M. \quad (1.20)$$

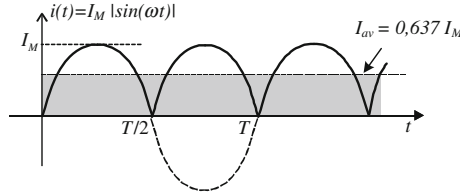


Fig. 1.4 The rectified harmonic current and its mean value

Practically, the average value represents the area between the pulse and the time axis over a single period, divided by that period. The average value of a harmonic signal of the form $f(t) = F_M \sin(\omega t)$ is zero since it consists of two equal areas with opposite signs (positive and negative half-periods). In some of the circuits of power electronics, such as rectifiers, the use is made of the rectified current (Fig. 1.4), where all the parts are positive, while the original form of the wave is retained. The cycle of such a signal is $T/2$, and the mean value is

$$I_{av} = \frac{1}{T/2} \int_0^{T/2} I_M \sin(\omega t) dt = \frac{2I_M}{\pi} \approx 0.637 I_M. \quad (1.21)$$

For complex-periodic currents the use is made of the form factor, as the measure of the discrepancy from the harmonic form, defined as

$$k = \frac{I_{rms}}{I_{av}} = \frac{I}{I_{av}}. \quad (1.22)$$

The form factor of a rectangular current according to Fig. 1.3 is $k = I_M \sqrt{D} / (I_M D) = 1/\sqrt{D}$ whereas for a rectified harmonic current it is $k = (I_M/\sqrt{2}) / (2I_M/\pi) = \pi/(2\sqrt{2}) = 1.11$.

As a measure of the discrepancy of a periodic signal from the harmonic form of a current/voltage signal the use is often made of either the distortion factor

$$DF = \frac{I_{1rms}}{I_{rms}}, \quad (1.23)$$

or of the total harmonic distortion

$$THD = \frac{\sqrt{I_{rms}^2 - I_{1rms}^2}}{I_{1rms}} = \frac{\sqrt{1 - DF^2}}{DF}, \quad (1.24)$$

where I_{rms} is the RMS value of the first harmonic and

$$I_{\text{rms}} = \sqrt{\sum_{n=0}^{\infty} I_{n\text{rms}}^2} = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \left(\frac{I_n}{\sqrt{2}}\right)^2} \quad (1.25)$$

is the total rms value of a complex-periodic current. In (1.25) I_0 is the DC component, and I_n is the amplitude of the n -th harmonic. If the DC component is zero, the total harmonic distortion is

$$\text{TDH} = \frac{\sum_{n=2}^{\infty} I_{n\text{rms}}^2}{I_{\text{rms}}}. \quad (1.26)$$

Example 1.1 Determine the effective (rms) value of $v(t) = 5 + 10 \sin(\omega_1 t + 30^\circ) + 12 \sin(\omega_2 t + 60^\circ)$ for:

- (a) $\omega_2 = 2\omega_1$
- (b) $\omega_2 = \omega_1$.

When the sinusoids are of different frequencies, and the terms are orthogonal, rms value is:

$$V_{\text{rms}} = \sqrt{V^2 + V_{\text{rms}}^2 + V_{\text{rms}}^2} = \sqrt{5^2 + \left(\frac{10}{\sqrt{2}}\right)^2 + \left(\frac{12}{\sqrt{2}}\right)^2} = 12.12 \text{ V}$$

- (a) First, we combine sinusoids using phasor addition:

$$\begin{aligned} 10 \sin(\omega_1 t + 30^\circ) + 12 \sin(\omega_1 t + 60^\circ) &= 14.66 \sin(\omega_1 t) + 15.39 \cos(\omega_1 t) \\ &= 21.25 \sin(\omega_1 t + 46^\circ) \text{ V}. \end{aligned}$$

The voltage function is then expressed as:

$$v(t) = 5 + 21.25 \sin(\omega_1 t + 46^\circ) \text{ V}$$

The rms value of voltage v is:

$$V_{\text{rms}} = \sqrt{V^2 + V_{\text{rms}}^2} = \sqrt{5^2 + \left(\frac{21.25}{\sqrt{2}}\right)^2} = 15.83 \text{ V}$$

1.3 Power of Periodic Currents

The product of the instantaneous values of a periodic voltage across a load and the current through the load is the instantaneous power:

$$p(t) = v(t)i(t). \quad (1.27)$$

Since the instantaneous values of the voltage or current could have different signs, the instantaneous power can in general be positive or negative. The power is positive if the energy is transferred from the source to the load and negative if the energy is transferred from the load to the source. A typical example of a load involving positive and negative instantaneous power is a coil and a capacitor driven by a harmonic signal. If, for example a coil of inductance L is connected to a voltage $V(t) = V_M \sin(\omega t)$, the current through the coil will be shifted by $-\pi/2$ with reference to the voltage and the instantaneous power will be

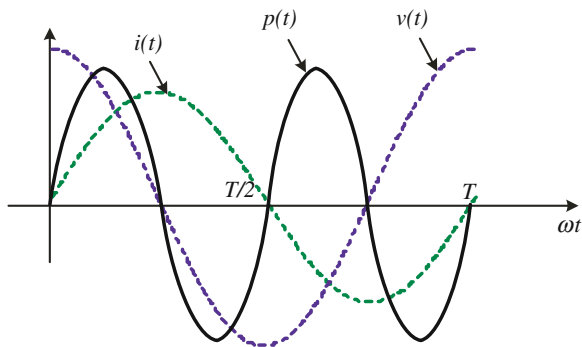
$$p(t) = [V_M \cos(\omega t)][I_M \cos(\omega t - \pi/2)] = \frac{1}{2}V_M I_M \sin(2\omega t).$$

The frequency of the instantaneous power will be double the voltage frequency (Fig. 1.5). The shaded area between the curve $p(t)$ and the time axis (Fig. 1.5) represents this work. During the first and the third quarter of the cycle this work is positive, i.e., the work of the source is converted to the energy of the magnetic field of the coil. During the other two quarters of the cycle (the second and the fourth) this work is negative, meaning that the energy of the magnetic field is returned back to the source.

During the intervals of negative instantaneous power, the coil behaves like a source and the source like a load. Energy is thus being exchanged between the source and the coil. Consequently, the total work of the source is zero and the average power is also zero.

The same conclusions may be drawn if a capacitor is driven by a harmonic signal. In two quarters of the cycle, the capacitor accumulates the electrostatic

Fig. 1.5 Instantaneous power of a coil driven by a harmonic signal



energy from the source and during the other two quarters this energy is returned back to the source. Consequently, here too the average power is equal to zero.

The average or active power is the one that does the work. For periodic currents it is defined by the time interval equal to one cycle:

$$P = \frac{1}{T} \int_0^T p(t) dt. \quad (1.28)$$

It can be shown that in the case of a capacitor the average power from the source is zero. If a capacitor is driven by a rectangular signal

$$P = \frac{1}{T} \int_0^T V_{DC} i_C(t) dt = V_{DC} \left[\frac{1}{T} \int_0^T i_C(t) dt \right] = V_{DC} I_{cav}, \quad (1.29)$$

where

$$I_{cav} = \frac{1}{T} \int_0^T i_C(t) dt, \quad (1.30)$$

is the average current through the capacitor, then the voltage across the capacitor is

$$V_C(t_0 + T) = V_C(t_0) + \frac{1}{C} \int_{t_0}^{t_0+T} i_C(t) dt. \quad (1.31)$$

Since it has been assumed that the voltage across the capacitor (source voltage) was periodic, i.e. $V_C(t_0 + T) = V_C(t_0)$ it follows that:

$$\frac{1}{C} \int_{t_0}^{t_0+T} i_C(t) dt = V_C(t_0 + T) - V_C(t_0) = 0. \quad (1.32)$$

By comparing (1.32) and (1.30), one comes to the conclusion that the average current through the capacitor is zero, thus the average power is also zero. It is shown in the same way that the average value of the voltage across a coil driven by a periodic rectangular current is also zero.

It can thus be concluded that either a coil or a capacitor dissipate no power if driven by a periodic signal. For this reason, they are called nondissipative elements. Since minimum dissipation of power is one of the basic requirements in the design of various efficient converters, coils and capacitors are the basic elements of these circuits together with the switching circuits generating periodic voltages and currents.

Example 1.2 A coil of inductance $L = 1 \text{ mH}$ and a capacitor of capacitance $1 \text{ }\mu\text{F}$ connect blocks B_1 and B_2 (Fig. 1.6a) and B_3 and B_4 (Fig. 1.6b), respectively. The current through the coil and the voltage across the capacitor are linear periodic functions determined by

$$i_L(t) = \begin{cases} 10 \text{ A} + \frac{1 \text{ A}}{0.75 \text{ ms}} t, \\ 11 \text{ A} - \frac{1 \text{ A}}{0.25 \text{ ms}} t, \end{cases} \quad (1)$$

$$t_0 < t < t_0 + 0.75 \text{ ms}, \quad t_0 + 0.75 \text{ ms} < t < t_0 + T = t_0 + 1 \text{ ms};$$

$$v_C(t) = \begin{cases} 11 \text{ V} - \frac{10 \text{ V}}{0.75 \text{ ms}} t, \\ 1 \text{ V} + \frac{10 \text{ V}}{0.25 \text{ ms}} t, \end{cases} \quad (2)$$

$$t_0 < t < t_0 + 0.75 \text{ ms}, \quad t_0 + 0.75 \text{ ms} < t < t_0 + T = t_0 + 1 \text{ ms}.$$

Draw the variations of the voltage across the coil and the current through the capacitor and determine their average values.

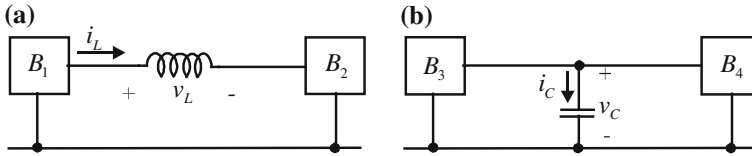


Fig. 1.6 Blocks B_1 and B_2 connected over coil (a) and capacitor (b)

The voltage across the coils is

$$V_L = L \frac{di_L}{dt}$$

$$= \begin{cases} L \frac{1 \text{ A}}{0.75 \text{ ms}} = 1 \times 10^{-3} \frac{1 \text{ A}}{0.75 \times 10^{-3}} = \frac{4}{3} \text{ V} = V_L^+, & t_0 < t < t_0 + 0.75 \text{ ms} \\ -L \frac{1 \text{ A}}{0.25 \text{ ms}} = -1 \times 10^{-3} \frac{1 \text{ A}}{0.25 \times 10^{-3}} = -4 \text{ V} = V_L^-, & t_0 + 0.75 \text{ ms} < t < t_0 + 1 \text{ ms} \end{cases}$$

The current and the voltage of the coil are drawn in Fig. 1.7.

The areas above and below the time axis within one cycle are mutually equal but of the opposite signs.

Namely

$$A = V_L^+ \times 0.75 = \frac{4}{3} \text{ V} \times 0.75 \text{ ms} = 1 \times 10^{-3} \text{ Vs}$$

$$A = V_L^- \times 0.25 = -4 \text{ V} \times 0.25 \text{ ms} = -1 \times 10^{-3} \text{ Vs}.$$

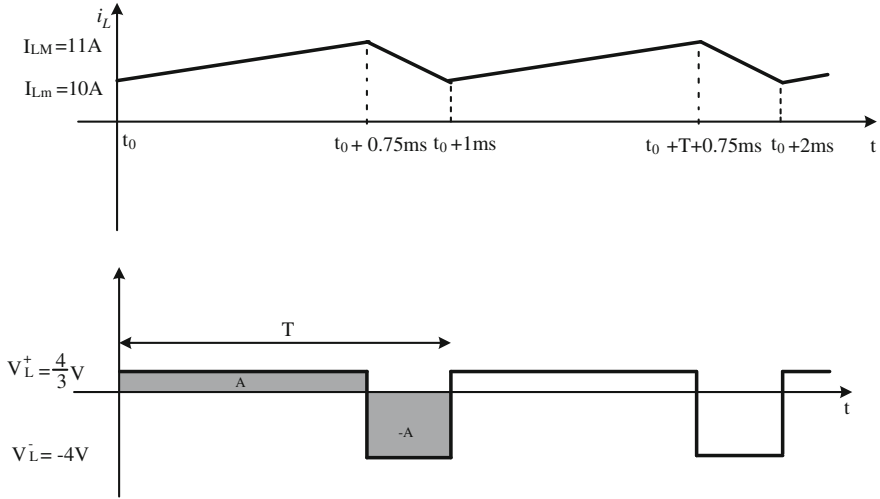


Fig. 1.7 Waveforms of the current and voltage the coil for the circuit shown in Fig. 1.6a

The average value of the voltage across the coil is

$$\begin{aligned}
 V_{Lav} &= \frac{1}{T} \int_{t_0}^{t_0+T} V_L(t) dt = \frac{1}{T} \left[\int_{t_0}^{t_0+0.75} V_L^+ dt + \int_{t_0+0.75}^{t_0+1} V_L^- dt \right] \\
 &= \frac{1}{T} (4/3 \times 0.75 - 4 \times 0.25) = \frac{1}{T} (A - A) = 0
 \end{aligned}$$

The current through the capacitor is:

$$i_C = C \frac{dv_C}{dt} = \begin{cases} -C \frac{10V}{0.75ms} = -1 \times 10^{-6} F \frac{10V}{0.75 \times 10^{-3} s} = -\frac{40}{3} \text{ mA} = I_C^-, \\ C \frac{10V}{0.25ms} = 1 \times 10^{-6} F \frac{10V}{0.25 \times 10^{-3} s} = 40 \text{ mA} = I_C^+, \end{cases}$$

The voltage and the current of the capacitor are drawn in Fig. 1.8.

The areas below and above the time axis are

$$\begin{aligned}
 -A &= I_C^- \times 0.75 \text{ ms} = \frac{-40}{3} \text{ mA} \times 0.75 \text{ ms} = -10 \text{ As}, \\
 +A &= I_C^+ \times 0.25 \text{ ms} = 40 \text{ mA} \times 0.25 \text{ ms} = +10 \text{ As}.
 \end{aligned}$$

The average current through the capacitor is

$$I_{Cav} = \frac{1}{T} \int_{t_0}^{t_0+T} i_C(t) dt = \frac{1}{T} (-A + A) = 0$$

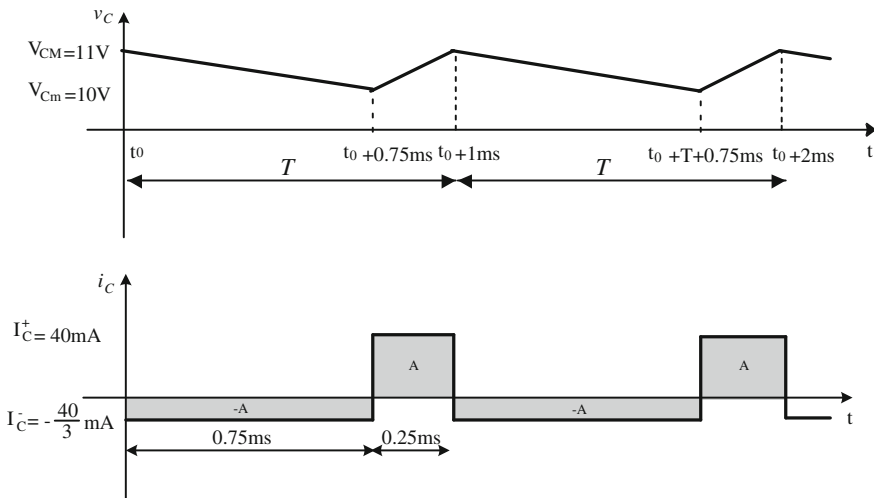


Fig. 1.8 Waveforms of the voltage and current the capacitor for the circuit shown in Fig. 1.6b

In general, however, when the load is an impedance $Z = |Z|e^{j\varphi}$, there will be a phase shift φ between the current and the voltage. If $V = V_M \cos(\omega t)$, then $i = I_M \cos(\omega t - \varphi)$ and the power active power is

$$P = V_M I_M \frac{1}{T} \int_0^T [\cos(\omega t)] [\cos(\omega t - \varphi)] dt = \frac{1}{2T} V_M I_M \int_0^T \cos \varphi dt, \quad (1.33)$$

i.e. since $V_M = \sqrt{2}V_{\text{rms}}$ and $I_M = \sqrt{2}I_{\text{rms}}$,

$$P = V_{\text{rms}} I_{\text{rms}} \cos(\varphi) = VI \cos(\varphi). \quad (1.34)$$

Thus, the active power is the product of the rms values of the voltage and the current and the cosine of the angle between the load voltage and the current. The power is maximum when the load voltage and the current are in phase ($\varphi = 0$), which is the case of a purely resistive load. In a resistor the electric energy is converted to thermal energy. If $\varphi = \pm\pi/2$, as in the case of a coil or capacitor, $\cos(\varphi) = 0$, and the active power in these elements is zero.

The phasor diagram of the voltage and a current which is phase shifted by φ is shown in Fig. 1.9. Bearing in mind (1.34), the work is performed only by voltage component $V \cos \varphi$ which is in phase with the current, so $V \cos \varphi$ is called the voltage component for active power. In addition, there is a passive component $V \sin \varphi$, which is orthogonal to the current vector. This component does not perform any work, i.e., it does not transform the electrical work of the source, so the corresponding power is called the reactive power and it is equal to

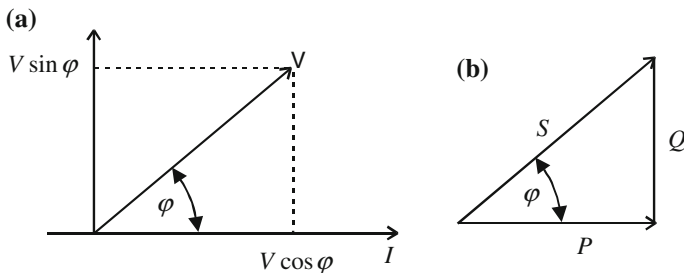


Fig. 1.9 The components of a voltage phasor for active and reactive powers (a) and power triangle (b)

$$Q = \frac{1}{2} V_M I_M \sin \varphi = VI \sin \varphi. \quad (1.35)$$

The reactive power is understood as the energy alternatively exchanged between the source and the load. The vector sum of the active and reactive powers

$$S = P + jQ \quad (1.36)$$

is the apparent power. Its modulus is

$$S = |S| = \sqrt{P^2 + Q^2} = VI. \quad (1.37)$$

Thus, the apparent power is the product of the rms values of the load voltage and the current.

The ratio of the active and apparent powers is called the power factor:

$$\text{PF} = \frac{P}{S} = \cos \varphi. \quad (1.38)$$

Therefore, the power factor of harmonic currents and voltages is $\cos \varphi$. If the current or the voltage is a complex-periodic function, then (1.38) should be multiplied by the distortion factor (1.23), i.e.

$$\text{PF} = \text{DF} \cos \varphi. \quad (1.39)$$

Example 1.3 A nonsinusoidal voltage is $v(t) = 5 + 10 \sin(2\pi 50 t + 30^\circ) + 15 \sin(4\pi 50 t + 45^\circ)$. This voltage is connected to the load which is a serial connection of a $10 \, \Omega$ resistor and a $10 \, \text{mH}$ inductance.

- Determine the power absorbed by the load, and
- derive an expression for the load current.

(a) The power absorbed by the load can be determined by the next equation:

$P = I_{\text{rms}}^2 R$. The DC current term is: $I_0 = \frac{V_0}{R} = 0.5 \text{ A}$.

The amplitudes of the ac current terms are

$$I_1 = \frac{V_1}{\sqrt{R^2 + (\omega_1 L)^2}} = \frac{10}{\sqrt{10^2 + (2\pi 50 \times 0.01)^2}} = 0.98 \text{ A}$$

$$I_2 = \frac{V_2}{\sqrt{R^2 + (\omega_2 L)^2}} = \frac{15}{\sqrt{10^2 + (4\pi 50 \times 0.01)^2}} = 1.45 \text{ A}$$

The rms value of the load current is

$$I_{\text{rms}} = \sqrt{I_0^2 + I_{1,\text{rms}}^2 + I_{2,\text{rms}}^2} = \sqrt{I_0^2 + \left(\frac{I_1}{\sqrt{2}}\right)^2 + \left(\frac{I_2}{\sqrt{2}}\right)^2}$$

$$= \sqrt{0.5^2 + \left(\frac{0.98}{\sqrt{2}}\right)^2 + \left(\frac{1.45}{\sqrt{2}}\right)^2} = 1.33 \text{ A}$$

The power absorbed by the load is

$$P = 1.33^2 \times 10 = 17.69 \text{ W}.$$

(b) The phase angles of the ac current terms are

$$\varphi_2 = 45^\circ - \arctg\left(\frac{4\pi 50 \times 0.01}{10}\right) = -11^\circ \varphi_1 = 30^\circ - \arctg\left(\frac{2\pi 50 \times 0.01}{10}\right) = 0^\circ$$

The load current can be expressed as

$$i(t) = 0.5 + 0.98 \sin(2\pi 50 t) + 1.45 \sin(4\pi 50 t - 11^\circ) \text{ A}$$

Example 1.4 The waveforms of voltage and current at a single phase load are recorded and presented in the analytical form:

$$v(t) = 100 + 320 \sin(2\pi 50 t) \text{ V}$$

$$i(t) = 20 \sin\left(2\pi 50 t - \frac{\pi}{4}\right) + 20 \sin\left(2\pi 100 t - \frac{\pi}{3}\right) \text{ A}$$

Determine:

- (a) the power absorbed by the load, and
- (b) the power factor.

(a) The power absorbed by the load is determined by computing the absorbed power at each frequency

$$P = V_0 I_0 + \sum_{i=1}^n \left(\frac{V_i I_i}{2} \right) \cos(\vartheta_i - \psi_i) = \frac{320 \times 20}{2} \cos\left(\frac{\pi}{4}\right) = 2.26 \text{ kW}$$

(b) The power factor is calculated by Eq. (1.38)

$$\text{PF} = \frac{P}{S} = \frac{P}{V_{\text{rms}} I_{\text{rms}}}$$

The rms values of the load current and voltage are:

$$V_{\text{rms}} = \sqrt{100^2 + \left(\frac{320}{\sqrt{2}}\right)^2} = 247.38 \text{ V}$$

$$I_{\text{rms}} = \sqrt{\left(\frac{20}{\sqrt{2}}\right)^2 + \left(\frac{20}{\sqrt{2}}\right)^2} = 20 \text{ A}$$

The power factor is

$$\text{PF} = \frac{2260}{247.38 \times 20} = 0.46.$$

1.4 Switching Elements

Switching elements are the constituent parts of the switching circuits (Fig. 1.10a). The basic switching circuit consists of a switch, a load, a power supply, and a control circuit. The control signal V_{cont} governs the state of the switch. The ideal switch should behave as an open circuit (infinite resistance) when OFF and as a short circuit (zero resistance) when ON. The static characteristic of the switch is nonlinear (Fig. 1.10b). In the OFF state, it coincides with the abscissa and in the ON state it coincides with the ordinate. Thus, in the ON state the voltage across the ideal switch is zero and in the OFF state the current through the switch is zero. Consequently, the power of dissipation of the switch is zero in these states, $p_p = V_p I_p = 0$. These states are called the static states. The ideal switch is instantly ON or OFF, meaning that the transition times from one state to the other are zero.

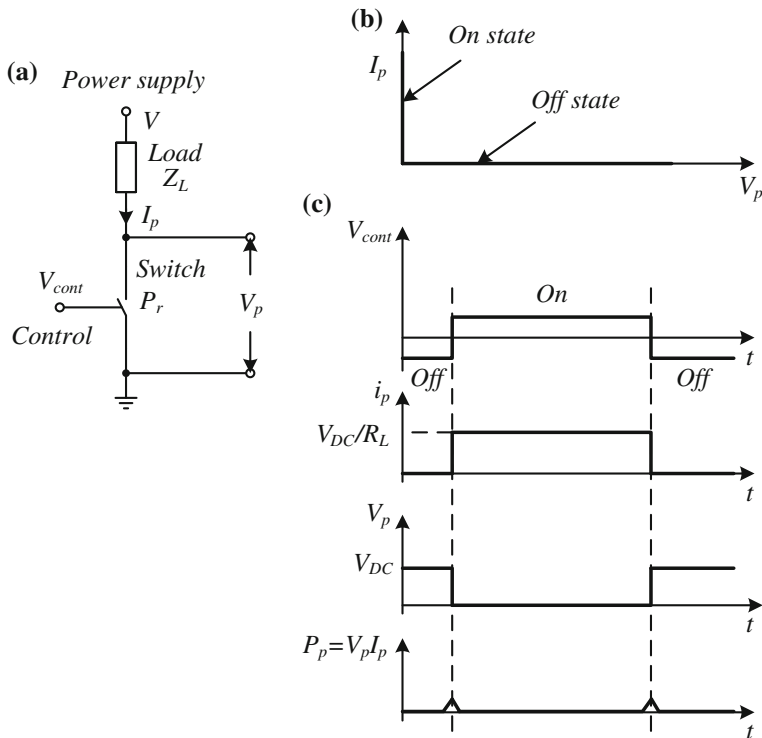


Fig. 1.10 Basic circuit (a), static characteristic of an ideal switch (b), and the current I_p , voltage V_p , and power dissipation p_p of an ideal switch (c) for a DC power supply (V_{DC}) and resistive load R_L

No electronic switch, however, behaves ideally. A real switching element is characterized by:

- finite resistance when OFF,
- nonzero resistance when ON,
- transition times from ON to OFF state and vice versa greater than zero, and
- dissipation of power in the switch.

The static and dynamic characteristics of a real switch are shown in Fig. 1.11. In most cases, the voltage in the on state and the current in the off state are negligible. Thus, the power of dissipation of a real switch in the static state is also negligible. In the transient condition, while changing the state of the switch, both current and voltage are present (Fig. 1.11b) and the instantaneous value of dissipation may be significant.

The transition times from one static state to the other are dependent on the frequency characteristics of the switching element, the character of the load, and the control circuit. They do not depend on the switching cycle T . Therefore, the average power dissipated by a switching element will grow with the decrease of T . Dynamic power dissipation at high frequencies may be considerable. For this reason, the

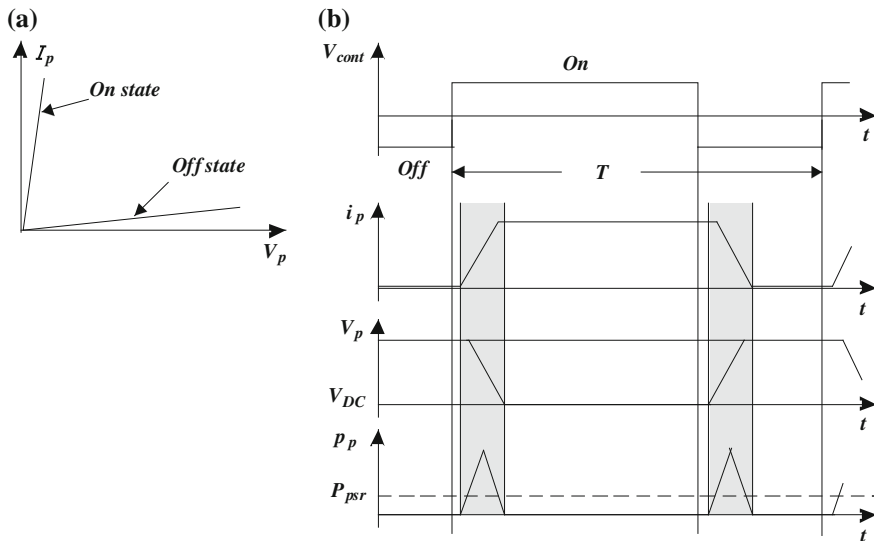


Fig. 1.11 Characteristics of a real switch: static (a) and dynamic (b)

maximum frequency of a switching circuit is limited not only by the turn-ON/turn-OFF times but also by the permitted power dissipation of the switch. This is particularly true for power switches and it is this type of switch that is predominantly used in power electronics.

The power semiconductor elements like diodes, bipolar or MOS transistors, thyristors, and BiMOS transistors are used as the switching elements. A common requirement for all of these elements is that the control of signals carrying considerable power has to be done by as short turn-ON/turn-OFF times as possible.

Power diodes can be classified into three groups: general purpose, very fast, and Schottky. The operating voltages and currents of general purpose diodes may range up to 3,000 V and 3,500 A, and those of very fast diodes up to 3,000 V and 1,000 A. The reverse recovery times are in the range from several hundreds nanoseconds to several microseconds. Schottky diodes have lower forward voltages and very short recovery times (below 10 ns). However, the reverse saturation current grows with the power of the diode so the characteristics are limited to 100 V and 300 A. Diodes are two terminal devices. This limits their applications as switches as the control load circuits are common.

Power bipolar transistors (PBT) are characterized by a very small collector-emitter on (saturation) resistance, from several $\text{m}\Omega$ to several tens of $\text{m}\Omega$. Owing to this, the collector-emitter on (saturation) voltage is within the limits of 0.5–1.5 V even at very high collector currents. The maximum voltages and currents range up to 1,200 V and 400 A. The maximum frequency of the pulse DC/DC converters using PBT as switches runs up to several tens (20–30) of kilohertz. PBTs as switches are mainly used in the common-emitter connection. The control is

implemented via a base circuit. If a turned-ON transistor is to reach the saturation region, in addition to the forward bias of the base-emitter junction, a sufficiently large base current is required so that the base-collector junction is also forward biased. Consequently, the control circuit requires a relatively large power.

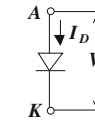
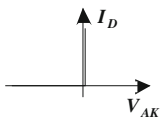
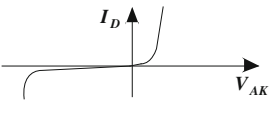
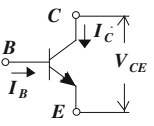
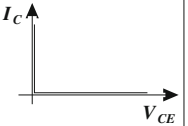
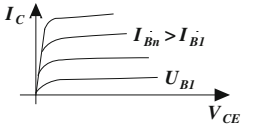
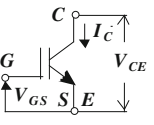
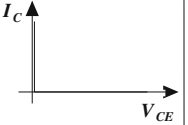
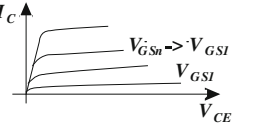
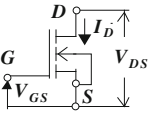
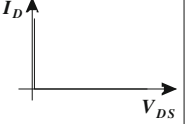
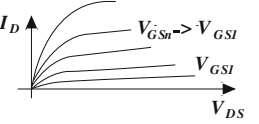
The power MOS transistors have recently been finding an increased use in the pulse converters. They are faster than PBTs and the maximum frequency of the converters based on power MOS devices ranges up to 100–200 kHz. The rated voltages and currents are smaller than those of PBT and are within the range of 1,000 V and 50 A, respectively. The input impedance of MOS transistors is high (of the order of $10^9 \Omega$), thus for their control it is sufficient to provide the corresponding gate-source voltage. Since the gate current is practically zero, there is no dissipation in the control circuit. Therefore, an MOS transistor is a voltage controlled switch compared to a PBT which is a current controlled switch.

The basic weakness of power MOSFETs is a relatively large on resistance (from several hundreds $m\Omega$ up to several Ω). This was the reason for the development of several types of BiMOS transistors which unite good properties of both bipolar transistors (small on resistance) and MOS (negligible driving current). One of these types is the insulated gate bipolar transistor (IGBT). Its input characteristics are like those of an MOS transistor and the output characteristics are like those of a PBT. The maximum voltages and currents range up to 1,200 V and 400 A and the maximum frequencies up to several tens of kHz (like PBT). The frequency characteristics of the static induction transistors (similar to JFET) have been improved. The maximum ratings of this type of transistor are 1,200 V, 300 A, and 100 kHz.

The characteristics and symbols of nonregenerative semiconductor switches (diodes, BT, and MOSFET) are shown in Table 1.1.

The thyristor is a representative of the regenerative switches (the switches where the change of state is supported by a positive feedback). In addition to the regenerative process, the essential difference compared to the PBT and MOSFET is in that the thyristors are turned on by feeding short pulses (several tens of milliseconds) to the gate. After switch-ON, a thyristor remains on even if the driving signal is removed from the gate. For the PBT and MOSFET devices the driving signal must be present throughout the on state. Thyristors are very powerful elements. The maximum voltages and currents range up to 10,000 V or A, respectively. Today a whole family of thyristors is commercially available. Each member of this family is specific regarding both its characteristics and its applications. The V–I characteristic, the symbol, and the equivalent circuit are shown in Table 1.2. A standard thyristor (SCR) is turned on by a positive pulse at the gate, but it cannot be turned off by a gate signal. The gate turn-off (GTO) and self-turn-off (SITH) are the self-turn-off thyristors. They are turned on by positive and turned off by negative pulses at the gate. The maximum voltages and currents of GTO thyristors are respectively 4,000 V and 3,000 A, and of SITH thyristors 1,200 V and 300 A. The maximum frequency of SITH is high and ranges up to several hundred kHz. Another thyristor type can be turned off at the gate. This is the MOS-controlled thyristor (MCT). Its

Table 1.1 Characteristics and symbols of nonregenerative switches

Element	Symbol	Ideal Characteristic	Real Characteristic
Diode			
Bipolar NPN Transistor			
IGBT			
MOSFET			

maximum ratings are 1,000 V and 100 A. A triac is an AC switch. Practically, it consists of two thyristors in anti-parallel connection and its characteristic in the I and III quadrants is symmetric. Its maximum ratings are 1,200 V, 300 A, and 400 Hz.

The reverse conduction thyristor (RCT) also can conduct in both half-cycles of an AC voltage. Practically, this is a thyristor with a diode in anti-parallel connection, the diode conducting during the negative half-cycle. The maximum ratings of the RCT are 2,500 V, 1,000 A forward, and 400 A reverse current.

In addition to the triode-type thyristors, there are several types of the diode-type thyristors (two-terminal devices without a control terminal). The four-layer diode and diac belong to this group. They are mainly used as switches for triggering thyristors.

Table 1.3 gives the comparative values of the basic parameters of semiconductor power switches. The qualitative characteristics of the most frequently used switching elements are presented in Table 1.4.

Table 1.2 Symbols, equivalent circuits, and V–I characteristics of regenerative switches

Type	Name	Symbol	Equivalent circuit	Characteristic
UNILATERAL	<i>UJT /</i> <i>UniJunction Transistor</i>			
	<i>CUJT /</i> <i>Complementary Unijunction Transistor</i>			
	<i>PUT /</i> <i>Programmable Unijunction Transistor</i>			
	<i>BOD /</i> <i>BreakOver Diode</i>			
	<i>SUS /</i> <i>Silicon Unilateral Switch</i>			
	<i>SCR /</i> <i>Silicon Controlled Rectifier</i>			
	<i>GATT /</i> <i>Gate Assisted Turn-off Thyristor</i>			
	<i>GTO /</i> <i>Gate Turn-off</i>			
	<i>LASCR /</i> <i>Light Activated SCR</i>			

(continued)

Table 1.2 (continued)

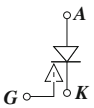
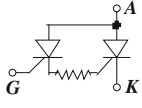
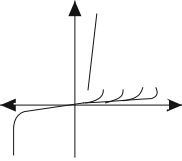
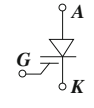
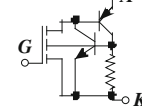
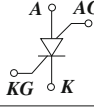
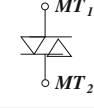
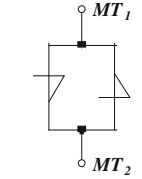
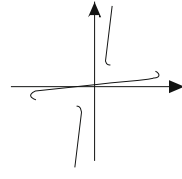
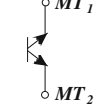
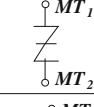
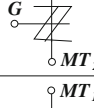
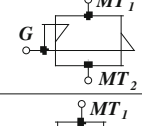
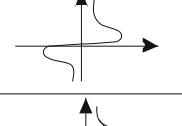
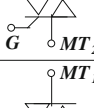
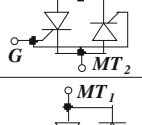
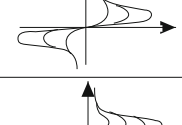
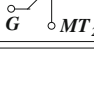
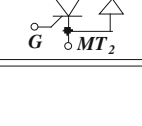
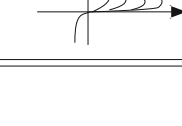
	<i>AGT /</i> <i>Amplifying</i> <i>Gate</i> <i>Thyristor</i>			
	<i>MCT /</i> <i>MOS</i> <i>Controlled</i> <i>Thyristor</i>			
	<i>SCS /</i> <i>Silicon</i> <i>Controlled</i> <i>Switch</i>			
	<i>ASCR /</i> <i>Assymetrical</i> <i>Silicon</i> <i>Controlled</i> <i>Rectifier</i>	<i>As SCR</i>	<i>As SCR</i>	
B I L A T E R A L	<i>DIAC /</i> <i>Diode</i> <i>AC</i>			
	<i>Triger /</i> <i>DIAC NPN</i>			
	<i>SIDAC /</i> <i>Silicon</i> <i>Diode</i> <i>AC</i>			
	<i>SBS /</i> <i>Silicon</i> <i>Baterial</i> <i>Switch</i>			
	<i>TRIAC /</i> <i>TRiode</i> <i>AC</i>			
	<i>RCT /</i> <i>Reverse</i> <i>Conducting</i> <i>Thyristor</i>			

Table 1.3 Characteristics of semiconductor power switches [1]

Class	Type	Maximum volt- age/current (V/A)	Maximum fre- quency (kHz)	Switching time (μs)	On resistance
Diode	General purpose	5,000/5,000	1	100	0.16 mΩ
	Very fast	3,000/1,000	10	2–5	1 mΩ
	Schottky	40/60	20	0.23	10 mΩ
Thyristors	SCR	5,000/5,000	1	200	0.25 mΩ
	RCT				
	GATT	2,500/400	5	40	2.16 mΩ
	GTO				
	SITH	2,500/1,000	5	40	2.1 mΩ
	MCT				
		1,200/400	20	8	2.24 mΩ
		4,500/3,000	10	15	2.5 mΩ
		4,000/2,200	20	6.5	5.75 mΩ
		600/60	20	2.2	18 mΩ
Bipolar transistors	Darlington	400/250	20	9	4 mΩ
		400/40	20	6	31 mΩ
		630/50	25	1.7	15 mΩ
		1,200/400	10	30	10 mΩ
MOSFET		500/8.6	100	0.7	0.6 Ω
		1000/4.7	100	0.9	2 Ω
		500/50	100	0.6	0.4 Ω
IGBT		1,200/400	20	2.2	18 mΩ
SIT		1,200/300	100	0.55	1.2 Ω

Table 1.4 Qualitative characteristics of switching elements containing control electrode

Element	Power	Speed
BJT	Medium	Medium
MOSFET	Low	High
SCR	High	Low
GTO	High	Slow
IGBT	Medium	Medium
MCT	Medium	Medium

In order to obtain a better idea about the characteristics of individual elements, Fig. 1.12 illustrates their applications with respect to frequency, voltage, and current [2].

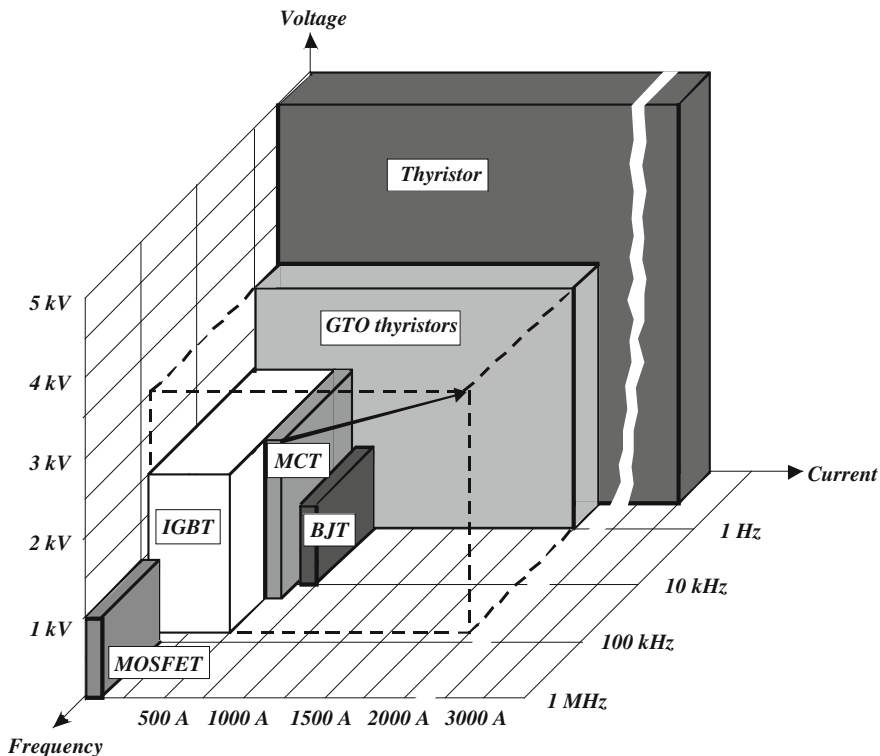


Fig. 1.12 Maximum characteristics of semiconductor power switches with respect to frequency, voltage, and current

1.5 Magnetic Elements

Pulse transformers, chokes, and resonant coils have found applications among the available magnetic elements. Transformers are used for galvanic separation and impedance matching, and chokes are used for filtering. These elements operate at frequencies above 20 kHz and their dimensions are much smaller compared to those used in linear converters. The basic equation of the mid- and high-frequency transformers can be written in the form

$$V_1 = 4N_1 S B f, \quad (1.40)$$

where V_1 is the rectangular input voltage, N_1 is the number of primary turns, S is the cross-section of the magnetic core, B is the maximum value of induction in the core, and f is the operating frequency. The product $N_1 S$ is a measure of the volume and weight of a transformer as N_1 is the measure of the amount of copper used and S is the measure of the magnetic material used. For a given input voltage, the volume and

Table 1.5 Geometric dimensions of some of the standard ferrite cores

Class of core	Type	l_e (cm)	S_e (cm ²)	V_e (cm ³)
Pot	P 7 × 4	1	0.07	0.07
	P 11 × 7	1.59	0.159	0.252
	P 14 × 8	2	0.25	0.5
	P 30 × 19	4.5	1.36	6.1
	P 42 × 29	6.86	2.65	18.2
EE	EE 20	4.3	0.31	1.34
	EE 30	6.7	0.6	4
	EE 42/20	9.7	2.4	23.3
	EE 55/25	12.3	4.2	52
EC	EC 35	7.74	0.84	6.53
	EC 52	10.5	1.8	18.8
	EC 70	14.4	2.79	40.1
U	U 15	4.8	0.32	1.54
	U 25	8.6	1.05	9.03
	U 57	16.3	1.71	27.9

weight are thus inversely proportional to the product Bf . If it is assumed that in mains transformers that $B = 1.8$ T, then $Bf = 1.8 \times 50 = 90$ T/s. For pulse transformers the maximum induction is about 0.3 T. If the frequency is 30 kHz, then $Bf = 9,000$ T/s. This means that pulse transformers are capable of transferring considerably higher powers per unit volume and weight compared to the mains transformers.

Owing to an increased operating frequency, special materials like ferrites or highly alloyed laminated metal must be used in pulse transformers. Ferrite cores are predominantly used. Namely, it is technologically simple to fashion the required shapes of cores which facilitates the realization of optimally designed transformers. Moreover, bulk conductivity of ferrite cores is very low so that eddy current losses are practically negligible. Mainly the EC, EE, U or X cores are used. For an optimally designed transformer, it is necessary to have data about its magnetic material and the core geometry. Table 1.5 presents the data for effective lengths of magnetic force lines l_e , cross-sections S_e , and volumes V_e of some of the standard ferrite cores.

Total losses in magnetic material consist of hysteresis, residual, and eddy current losses. In ferrite cores hysteresis losses prevail. These losses increase with frequency and maximum variation of induction ΔB per switching cycle. Catalogues specify maximum induction for bipolar symmetric driving, $B_{ac} = \Delta B/2$. In order to prevent shifting of the core to the saturation region, most of the time $B_{ac} < 0.3T$, but at frequencies close to 1 MHz the limitation is between 30 and 50 mT. Figure 1.13 shows the losses in materials N49 and N59 (manufacturer Siemens) for $B_m = 50$ mT at frequencies 500 kHz and 1 MHz.

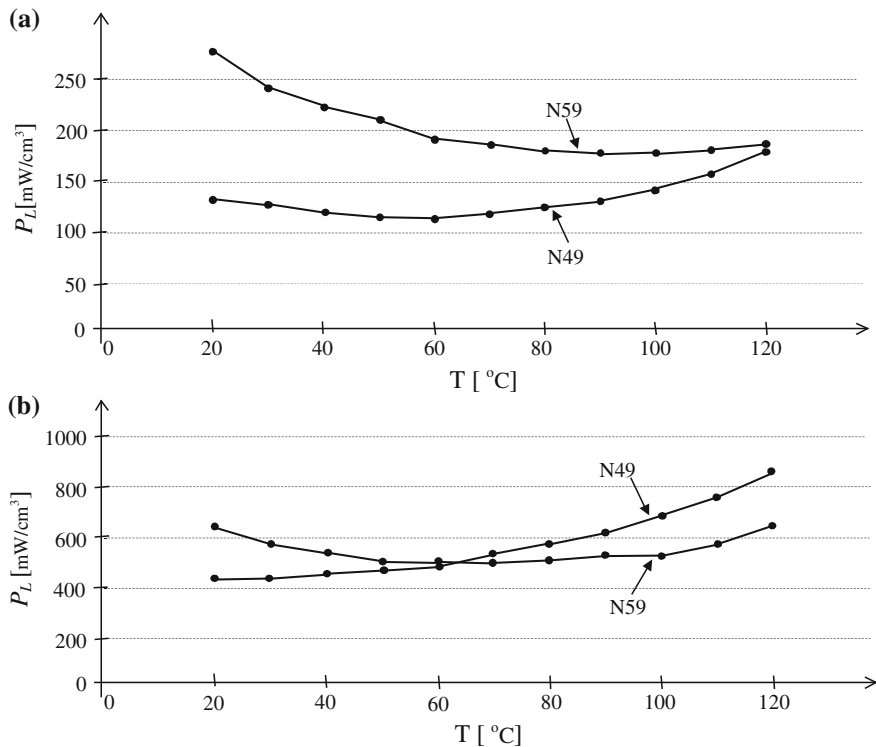


Fig. 1.13 Losses in ferrite materials N49 and N59 as functions of temperature at frequencies 500 kHz (a) and 1 MHz (b) and for $B_m = 50$ mT

1.5.1 Chokes

Chokes are magnetic elements made of copper wire wound around ferromagnetic cores. The job of a choke designer is to:

- select the core and determine the air gap if required,
- calculate the cross-section, length, and the number of turns of the copper wire, and
- select the mode of winding.

The basic parameter of a choke is its inductance. If the core contains an air gap, then the inductance is approximately

$$L = \frac{\mu_0 \mu_e}{\Sigma l / S} N^2, \quad (1.41)$$

where l is the length of magnetic force lines of each individual part of the core made of the same magnetic material and with a constant cross-section, S is the cross-section of the core, $\mu_0 = 4\pi \times 10^{-7}$ H/m is magnetic permeability of the vacuum, μ_e is the effective magnetic permeability, and N is the number of turns. The effective

permeability is defined as the resulting permeability of a core consisting of materials with different permeabilities. It depends on the shape and dimensions of the core and particularly on the width of the air gap in the magnetic material.

The effective length of magnetic force lines l_e is defined as

$$l_e = \frac{(\Sigma l/S)^2}{\Sigma l/S^2}, \quad (1.42)$$

and the effective magnetic cross-section is

$$S_e = \frac{l_e}{\Sigma l/S}. \quad (1.43)$$

The effective magnetic volume is determined by

$$V_e = l_e S_e. \quad (1.44)$$

Now the choke inductance can be written in the form

$$L = \mu_0 \mu_e \frac{S_e}{l_e} N^2. \quad (1.45)$$

It is quite difficult to determine the effective magnetic permeability of a core containing an air gap. For this reason, the manufacturers give the values of the inductance factor A_L which represents the inductance of the choke consisting of the core and one turn. The inductance of the coil of a choke is

$$L = A_L N^2. \quad (1.46)$$

The inductance factor A_L is determined experimentally by measuring the inductance of a coil containing only one turn and it is presented in the form of a diagram like the one in Fig. 1.14. The inductance factor A_L of ferrite cores ranges from 5 to 10,000. It depends on the type of material and core dimensions. For larger cores, the inductance factor A_L is larger. In addition, A_L is dependent on the air gap of the core (Fig. 1.15).

1.5.2 Transformers

Transformers consist of at least two inductively coupled windings. The windings are galvanically separated, thus only the transfer of AC signals is possible. The input winding is called the primary, and the output is the secondary. Voltage induced in the secondary can be lower, or higher, or equal to the primary voltage. The ratio of the secondary and the primary voltage is determined by the ratio of the number of the secondary and the primary windings. Under the influence of the

Fig. 1.14 Choke inductance as function of the number of turns for different values of inductance factor A_L

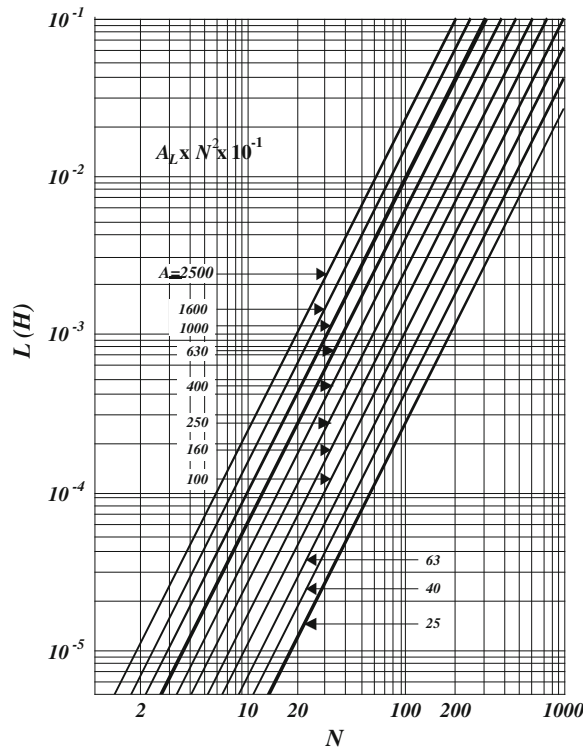
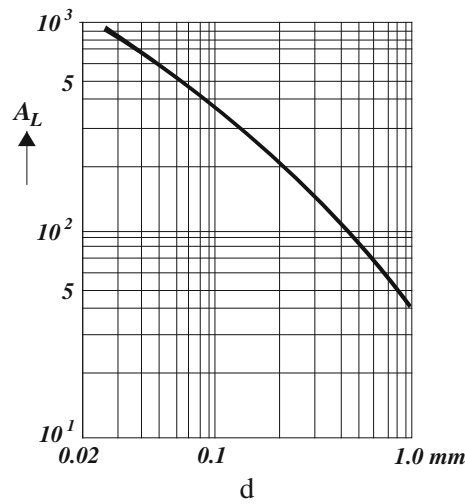


Fig. 1.15 Inductance factor as function of the width of the air gap of ferrite core profile E20 made of material N27 (Siemens)



magnetic flux caused by the voltage V_1 in the primary winding, the electromotive forces E_1 and E_2 will be induced in the primary and the secondary windings, respectively

$$E_1 = 4.44 \times 10^{-4} f N_1 B_m S_e, \text{ (V)}, \quad (1.47)$$

$$E_2 = 4.44 \times 10^{-4} f N_2 B_m S_e, \text{ (V)}, \quad (1.48)$$

where $f(\text{Hz})$ is the driving frequency, N_1 and N_2 are the respective numbers of turns in the primary and in the secondary, $B_m(\text{T})$ is the amplitude of magnetic induction in the core, and $S_e(\text{cm}^2)$ is the effective cross-section of the core. If the voltage drops in the windings are neglected, then $V_1 = E_1$ and $V_2 = E_2$ and the ratio of voltage transformation is

$$n = \frac{V_1}{V_2} = \frac{N_1}{N_2} \quad (1.49)$$

Since the inductance factors of the primary and the secondary are equal, it follows that:

$$n = \frac{V_1}{V_2} = \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}} \quad (1.50)$$

If the secondary is loaded, the current I_2 will flow. The currents of the primary I_1 and the secondary I_2 will maintain magnetic equilibrium if $I_1 N_1 = I_2 N_2$, giving

$$\frac{I_1}{I_2} = \frac{N_2}{N_1} = \frac{1}{n}. \quad (1.51)$$

A real transformer can be replaced by the equivalent circuit in Fig. 1.16 consisting of a T equivalent circuit and an ideal transformer. Real losses within a transformer are modeled by the stray inductance L_e . The coupling coefficient k depends on the degree of coupling of the magnetic fields of the windings. For ferromagnetic transformer cores, k is close to unity because almost all magnetic field lines close within the transformer core. The Ohmic resistances of the

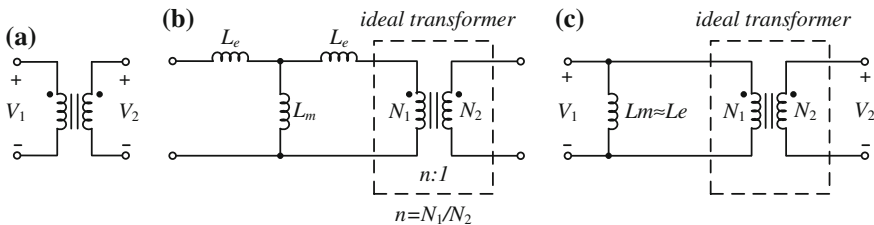


Fig. 1.16 Real transformer (a) and its equivalent circuits (b) and (c) ($L_m = kI_1$, $L_e = L_1 - L_m$)

transformers used in electronics are negligible. Consequently, these transformers can be represented by a parallel connection of a coil, whose inductance is equal to the inductance of the primary winding, and an ideal transformer with a transformation ratio $n = N_1/N_2$ (Fig. 1.16c).

1.6 Capacitors

Capacitors have found a very wide application in power electronics. Typical applications are:

- protection circuits of power switches,
- various types of filters,
- resonant circuits of converters for achieving the conditions of soft commutation of switching elements,
- AC circuits for power factor correction,
- pulse DC/DC converters for DC component separation,
- circuits for forced turning on and off of semiconductor switches (bipolar transistors and thyristors) etc.
- Globally, they can be classified in three groups:
 - ceramic,
 - film and
 - electrolytic.

Figure 1.17 shows the areas of capacitance and the permitted operating voltages for the three groups of capacitors.

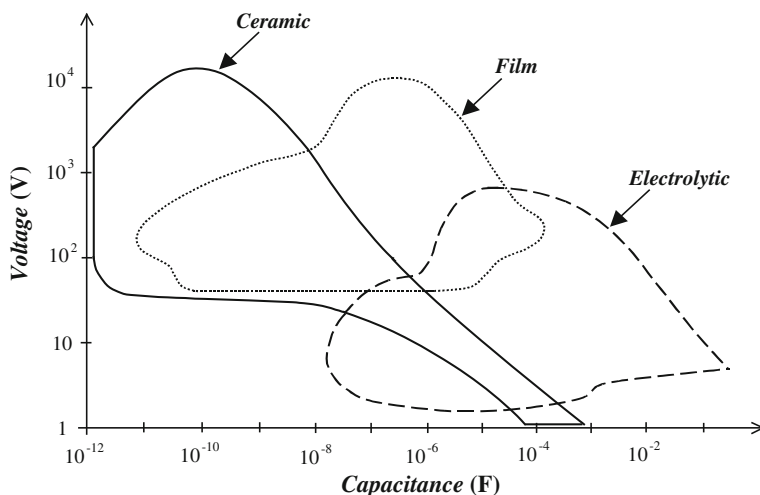
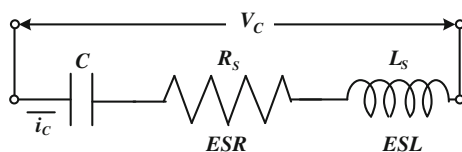


Fig. 1.17 Areas of capacitance and permitted operating voltages

Table 1.6 Relative dielectric constants ϵ_r of standard dielectric materials

Dielectric	ϵ_r
Vacuum	1
Air (atmosphere)	1.00059
Ceramic	20–12,000
Ta ₂ O ₃	10–25
Glass	4–9.5
Al ₂ O ₃	7
Polystyrene and polypropylene	2.5
Polycarbonate	2.8
Impregnated paper	2.6

**Fig. 1.18** Equivalent circuit of capacitor

The basic function of a capacitor is to accumulate electrical energy in the form of electric charge. The electric charge Q and the accumulated energy E_C are determined by

$$Q = CV_C, \quad (1.52)$$

$$E_C = \frac{1}{2} CV_C^2, \quad (1.53)$$

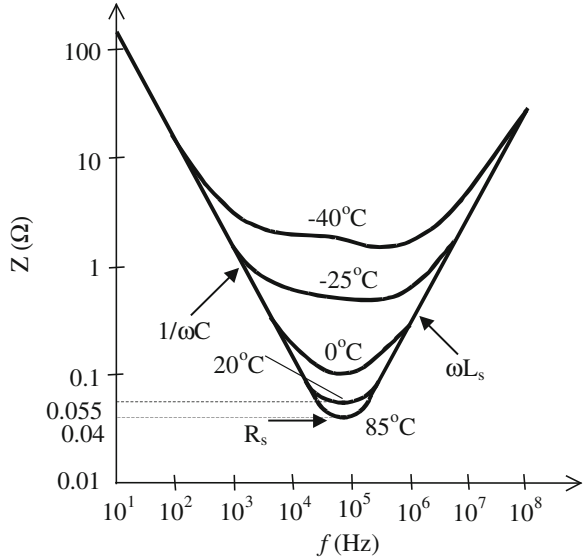
where V_C is the voltage applied to the capacitor and C is its capacitance. The capacitance C is directly proportional to the surface S of the electrodes and inversely proportional to the thickness d of the dielectric layer between them, thus:

$$C = \frac{\epsilon_0 \epsilon_r S}{d}. \quad (1.54)$$

Relative dielectric constants ϵ_r for different materials are shown in Table 1.6.

A capacitor can be represented by the equivalent circuit shown in Fig. 1.18, where $R_s = \text{ESR}$ is the equivalent series resistance and $L_s = \text{ESL}$ the equivalent series inductance. The series resistance is the basic cause of dissipation in a capacitor and it is most often expressed by the power factor $\tan \delta$ defined as

Fig. 1.19 Impedance modulus of aluminum electrolytic capacitor 100 mF/ 63 V as a function of frequency



$$\tan \delta = \omega C R_s. \quad (1.55)$$

The power factor $\tan \delta$ is given in catalogue data for capacitors.

ESL represents the series inductance of the terminals of the internal structure of a capacitor. Besides being dependent on the type of capacitor, the values of the parasitic elements ESR and ESL depend on packaging and method of mounting in a circuit. The total impedance of a capacitor is determined by

$$Z(\omega) = R_s + j \left(\omega L_s - \frac{1}{\omega C} \right), \quad (1.56)$$

and its modulus is shown in Fig. 1.19. The minimum of the impedance modulus is equal to the resistance R_s and it is obtained at the intrinsic resonance frequency

$$\omega_r = \frac{1}{\sqrt{L_s C}}. \quad (1.57)$$

Below this frequency, the impedance is of the capacitive character and the influence of ESL can be neglected. For $\omega > \omega_r$, the influence of ESL prevails.

One electrode of electrolytic capacitors is usually made of aluminum or tantalum. A thin oxide layer serving as dielectric is formed on that electrode. The other electrode is electrolyte in either liquid or solid state. The electrode carrying the dielectric must always be at positive potential. The electrolytic capacitors should have large values of ESR and ESL. This has a negative effect on the properties of the converters where these capacitors are used in the output filters. The ripple of the output voltage is increased and the stability of the control module is decreased

owing to the difficulties in the design of the compensator in the feedback loop. For this reason, it is recommendable to use a parallel connection of several capacitors of lower capacitance instead of one large capacitor. In addition, it is recommendable that a ceramic or film (polypropylene) capacitor of small ESR and ESL is connected in parallel with the electrolytic capacitor. The influence of the parasitic elements of ESR and ESL can be reduced if specially designed four-terminal capacitors are used in the output filter.

Tantalum capacitors have a high-specific capacitance (high capacitance for small dimensions and low values of ESR and ESL). ESR and ESL tantalum chip capacitors have especially low values.

The dielectric of ceramic capacitors is ceramic material. Depending on the composition of the ceramic material, two main classes of ceramic capacitors can be defined. The relative dielectric constant of class I capacitors is below 500 ($\epsilon_r < 500$). The capacitance does not depend on supply voltage. These capacitors have small power losses even at high frequencies ($\tan\delta$ is about 0.15 % at 1 MHz). They are used in resonant circuits, as timing elements, for filtering, etc. The relative dielectric constant of class II capacitors ranges from 1,000 to 10,000. Their capacitance is a nonlinear function of voltage and temperature. They have higher power losses ($\tan\delta$ is about 3 % at 1 MHz) than the class I capacitors. Owing to high values of ϵ_r , the capacitance is relatively high compared to dimensions.

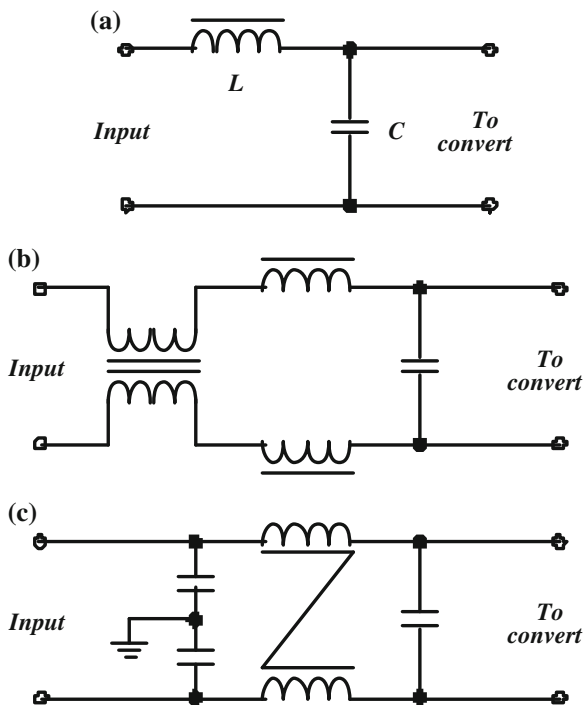
The dielectric of film capacitors is usually a thin film of polypropylene (MKP capacitors) or of polyester (MKT capacitors). Very often, these dielectrics are combined with metallized paper, resulting in improved ability of enduring large voltage pulses. The film capacitors are mainly used in pulse circuits involving very fast voltage variations dv/dt .

1.7 Radio-Frequency Interference

In the instants of the change of state of a power switch, a very large change of voltage and current per unit time (from 10^6 to 10^9 A/s or V/s) is generated. This is the reason that the pulse converters generate interference, both conductive and electromagnetic. Through the input and the output contacts of a converter, conductive interference acts upon the primary source and also upon the load. This may cause erroneous operation of electronic equipment whether it is supplied from the primary source or by a converter.

A converter irradiates electromagnetic interference into the surrounding space. This may hinder the operation of the nearby electronic equipment. For this reason, the removal of radio-frequency interference is one of the key problems in the design of pulse converters. Interference cannot be entirely eliminated, but it can be reduced to within permitted limits. The limits for permitted interference are defined by various national standards and international regulations (among the best known ones is *MIL-STD-461*). The interference, which propagates along cables in the form of high frequency currents, is classified as symmetric (between the supply chords)

Fig. 1.20 Typical filter cells for interference reduction, simple L, C filter (a) and more efficient circuits (b and c)



and nonsymmetric, which closes through the ground. Symmetric interference at the input of a converter, as a consequence of the AC component, appears at the internal impedance of the input capacitor. Nonsymmetric interference at the input is closed, by means of the parasitic capacitance of the circuit or by inductive coupling between some of the parts, through the ground.

Symmetric interference at the output is caused by the AC component of the output current on the internal impedance of the output capacitor. It is for this reason that at the output four-terminal electrolytic capacitors with low series impedance should be used. The circuit of nonsymmetric interference at the output is closed through the load and the ground.

The AC components of the input current, generating interference on the supply lines, can be eliminated or reduced to permitted limits. This is accomplished by inserting a filter between the primary source and the stabilizer, or converter, as shown in Fig. 1.20. The filter shown in Fig. 1.20a attenuates the primary source current created by the stabilizer, which behaves like a pulse load. Considerably, more efficient are the circuits shown in Fig. 1.20b, c. In these cases, "isolation" of the stabilizer from the input and the output lines is accomplished. In this way the stabilizer "floats" in its own oscillations. This is carried out by introducing chokes in both the input and the output lines of the stabilizer. The problems caused by interference are most efficiently solved if interference is taken into consideration throughout the design and production of a converter. In doing so, the parasitic

capacitance can be reduced and the lengths and the surfaces of the loops containing pulse currents can be minimized. In addition, the connection of the converter is of importance, bearing in mind the technical requirements.

1.8 Cooling of Components

The electronic components of power electronics are loaded by significant voltages and currents, which leads to significant dissipation and heating of these components. Consequently, the internal temperatures of the components can be considerably higher than that of the surrounding environment. The excessive heating, particularly of semiconductor components, not only degrades their basic characteristics and cuts their lifetimes, but can also lead to catastrophic failures. To avoid this, a designer must strictly take care of the mode of removing the heat, i.e., of component cooling. The elements for the removal of heat are called heat sinks.

If heating of the components is excessive, cooling is carried out by fans. More often, however, large surfaces of a heat-conducting material are mounted on the components and they collect the heat. Sometimes the chassis of the equipment is used for that purpose. Heat sinks are manufactured as specific components. Most frequently, they are plates or profiled ribs made of aluminum or copper (Fig. 1.21). Profiled ribs are more frequently used since they possess larger surfaces and better drain (radiate) heat. Usually they are black colored to radiate heat better.

High-power components carrying heat sinks should be mounted in such a way that an air stream naturally flows over them. Sometimes cabinets are perforated to enable circulation of air.

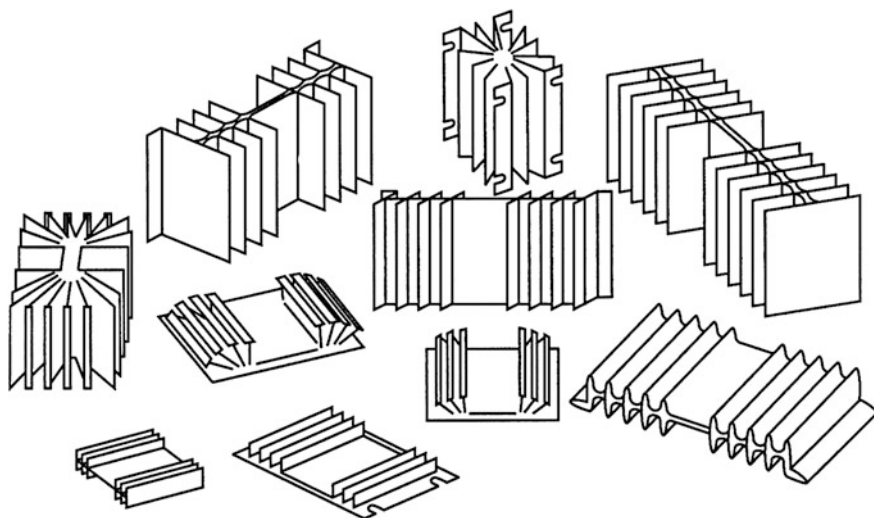


Fig. 1.21 Rib-profiled heat sinks

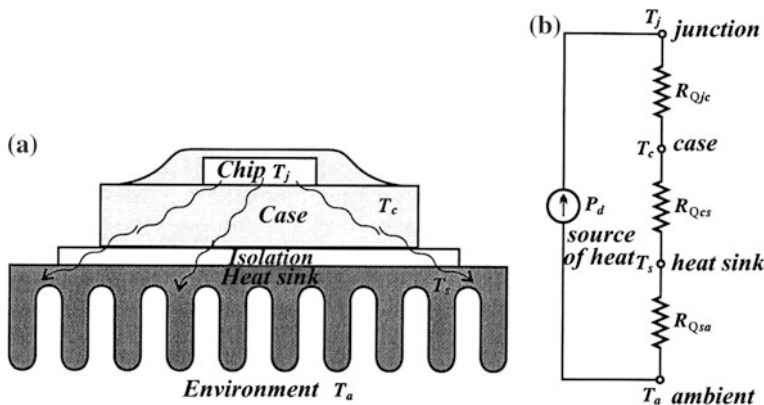


Fig. 1.22 Multi-layer heat transfer from a semiconductor plate (chip) to the environment (a) and thermal equivalent circuit (b)

The component case is mounted directly on the chassis or on the heat sink if an electric contact between them is permitted. For instance, transistors are mounted in this way if the collector is grounded (the collector is connected to the case). If the collector does not have a ground potential, then the case is isolated from the heat sink by a thin insulator layer (Fig. 1.21). Most often it is a thin mica plate which is the electric insulation of the case from the chassis or the heat sink. On the other hand, mica is a good conductor of heat and provides a good transfer of heat from the case to the heat sink.

Power dissipation causes heating of semiconductor devices. The highest temperature is at the junction which carries the highest current density. The maximum permitted temperature of silicon junctions is within the limits of (170–200) °C. However, a majority of manufacturers guarantee the component characteristics given in datasheets up to a silicon junction temperature of 125 °C. The heat at the junction is transferred to the component case and from the case, through the isolation layer, to the heat sink (Fig. 1.22). Within this system, temperature is distributed in such a way that it is the highest in the junction (chip) and drops across the case and the heat sink to the ambient temperature. The distribution is equivalent to the distribution of potentials in an electrical network. Thus, the system for heat removal (component cooling) can be considered through a thermal equivalent circuit (Fig. 1.22b).

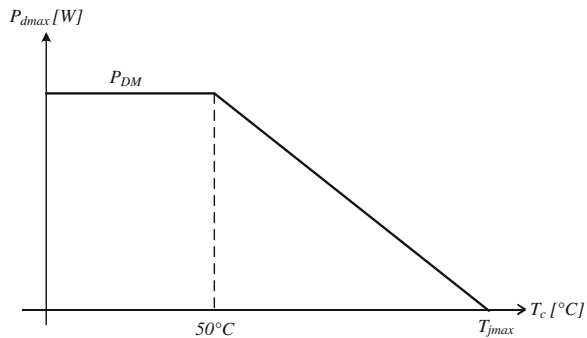
Temperatures are equivalent to potentials. The characteristic temperatures are:

- T_j —p-n junction temperature,
- T_c —case temperature,
- T_s —sink temperature
- T_a —ambient temperature.

The temperature drops across the thermal resistances are:

- R_{jc} —junction-case resistance,

Fig. 1.23 Typical dependence of the permitted maximum dissipation on case temperature T_c



- R_{cs} —case-sink resistance and
- R_{sa} —sink-ambient resistance.

The total resistance between the junction and the ambient is the sum of the previous three resistances, i.e.,

$$R_{ja} = R_{jc} + R_{cs} + R_{sa} = \frac{T_j - T_a}{P_d} \quad (1.58)$$

and is equal to the ratio of the temperature difference junction-ambient and the dissipated power. The thermal resistance is expressed in $^{\circ}C/W$.

The thermal resistance junction-case R_{jc} of transistors and integrated circuits is determined on the basis of the dependence of the maximum permitted power of dissipation P_{dmax} on the case temperature (Fig. 1.23). This characteristic is usually given in datasheets of power components and circuits. The function $P_{dmax} = f(T_c)$ is approximately constant for $T_c < 50^{\circ}C$ and for $T_c > 50^{\circ}C$ it drops linearly. The rate of this drop depends on the type of case. The slope of the curve is determined by the thermal resistance which is defined as:

$$R_{jc} = \frac{T_j - T_c}{P_{dmax}} = \frac{T_{jmax} - 50^{\circ}C}{P_{DM}}. \quad (1.59)$$

At the maximum permitted junction temperature, T_{jmax} , the maximum power dissipation is equal to zero. For instance, for $T_{jmax} = 150^{\circ}C$ and $P_{DM} = 50 W$, the thermal resistance junction-case is

$$R_{jc} = \frac{150 - 50^{\circ}C}{50 W} = 2^{\circ}C/W. \quad (1.60)$$

The thermal resistance indicates the capability for heat removal. A higher resistance means a higher temperature difference between two points in the cooling system. In other words, higher thermal resistance means inferior removal of heat.

Typical values of thermal resistance R_{jc} are within limits from $0.2^{\circ}C/W$ for power transistors up to $1,000^{\circ}C/W$ for low power transistors. These values depend

Table 1.7 Approximate values of junction-case resistance R_{jc} , junction-ambient resistance R_{ja} and power of dissipation P_{dh} for which a heat sink is required at 25 °C

Case	R_{jc} (°C/W)	R_{ja} (°C/W)	P_{dh} (W)
TO-3 metal	3	40	2.80
TO-39 metal	20	120	0.65
TO-202 plastic	7	70	1.56
TO-220 plastic	3	60	1.80

Table 1.8 Orientational values of the resistance between case and heat sink for different insulation materials

Case	Insulation layer	R_{CS} (°C/W)
TO-3	Mica	0.5
TO-3	Beryllium oxide	0.07
TO-220	Silicon jelly	0.6
TO-220	Mica plate and silicon jelly	0.8

Table 1.9 Orientational values of the resistance between heat sink and ambient for several types of heat sinks

Heat sink	Length (mm)	Width (mm)	Height (mm)	R_{sa} (°C/W)
Ribbed	75	120	120	0.9
Ribbed	150	120	120	0.5
Plate of black aluminum	125	125	3	2.5
Plate of black aluminum	175	175	3	1.6

on the type of case (material and component size) (Table 1.7). In order to reduce the thermal resistance R_{jc} the collector of power transistors is often electrically and thermally connected to the case.

If the power dissipation of a semiconductor component is higher than P_{dh} (Table 1.7) a heat sink is required. Otherwise, semiconductor could be damaged or destroyed.

The thermal resistance case-heat sink R_{CS} depends not only on the type of case but also on the insulating material between the case and the sink (Table 1.8).

The thermal resistance heat sink—ambient R_{sa} depends on the shape, size, position and material of the heat sink. Table 1.9 gives orientational values for thermal resistance R_{sa} for several different heat sinks.

The transfer of heat between a sink and the environment is carried out by irradiation and convection. Thermal resistance due to irradiation is given by the Stefan-Boltzmann law

$$P_{\text{rad}} = 5.7 \times 10^{-8} EA(T_s^4 - T_a^4), \quad (1.61)$$

where $P_{\text{rad}}(W)$ is irradiated power, E is emissivity (for black colored aluminum $E = 0.9$), $A(m^2)$ is the external surface, $T_s(K)$ is the sink temperature, and $T_a(K)$ is the ambient temperature. Thermal resistance due to radiation is:

$$R_{sa,\text{rad}} = \frac{\Delta T}{P_{\text{rad}}} = \frac{T_s - T_a}{5.7 \times 10^{-8} EA(T_s^4 - T_a^4)} \quad (1.62)$$

For instance, if $T_s = 120^\circ\text{C} = 393\text{ K}$, $T_a = 20^\circ\text{C} = 293\text{ K}$, and heat sink is made of black oxidized aluminum, then:

$$R_{sa,\text{rad}} = \frac{0.12}{A} \quad (1.63)$$

Power dissipation through convection is determined by [2]

$$P_{\text{conv}} = 1.34 A \frac{(\Delta T)^{1.25}}{d_{\text{vert}}^{1.25}} \quad (1.64)$$

where $A(m^2)$ is the vertical surface, ΔT is the temperature difference between the sink surface and the ambient, and $d_{\text{vert}}(m)$ is the vertical dimension. Thermal resistance due to convection is given by

$$R_{sa,\text{conv}} = \frac{\Delta T}{P_{\text{conv}}} = \frac{1}{1.34} \left(\frac{d_{\text{vert}}}{\Delta T} \right)^{0.25} \quad (1.65)$$

For $d_{\text{vert}} = 10\text{ cm}$ and $\Delta T = T_s - T_a = 100^\circ\text{C}$

$$R_{sa,\text{conv}} = \frac{0.13}{A}. \quad (1.66)$$

Total thermal resistance between a sink and the ambient temperature can be considered as a parallel connection of the radiation and convection resistances, i.e.,

$$R_{sa} = \frac{R_{sa,\text{rad}} \cdot R_{sa,\text{conv}}}{R_{sa,\text{rad}} + R_{sa,\text{conv}}}. \quad (1.67)$$

These are only approximate expressions for calculation of the thermal resistance sink-ambient.

Problems

- 1.1. Calculate the mean and rms value of the current whose waveform is shown in Fig. 1.24.
- 1.2. The voltage and current of a load are periodic function with $T = 10\text{ ms}$. Their functions are described by
Determine:

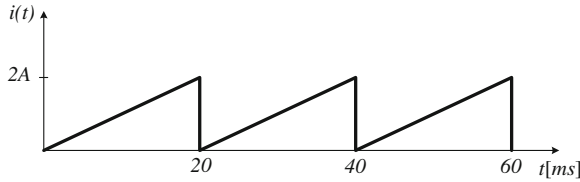


Fig. 1.24 The waveform of the current, saw tooth shape

- (a) the instantaneous power, and
- (b) the average power.

$$v(t) = \begin{cases} 10 \text{ V} & 0 < t < 5 \text{ ms} \\ 0 & 5 \text{ ms} < t < 1 \text{ ms} \end{cases}$$

$$i(t) = \begin{cases} 3 \text{ A} & 0 < t < 6 \text{ ms} \\ -1 \text{ A} & 6 \text{ ms} < t < 10 \text{ ms} \end{cases}$$

- 1.3. A voltage source $v(t) = 100 \cos(2\pi 50 t)$ [V] is applied to a nonlinear load, resulting in nonsinusoidal current: $i(t) = 4 + 10 \cos(2\pi 50 t + 30^\circ) + 20 \cos(4\pi 50 t + 45^\circ)$ [A]. Determine:

- (a) the power absorbed on the load,
- (b) the power factor, and
- (c) the total harmonic distortion of the load current.

- 1.4. Waveforms of voltage and current on a single-phase load are recorded and harmonics are presented in Fig. 1.25a, b. Determine:

- (a) the power absorbed by the load, and
- (b) the power factor.

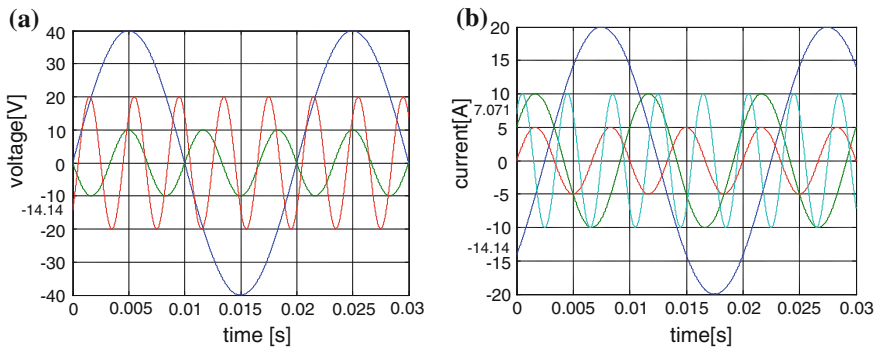


Fig. 1.25 Harmonics of recorded signals on the load **a** voltage, **b** current

- 1.5. Determine total thermal resistance between the sink and the ambient for a semiconductor component if $A = 20 \text{ cm}^2$, $d_{\text{vert}} = 5 \text{ cm}$, $E = 0.8$, $T_s = 125^\circ\text{C}$ and $T_a = 15^\circ\text{C}$.

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2. Mohan, N., et al.: Power Electronic-Converters, Applications and Design. Wiley, New York (1995)

Chapter 2

Diodes and Transistors

In all basic circuits of the pulse DC/DC or DC/AC voltage converters, the switching elements are transistors (bipolar and unipolar) and diodes. In the analysis of a basic circuit, transistors and diodes have been considered as ideal switches (zero on-resistance, infinite off-resistance, and instantaneous transition from one state to the other). However, they are not ideal switches but have real parameters, in both the static and dynamic modes of operation. The influence of these parameters on the characteristics of pulse converters is considerable, particularly on the efficiency factor. For this reason, in this chapter, a description is given of the basic switching characteristics of transistors (bipolar and unipolar) and diodes. An analysis is presented of the modes of control of transistor switches and the optimum control circuits are given. The analysis is of a general character and applies to all pulse assemblies using diodes or transistors as switches.

2.1 Diode as a Switch

The static characteristic of a p-n junction diode is nonlinear and is determined by

$$I_d = I_s \left(e^{V_d/m_d\phi_t} - 1 \right) \quad (2.1)$$

where I_s is the reverse saturation current, m_d is the correction factor ($m_d = 2$ for small currents—in the vicinity of the knee of the characteristic and $m_d = 1$ at higher currents), ϕ_t is the temperature potential. The static characteristic (Fig. 2.1) consists of three regions: conduction region (low-resistance), cut off (high-resistance), and breakdown. The region where the operating point is found depends on the voltage applied to the diode. Therefore, a diode can be used as a switch because its resistance can be controlled by the applied voltage.

When a diode is forward biased and if $V_d > V_{Dt}$, where V_{Dt} is the conduction threshold voltage, the diode is on (conducting). Then its resistance is small (from 10 to 100 Ω). Since the threshold voltage of Si diodes is $V_{Dt} = (0.5\text{--}0.6)$ V, in the conduction region $V_d \gg m\phi_t$, and $\exp(V_d/m_d\phi_t) \gg 1$, so the current is

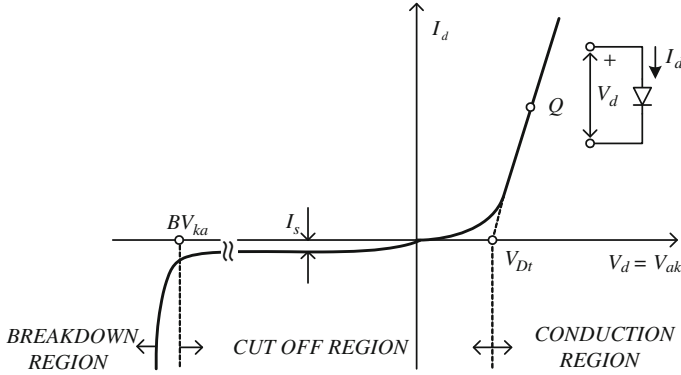


Fig. 2.1 The static diode characteristic

$$I_d \approx I_s e^{V_d / (m_d \phi_t)} \quad (2.2)$$

The dynamic diode resistance is the reciprocal value of the dynamic diode conductance and is defined by

$$r_d = \left. \frac{1}{dI_d/dV_d} \right|_{V_d=\text{const}} = \frac{m_d \phi_t}{I_{DQ}}, \quad (2.3)$$

where I_{DQ} is the diode current at the quiescent operating point Q . Any increase of the diode current I_{DQ} decreases the dynamic resistance. For instance, for $I_{DQ} = 1 \text{ mA}$, $r_d = 26 \Omega$ and for $I_{DQ} = 26 \text{ mA}$, $r_d = 1 \Omega$. It has been assumed that $\phi_t = 26 \text{ mV}$ and $m_d = 1$. It should be emphasized that (2.3) is the p-n junction resistance. The total resistance between the anode and the cathode is increased by the resistance of the base (substrate), which is typically $10\text{--}100 \Omega$, i.e., $R_d = r_d + r_b$. At high currents the resistance r_b is dominant and the V - I characteristic in that region is almost linear.

In many practical applications a conducting diode can be approximated, with a satisfactory accuracy, by a straight line of the slope determined by R_D and a voltage source V_{Dt} (Fig. 2.2a). Then

$$V_d = V_{Dt} + R_D I_D. \quad (2.4)$$

On the other hand, in the majority of diode applications as a switch, the resistance of the driving circuit, which determines the current I_{DQ} in the quiescent operating point Q , is much higher than R_D so that the voltage variation across the diode is negligible. The diode is then replaced by a voltage source V_D and its characteristic is drawn as a straight line that passes through the operating point Q and is orthogonal to the V_D axis (Fig. 2.2b). Typically $V_D = 0.7\text{--}0.8 \text{ V}$ and includes a voltage drop of $0.1\text{--}0.2 \text{ V}$ across R_D .

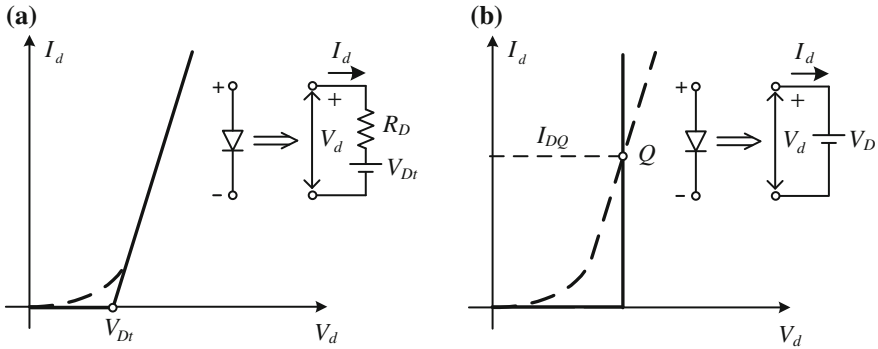


Fig. 2.2 The practical approximations of the V-I characteristic in the conduction region and the corresponding diode equivalent circuits (*dashed line*—real characteristic)

When a diode is reverse biased, i.e., $V_{AK} < 0$, and if $|V_{AK}| > m_d \phi_t$, then $\exp(V_D / m_d \phi_t) \ll 1$ and the current through the diode is equal to the reverse saturation current $I_{DF} = -I_S$. Namely, already at $V_{AK} = -0.2$ V from (2.1) it follows that $I_D = -0.98I_S$. This means that at very small reverse voltages the cathode-anode current is saturated at $-I_S$. The measurements, however, indicate that the reverse current is considerably larger than I_S . This difference is largely due to generation-recombination of charge carriers in the transition region of the p-n junction. At reverse bias, the concentration of charge carriers in the depleted region drops well below the equilibrium concentration. Consequently, recombination is decreased and generation prevails. Owing to the generation of electron-hole pairs a reverse current proportional to the volume of the depleted region Sd and the rate of generation of pairs $G = n_i / (2\tau_0)$ arises, i.e.,

$$I_G = Sq \frac{n_i}{2\tau_0} d, \quad (2.5)$$

where S is the p-n junction area, d is the width of the transition region, n_i is the intrinsic concentration of free charge carriers, τ_0 is the lifetime of carriers in the transition region. It is well known that the width of the transition region increases with increasing the reverse bias, thus causing the increase of the reverse current due to increased generation of the electron-hole pairs:

$$I_G = Sq \frac{n_i}{2\tau_0} d_0 \left(1 - \frac{V_I}{\phi_k}\right)^n, \quad (2.6)$$

where V_I is the reverse voltage, ϕ_k is the contact potential, d_0 is the width of the depletion region at $V_I = 0$, $n = 1/2$ for abrupt and $n = 1/3$ for a p-n junction with a linear distribution of impurities.

The reverse saturation current I_S obtained on the basis of the diffusion theory of the p-n junction is determined by

$$I_s = Sq \left(\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n} \right), \quad (2.7)$$

where D_p , L_p , and D_n , L_n are the respective diffusion coefficients and the diffusion lengths for the holes and electrons, respectively, p_{n0} is the concentration of holes in n -type semiconductor, n_{p0} is the concentration of electrons in p -type semiconductor. In the majority of practical applications the p-n junction is highly asymmetric since the concentration of holes p_{p0} in the p -type region is much higher than the concentration of electrons in the n -type region. Therefore, a p^+n^- junction is the most frequent one. Then, $p_{p0} \gg n_{n0}$ and the hole current in (2.7) is much higher (several orders of magnitude) than the electron current. The reverse saturation current is thus

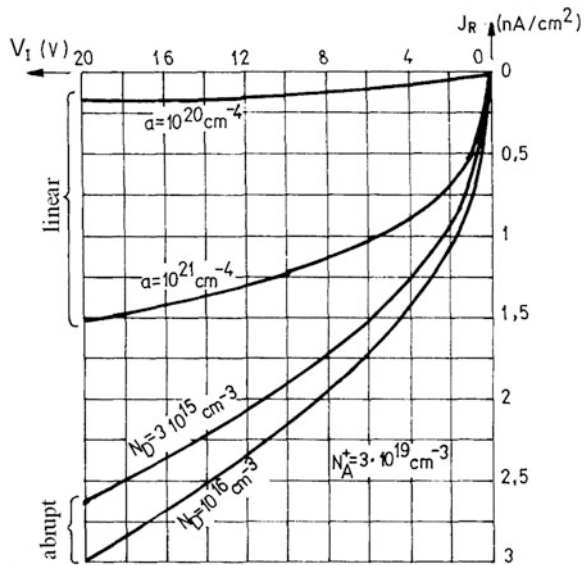
$$I_s \approx I_{sp} = Sq D_p \frac{p_{n0}}{L_p}. \quad (2.8)$$

Applying the relations $p_{p0}n_{n0} = n_i^2$ and $L_p = D_p \tau_0$ one obtains:

$$\frac{I_G}{I_s} = \frac{1}{2} \frac{d}{L_p} \frac{n_{n0}}{n_i}. \quad (2.9)$$

For instance, for a silicon diode with the following parameters: $d = 10^{-4}$ cm, $L_p = 2 \times 10^{-2}$ cm, $n_{n0} = 2.5 \times 10^{15}$ cm $^{-3}$, and $n_i = 1.9 \times 10^{10}$ cm $^{-3}$ the ratio of the reverse generation current I_G to the reverse saturation current I_s is $I_G/I_s \approx 300$. At voltages of approximately 10 volts this ratio may become several thousands. Therefore, the total reverse current of a diode is shown in Fig. 2.3.

Fig. 2.3 Reverse current density versus reverse voltage for linear and abrupt p-n junction



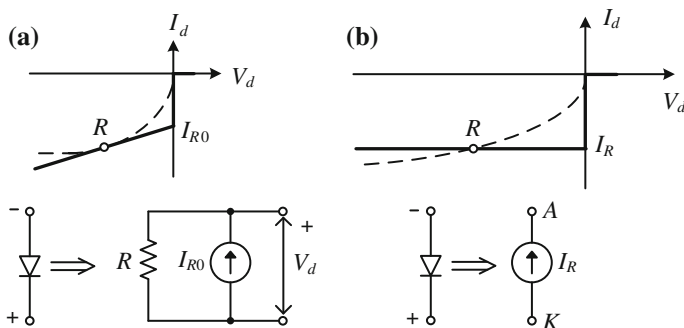


Fig. 2.4 The approximations of V-I characteristic and the corresponding equivalent circuits in the reverse region (*dashed lines*—real characteristics)

$$I_I = I_s + I_G \approx I_G. \quad (2.10)$$

Thus for linear and abrupt junctions the current density characteristic of a diode according to (2.6) is parabolic. In practice, however, the reverse characteristic of a diode is often replaced by a straight line tangential to the operating point R with a segment $-I_{R0}$ on the ordinate (Fig. 2.4a). This means that a diode can be replaced by a parallel connection of a current source I_{R0} and a leakage (reverse) resistance R_I (Fig. 2.4a). Then

$$I_d = -(I_{R0} + V_d/R_I). \quad (2.11)$$

Reverse resistance R_I ranges from several tens k Ω (power diodes) to several hundreds M Ω . The resistance of the driving circuit is usually much lower than R_I , and the change of the reverse current can be neglected. The diode is then replaced by a current source $I_{RR} > I_{R0}$ (Fig. 2.4b) which is specified for a given reverse voltage V_I . The reverse current I_{RR} is usually between 10^{-12} and 10^{-6} A for silicon diodes. Since this current is directly proportional to the surface of the p-n junction, this means that I_{RR} of power diodes is large and can be of the order of mA.

When the reverse voltage is higher than the breakdown voltage of a p-n junction, the diode behaves like a Zener diode if the current is limited. Typical values of the breakdown voltage are between several V up to 100 V. For a high voltage diode this voltage ranges from several 100 V up to several kV.

2.1.1 The Temperature Characteristics

The basic static parameters of a diode as a switch are the reverse current I_R when diode is not conducting and the forward bias voltage V_D when it is conducting. In many applications the temperature sensitivities of these parameters are of

considerable influence on the temperature sensitivities of the functional parameters of the circuits incorporating diodes.

The reverse current is approximated by (2.5). All parameters except n_i are constants independent on temperature, whereas the temperature dependence of n_i^2 is determined by:

$$n_i^2 = AT^3 e^{-V_g/\phi_t}, \quad (2.12)$$

where T is temperature in K, $A = 1.5 \times 10^{32} \text{ cm}^6 \text{ K}^3$, V_g is the bandgap voltage and at room temperature it is 1.11 V. Voltage V_g is also temperature dependent and for silicon it is approximately determined by¹

$$V_g(t) = V_{g0} - 3.6 \times 10^{-4} T, \quad (2.13)$$

where $V_{g0} = 1.21 \text{ V}$ is the bandgap voltage for silicon at absolute zero. The reverse current thus can be written in the form

$$I_R = B T^{3/2} e^{-V_g/(2\phi_t)}, \quad (2.14)$$

where:

$$B = qSA^{1/2} \frac{d}{2\tau_0}. \quad (2.15)$$

After differentiating (2.14) over temperature and rearranging it, the temperature coefficient of the reverse current is obtained as

$$\frac{dI_R}{I_R dT} = \frac{1}{2T} \left(3 + \frac{V_{g0}}{\phi_t} \right). \quad (2.16)$$

At room temperature $T_0 = 300 \text{ K}$, the temperature potential is $\phi = 26 \text{ mV}$, $V_{g0} = 1.21 \text{ V}$ and

$$\left. \frac{dI_R}{I_R dT} \right|_{T_0} = 0.0825 \left[\frac{1}{^\circ\text{C}} \right] \quad (2.17)$$

Very often, however, a more practical expression for $I_R = f(T)$ is used

$$I_R(T) = I_R(T_0) 2^{\frac{T-T_0}{T_x}}, \quad (2.18)$$

where $I_R(T_0)$ is the current I_R at temperature T_0 and T_x is the temperature variation with respect to T_0 , which doubles the value of I_R . T_x can be calculated by equating (2.14) and (2.18) which gives

$$\frac{3}{2} \ln \frac{T}{T_0} + \frac{V_g}{2\varphi_t} \left(\frac{\varphi_t}{\varphi_t(T_0)} - 1 \right) = \frac{T - T_0}{T_x} \ln 2. \quad (2.19)$$

If $(T - T_0)/T_0 \ll 1$ the logarithm of the temperature ratio can be written in the form

$$\ln \frac{T}{T_0} = \ln \left(1 + \frac{T - T_0}{T_x} \right) \approx \frac{T - T_0}{T_x}. \quad (2.20)$$

Since $\varphi_t/\varphi_t(T_0) = T/T_0$, from (2.19) and (2.20) it follows that:

$$T_x = \frac{2 \ln 2}{3 + V_g/\varphi_t} T_0. \quad (2.21)$$

At room temperature ($T = 300$ K) for a silicon diode $T_x = 9$ °C. This would mean that the reverse current doubles for each 9 °C. Here the influence of the reverse saturation current is neglected. It can be shown that its variation with temperature is higher by a factor of 2 (it doubles for each 4.5 °C) since the generation current is proportional to n_i ($I_G \approx I_R \sim n_i$) whereas the injection current is proportional to n_i^2 ($I_S \sim n_i^2$). Due to the influence of the temperature variations of I_S it is accepted in practice that the total reverse current doubles for each 10 °C, i.e.

$$I_R = I_R(T_0) 2^{\frac{T-T_0}{10^\circ\text{C}}}. \quad (2.22)$$

It should be stressed that for small silicon diodes the current $I_R(T_0)$ is quite small and in many applications its temperature variation is of no importance.

The forward bias voltage V_d is also a function of temperature. The case of high currents I_D , when $m_d = 1$, will be considered first. Now the diffusion current compared to the generation-recombination current is dominant and using (2.2), (2.7), and (2.12), taking that $p_{n0} = n_i^2/N_D$ and $n_{p0} = n_i^2/N_A$, one obtains

$$V_d = V_g - \varphi_t \ln \frac{DT^3}{I_D}. \quad (2.23)$$

where D is a temperature independent constant. By differentiating V_d in terms of temperature at a constant current I_D it follows

$$\frac{dV_d}{dT} = \frac{V_d}{T} + \frac{dV_g}{dT} - \frac{\varphi_t}{T} \left(3 + \frac{V_g}{\varphi_t} \right). \quad (2.24)$$

At room temperature for $V_d = 0.7$ V

$$\frac{dV_d}{dT} = \frac{700}{300} - 0.36 - \frac{26}{300} \left(3 + \frac{1110}{26} \right) = -2 \frac{\text{mV}}{^\circ\text{C}}.$$

Therefore, the temperature coefficient of the forward bias voltage is negative. Typically, V_d decreases by 2 mV if the temperature increases by 1 °C. It should be stressed that the expression (2.24) is general because it is also valid for low currents. Then $m_d = 2$ and the generation-recombination current proportional to n_i is dominant instead of I_S , so that

$$V_d = V_g - 2\phi_t \ln \frac{PT^{3/2}}{I_D}, \quad (2.25)$$

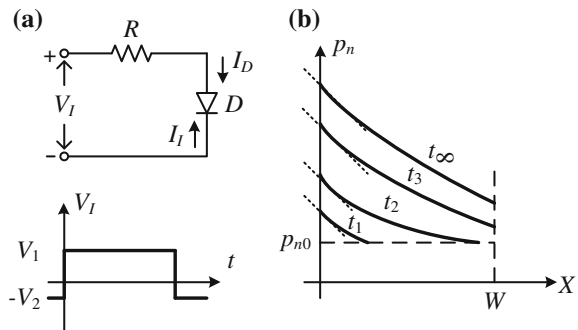
where P is a temperature independent constant. By differentiating (2.25) in terms of T one obtains after rearrangement that at low currents dV_d/dT is determined by (2.24). From (2.24), it is noticeable that the temperature coefficient depends on the position of the operating point. For instance, for $V_D = 0.6$ V, $dV_d/dT = 2.32$ mV/°C and for $V_D = 0.8$ V, $dV_d/dT = 1.66$ mV/°C. In general, it can be said that depending upon the operating regime the temperature coefficient of the forward bias voltage is within the range -1.5 to -2.5 mV/°C.

2.1.2 Dynamic Diode Characteristics

In addition to the static parameters in the switching regime, it is important to know the dynamic response of the diode. The dynamic characteristics of the diode are determined by the transition processes, i.e., the turn-on/turn-off transition times in response to a pulse drive.

Let the diode be driven through a resistance R by a pulse voltage source varying between $-V_2$ and V_1 (Fig. 2.5). The turn-on processes at the instant $t = 0$ will be considered first. For $t < 0$ $V_I = -V_2$ the diode is reverse biased and off. A change of the input voltage at $t = 0$ turns on the diode. If R is much higher than the diode resistance, the current through the diode is

Fig. 2.5 The basic diode switching circuit (a) and distribution of holes in the n -region (b)



$$I_D = \frac{V_1 - V_D}{R} \approx \frac{V_1}{R}, \quad (2.26)$$

because $V_1 \gg V_D$. It is known that the diode current is proportional to the gradient of the injected holes at the edge of the transition region, i.e.,

$$I_D = -qSD_p \frac{dp}{dx} \Big|_{x=0} = \frac{V_1}{R} = \text{const.} \quad (2.27)$$

During the turn-on process, the hole concentration at the edge of the transition region grows from the equilibrium concentration p_{n0} to the concentration determined by the steady state voltage applied across the diode. Since the current through the diode is constant, the change of the hole concentration at the edge of the transition region is also constant (Fig. 2.5b). Practically the steady state is established after a period somewhat longer than the lifetime of the holes, τ_p .

In general, the spatial concentration of holes in the n region during turn-on (Fig. 2.5b) is determined by the diffusion equation:

$$D_p \frac{\partial^2(\Delta p_n)}{\partial x^2} = \frac{\partial(\Delta p_n)}{\partial t} + \frac{\Delta p_n}{\tau_p}, \quad (2.28)$$

where $\Delta p_n = p_n - p_{n0}$ is the excess hole concentration in the n region. The equation governing the excess hole charge can be obtained if Eq. (2.28) is multiplied by $qSdx$ and integrated along the neutral region from $x = 0$ to $x = w$. Therefore:

$$qSD_p \left[\frac{\partial(\Delta p_n)}{\partial x} \Big|_w - \frac{\partial(\Delta p_n)}{\partial x} \Big|_0 \right] = \frac{d}{dt} \int_0^w qS\Delta p_n dx + \frac{1}{\tau_p} \int_0^w eS\Delta p_n dx. \quad (2.29)$$

Since the hole charge is determined by

$$Q_p = \int_0^w qS\Delta p_n dx \quad (2.30)$$

and taking into account (2.27), Eq. (2.29) can be written in the form

$$I_p(0) - I_p(w) = \frac{dQ_p}{dt} + \frac{Q_p}{\tau_p}. \quad (2.31)$$

In the same way, it is possible to derive the equation for the excess electrons in the neutral region. In practice, however, the impurity concentrations of the two sides of the junction are distinctly asymmetric, thus $N_A \gg N_D$, $p_{n0} \gg n_{p0}$ and consequently $Q_p \gg Q_n$. This indicates that the influence of holes on the dynamic process is dominant. Due to this, the index “ p ” in (2.31) can be replaced by “ d ”. Since $I_p(0) - I_p(w) \approx I_p(0) = I_d$ it follows

$$I_d = \frac{dQ_d}{dt} + \frac{Q_d}{\tau_d}. \quad (2.32)$$

This is the charge control equation and it represents the basic relation between the diode current and the excess minority carriers charge in the dynamic operating mode of the diode. In the steady state for a conducting diode $dQ_d/dt = 0$ and $I_d = Q_d/\tau_d$. The injection process is in equilibrium with the recombination process. In other words, a dynamic equilibrium between injection and recombination has been established. The amount of charge in the vicinity of the transition region is constant and proportional to the current through the diode.

At the instant t_0 the input voltage abruptly changes from $+V_1$ to $-V_2$. The diode is reverse biased, but the current through the diode does not drop immediately to the value of the reverse current. On the contrary, for some time the diode conducts with low resistance in the reverse direction (cathode–anode), the current being determined by the external elements. Namely, if $V_d \ll V_2$, the reverse current through the diode is

$$I_1 \approx V_2/R_2 = \text{const.} \quad (2.33)$$

When, at the instant $t = t_0$ the diode is abruptly reverse biased, the direction of the field applied to the p-n junction will change. The direction of the applied field is from the cathode towards the anode and it supports movement of the minority charge carriers. Thanks to this, the excess holes from the n region return to the p region. The direction of the change of the hole concentration at the edge of the junction is altered (Fig. 2.6a). Since the current is constant, the slope of the hole concentration at the edge of the junction is also constant. During this time the piled up charge clears away. A constant reverse current (low diode resistance) will exist as long as the hole concentration at the edge of the junction is greater than zero.

The duration of this phenomenon is called the discharge time, often the accumulation or storage time. It is denoted by t_s . Therefore, during t_s the charge piled up in the vicinity of the p-n junction clears away, i.e., during t_s the diode retains low resistance.

Putting $I_d = I_1$ into Eq. (2.32) and using the initial condition $Q_d(0) = \tau_d I_D$, one obtains that the change of the excess hole charge is

$$Q_d(t) = \tau_d(I_D + I_1)e^{-t/\tau_d} - I_1\tau_d. \quad (2.34)$$

From the condition $Q_d(t_s) = 0$ and (2.34) the storage time is

$$t_s = \tau_d \ln(1 + I_D/I_1). \quad (2.35)$$

Therefore, the storage time is lower if the forward current is lower (Fig. 2.7a), since the stored charge is lower. On the other hand, the storage time is lower if the reverse current is higher (Fig. 2.7b), because the process of clearing away the stored charge is faster.

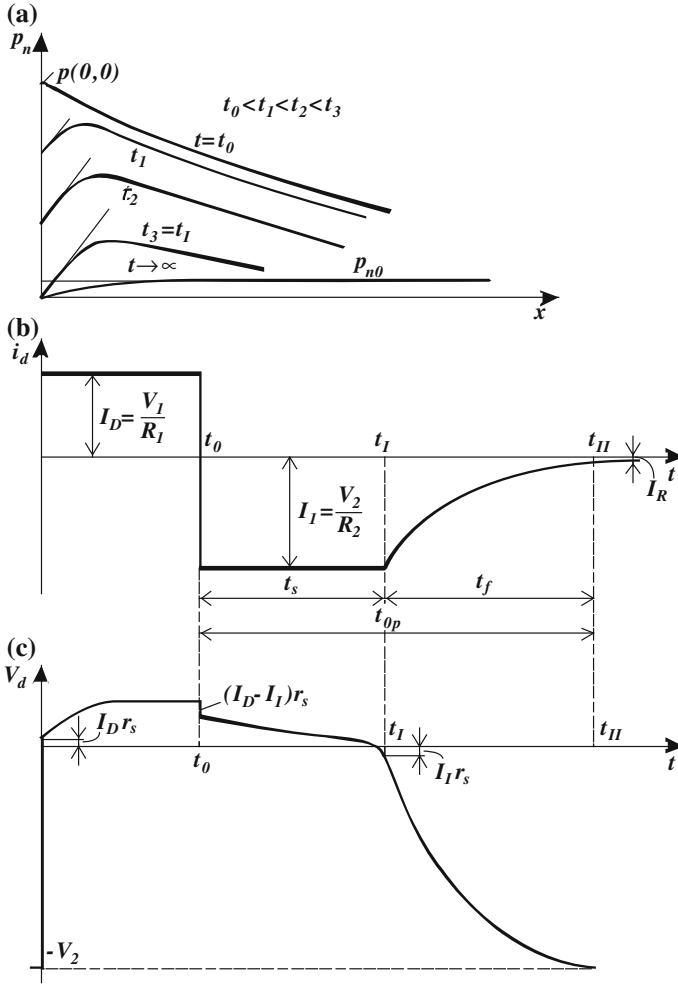


Fig. 2.6 Variation of the hole concentration (a), current (b), and voltage (c) during the turn-off process

Figure 2.6 shows the variations of the current and voltage of a diode in the transient regime. At the instant $t = t_0$ voltage undergoes a negative swing

$$\Delta V = r_s(I_D - I_I). \quad (2.36)$$

Here r_s is the Ohmic resistance of the diode and $I_D - I_I$ is the current swing through the diode at the initial moment. During t_s the voltage across the diode drops to a value $-r_s I_I$. After t_s the diode is obviously reverse biased. The turn-off process continues until the reverse current I_R is attained. The current through the diode reduces and the voltage across it grows more negative. This time is called the fall time and is denoted

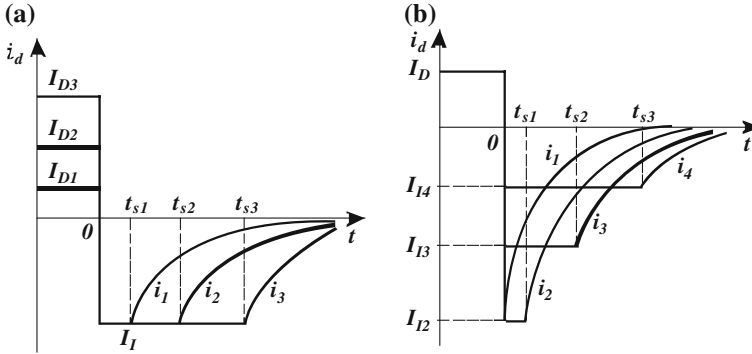


Fig. 2.7 The illustration of the dependence of storage time on forward current for a constant reverse current (a) and on reverse current for a constant forward current (b)

by t_f . Practically, during t_f the capacitor formed by the reverse biased p-n junction is charged. The total turn-off time of the diode $t_s + t_f$ is called the recovery time (denoted by t_r), or sometimes the reverse recovery time (denoted by t_{rr}).

It has been shown that the duration of the transient process is directly proportional to the lifetime of the minority carriers. For this reason in order to reduce τ_p in the n region in fast diodes one introduces the recombination centers, most frequently the atoms of gold. In this way, it is possible to obtain $\tau_p < 1$ ns. Fast diodes, however, have larger reverse saturation currents and lower breakdown voltages. The lifetime of holes in diodes with gold atoms increases with temperature, namely:

$$\tau_p(T) = \tau_p(T_0)(T/T_0)^r, \quad (2.37)$$

where r is a constant; for low injections in silicon it amounts to 3.5 and in germanium 2.2. For instance, for a temperature increase from 213 K (-60°C) to 353 K ($+80^\circ\text{C}$) the average lifetime in silicon increases nearly six times. The duration of the transient process thus largely depends upon temperature.

2.1.3 Schottky Diodes

It is known that the junction of a metal and a weakly doped semiconductor possesses rectifying properties. For instance, at an aluminum— n -type silicon junction, when the donor concentration in silicon is $N_D < 5 \times 10^{18} \text{ cm}^{-3}$, a Schottky barrier is formed and the junction is conductive in one direction and nonconductive in the other. A structure metal— n -type semiconductor with typically $N_D \leq 10^{16} \text{ cm}^{-3}$ makes a Schottky diode.

A Schottky barrier at a metal-semiconductor junction depends upon the type of metal and is within limits 0.58 and 0.85 V. This barrier, similarly to that of a p-n junction, prevents the diffusion of electrons from metal to semiconductor in a

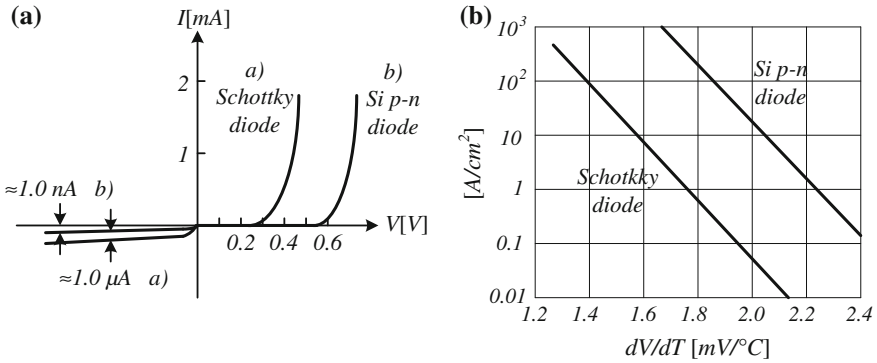


Fig. 2.8 V-I characteristic of Schottky diode (a) and temperature coefficient of forward voltage (b)

nonbiased diode. A positive polarization of the diode (metal is at a higher potential) decreases the potential barrier and electrons from semiconductor cross over to metal. A reverse polarization increases the potential barrier and widens the space charge region which prevents the movement of electrons. The diode is then not conducting. On the semiconductor side the phenomena are identical to those in a p-n junction.

The static V-I characteristic of a Schottky diode is similar to that of a p-n junction diode (Fig. 2.8) and can be written in the form

$$I_d = I_{D0}(e^{V_d/\varphi_t} - 1), \quad (2.38)$$

where the reverse saturation current is

$$I_{D0} = K_{SB} T^2 e^{-\phi_B/\varphi_t}. \quad (2.39)$$

K_{SB} is a constant which is determined experimentally and ϕ_B is the Schottky barrier. The reverse current of a Schottky diode is three to four orders of magnitude higher than the reverse current of a p-n junction diode of the same surface. For a junction with a surface of $S = 100 \mu\text{m}^2$ the reverse current is within the limits $2 \times 10^{-14} \text{ A}$ and 1 nA , depending on the material used.

Except for the difference in the reverse currents the threshold voltages of a Schottky and a p-n junction diodes are quite different. For a Schottky diode this voltage is typically 0.3 V whereas for a Si p-n diode it is approximately 0.6 V . Due to the smaller potential barrier the temperature coefficient of the forward voltage for a Schottky diode is smaller than that of a p-n junction diode (Fig. 2.8b). By neglecting one in the brackets of Eq. (2.38) and having in mind (2.39) it follows

$$\left. \frac{dV_d}{dT} \right|_{\Delta I_d=0} = \frac{V_d}{T} - \frac{\varphi_t}{T} \left(2 + \frac{\phi_B}{\varphi_t} \right). \quad (2.40)$$

For a Schottky diode with aluminum at room temperature $\phi_B = 0.7$ V. If V_D is taken to be 0.4 V, one obtains that $dV_D/dT = -1.2$ mV/°C. The experimentally obtained characteristics for the p-n junction and Schottky diodes (Fig. 2.8b) show that the temperature coefficient of a Schottky diode is smaller by about 0.4 mV/°C.

Schottky diodes are faster. In p-n junction diodes current is carried predominantly by minority carriers. Owing to their accumulation around the junction a delay arises in the turn-off process. In Schottky diodes the electrons are free charge carriers in metal and majority carriers in semiconductor. Current is thus carried by majority carriers and there is no effect of accumulation of minority carriers. Thanks to this Schottky diodes are considerably faster compared to p-n junction diodes. The recovery time of small-signal Schottky diodes is typically less than 0.1 ns.

2.1.4 The Selection of Pulse Diodes

For a good selection of a diode in each specific circuit, it is necessary to know its operation well, the circuit properties and manufacturer's data. These data are usually given in the form of maximum ratings of the static parameters in the forward and the reverse regions and the parameters of the transient state. Usually the following parameters are given at 25 °C:

- the maximum reverse voltage V_I or V_R (this is the maximum negative voltage still not causing the breakdown),
- the maximum reverse current I_R or I_I (this is the current at V_I),
- the maximum forward dc current I_D or I_F ,
- the maximum forward dc voltage V_D at the current I_D ,
- the maximum permitted power P_D (often this information is given instead of I_D or V_D),
- the maximum allowed junction temperature $T_{j\max}$ (this is most often the temperature at which the reverse current is not greater than the given value of I_I . Otherwise, the maximum p-n junction temperature is 90 °C for germanium and 175 °C for silicon diodes),
- the diagram of the permitted forward current versus temperature (Fig. 2.9a) and
- the diagram of the permitted power versus case temperature (Fig. 2.9b).

These data are given for diodes regardless of their purpose. In particular, for pulse diodes, the following additional data are given:

- the maximum forward current I_{DM} , when the current through the diode is pulsed (often the pulse width for a given I_{DM} is specified), and
- the maximum recovery time t_{tr} (usually both the forward and the reverse currents of the transient regime are given for which the specified t_{tr} is guaranteed).

Table 2.1 contains the maximum ratings of the basic parameters for some types of power, low-power, and Schottky diodes.

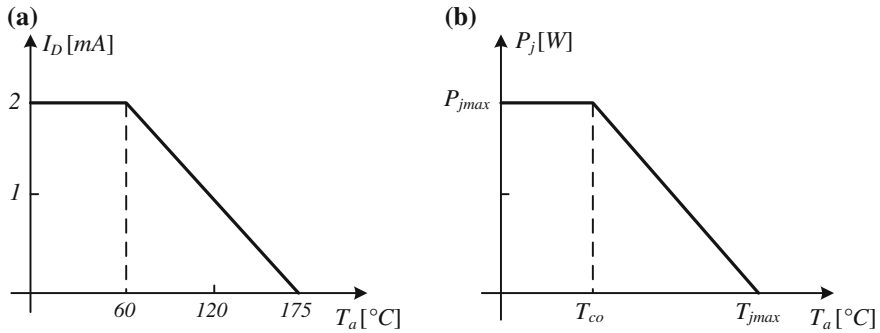


Fig. 2.9 The permitted forward current as a function of the ambient temperature (a) and the permitted junction power as a function of the case temperature (b)

Table 2.1 The basic parameters of different types of diodes

Type	The characteristics at 25 °C						
	I_p [A]	I_{DM} [A]	V_D [V]	I_D [A]	V_I [V]	I_R/V_I [mA]	$t_{rr,max}$ [ns]
Power diodes							
		10 ms	$T_j = 100\text{ °C}$		$T_j = 100\text{ °C}$		$I_D = I_I = 10\text{ mA}$
BYW 77-50	25	500	0.85	20	50	2.5	35
BYW 78-200	50	1500	0.85	50	200	5	60
BYW 08-100	80	1500	0.92	80	100	5	60
BYT 03-400	3	60	1.3	3	400	0.5	2
BYT08P-300A	8	100	1.3	8	300	2.5	2.2
Low power diodes							
		8.3					
1N4149	0.2	0.5	–	–	75	50×10^{-5}	4
1N4151	0.2	0.5	1	0.05	45	50×10^{-5}	2
1N4152	0.2	0.5	0.88	0.02	40	50×10^{-5}	2
1N3070	0.2	0.5	1	0.1	200	100×10^{-5}	5
Schottky diodes							
Bat 17	0.3	–	0.6	10	4	0.25×10^{-3}	<5 ($\tau < 100\text{ ps}$)

The dependence of the forward DC current on the ambient temperature T_a (Fig. 2.9a) shows that for $T_a \leq 60\text{ °C}$ the forward current is constant $I_D = 2\text{ A}$ in the given example. Above this temperature, the permitted forward current drops and for $T_a = T_{jmax}$ it is zero.

The power dissipated in a diode is $P_D = V_D I_D$ and it behaves as a source of heat. Consequently, the diode temperature increases. Thus, the process of self-destruction is possible as the influence of the current temperature coefficient which is positive prevails over the voltage temperature coefficient which is negative. Above the housing temperature T_{c0} the maximum permitted power of the junction decreases (Fig. 2.9b). In the range $T_{c0} < T < T_{j\max}$

$$\frac{T_{j\max} - T_{c0}}{P_{j\max}} = \frac{T_{j\max} - T_c}{P_j}, \quad (2.41)$$

where T_c is the housing temperature, P_j is the permitted, and $P_{j\max}$ is the maximum permitted junction power. From (2.41) it follows:

$$P_j = \frac{T_{j\max} - T_c}{R_{jc}}, \quad (2.42)$$

where

$$R_{jc} = \frac{T_{j\max} - T_{c0}}{P_{j\max}}. \quad (2.43)$$

is the thermal resistance between the junction and the housing. A part of the heat is exchanged between the housing and the ambient. In relation to this, the thermal resistance housing-ambient is defined as the difference between the junction-housing resistance and the total resistance, i.e.,

$$R_{ca} = \frac{T_{j\max} - T_a}{P_j} - R_{jc}. \quad (2.44)$$

The removal of heat is facilitated by mounting the diode on a heat sink. The junction temperature is then

$$T_j = P_j(R_{jc} + R_{ch} + R_{ha}) + T_a, \quad (2.45)$$

where R_{ch} and R_{ha} are the respective resistances housing-heat sink and heat sink-ambient.

2.2 Bipolar Transistor as a Switch

The applications of diodes as switches are quite limited owing to the fact that a diode is a two-terminal device so the control and the controlled circuits are the same. A transistor is a three-terminal device and the control circuit is separated from the load. In accordance with this, it is a standard switching element. In principle, transistors can be connected to a switching circuit in three different configurations:

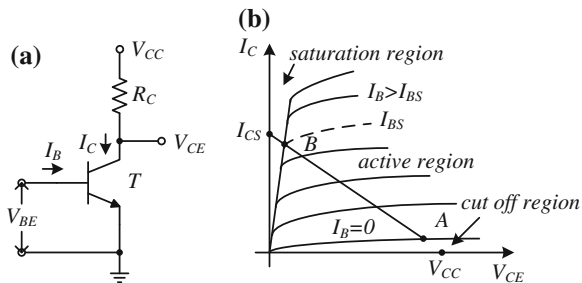


Fig. 2.10 The basic switching circuit (a) and operating regions of transistors (b)

common-emitter, common-base, or common-collector. As a rule, however, transistors are used as switches in the common-emitter configuration. Namely, in this case it is the highest ratio of the load current (collector current) to the input control current (base current), which maintains the on state of the transistor. In other words, this configuration requires the least power for performing control which is the basic requirement for any switch.

In addition to the transistor being used as the switch, the basic switching circuit comprises a load and a power supply (Fig. 2.10a). Depending upon the position of the operating point the transistor will be in one of the three possible regions: saturation, cut off, or active region (Fig. 2.10b). As a switch the transistor is either in saturation or is cut off. The saturation corresponds to the on-state and cut off to the off-state of the switch. These are the static states of the switch. For the analysis of the parameters of the switch use will be made of the Ebers-Moll equations given in the following form

$$I_C = \alpha_N I_E - I_{C0} \left(e^{V_{BC}/(m_c \varphi_t)} - 1 \right), \quad (2.46)$$

$$I_E = \alpha_I I_C + I_{E0} \left(e^{V_{BE}/(m_e \varphi_t)} - 1 \right), \quad (2.47)$$

where α_N and α_I are the respective current gain coefficients of the transistor in the common-base connection for the direct (normal) and reverse modes, I_{C0} is the collector current with the emitter circuit open, I_{E0} is the emitter current with the collector circuit open, m_c and m_e are the respective correction coefficients of the collector and emitter p-n junctions. Like in the case of the diode m_c and m_e are 2 at low currents and 1 at medium currents.

2.2.1 The Cut Off Region

In the cut off region the transistor as a switch is in the off state. It would be ideal if the collector current in this state, i.e., the load current, were equal to zero. In reality,

however, this current does exist. Its value depends on the method the transistors have been switched off. Each of these methods will be analyzed.

1. Both p-n junctions are reverse biased, i.e. $V_{BC} < 0$ and $V_{BE} < 0$

Let $|V_{BC}| \gg m_c \varphi_t$ and $|V_{BE}| \gg m_e \varphi_t$ (these conditions are already fulfilled if V_{BC} and V_{BE} are several 100 mV since $\varphi_t = 26$ mV and $\max\{m_e, m_c\} = 2$). Then:

$$e^{V_{BC}/m_c \varphi_t} \ll 1 \quad \text{and} \quad e^{V_{BE}m_e \varphi_t} \ll 1,$$

and from (2.46) and (2.47) it follows:

$$I_C = \alpha_N I_E + I_{C0} \quad (2.48)$$

$$I_E = \alpha_I I_C - I_{E0}. \quad (2.49)$$

From (2.48) and (2.49), having in mind that

$$\alpha_I I_{C0} = \alpha_N I_{E0} \quad (2.50)$$

one obtains that the collector and the emitter currents, when both junctions are reverse biased, are determined by:

$$I_C = \frac{1 - \alpha_I}{1 - \alpha_I \alpha_N} I_{C0}, \quad (2.51)$$

$$I_E = -\frac{\alpha_I(1 - \alpha_N)}{\alpha_N(1 - \alpha_N \alpha_I)} I_{C0}. \quad (2.52)$$

Typical values of the current coefficients are $\alpha_N = 0.96 - 0.995$ and $\alpha_I = 0.3 - 0.7$. At small currents, these values are several time smaller. Thus, $\alpha_N \alpha_I \ll 1$ and

$$I_c \approx (1 - \alpha_I) I_{C0} < I_{C0}, \quad (2.53)$$

$$I_E \approx -\frac{\alpha_I}{\beta_N} I_{C0}, \quad (2.54)$$

where

$$\beta_N = \frac{\alpha_N}{1 - \alpha_N} \quad (2.55)$$

is the common emitter current gain. The transistor can be replaced by the simplified equivalent circuit (Fig. 2.11a). The negative base current is given by

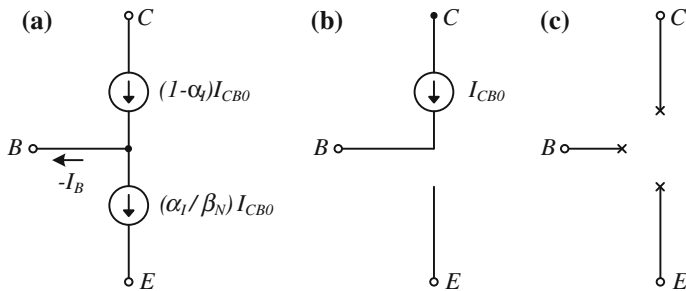


Fig. 2.11 The simplified equivalent circuits of transistor in the cut off region when both junctions are reverse biased

$$I_B \approx -(1 - \alpha_I + \alpha_I / \beta_N) I_{C0}. \quad (2.56)$$

At small currents, β_N ranges from 1 to 5 and $\alpha_I \ll 1$ so that $I_C \approx I_{C0}$, $I_E \approx 0$, and $I_B = -I_{C0}$. The transistor equivalent circuit is shown in Fig. 2.11b. This is, therefore, equivalent to the open emitter. Since $I_C = -I_B$, it is customary that the collector-base current is denoted by I_{CBO} (open emitter collector-base current) and is often called—the reverse base current. It is straightforward to show that $V_{BE} < 0$ when the emitter is open. Namely, by introducing $I_E = 0$ and $I_C = I_{C0}$ in (2.47) one obtains:

$$V_{BEO} = m_e \phi_t \ln(1 - \alpha_N) = -m_e \phi_t \ln(1 + \beta_N). \quad (2.57)$$

For $m_e = 2$ and $\beta_N = 3$, $V_{BEO} = -72$ mV. The current I_{CBO} is temperature dependent and, like the reverse diode current, it doubles with every 10 °C of temperature increase, i.e.

$$I_{CBO}(T) = I_{CBO}(T_0) 2^{\frac{T-T_0}{10^\circ\text{C}}}. \quad (2.58)$$

Usually I_{CBO} at room temperature is of the order of nA and for power transistors of the order of μA . In most practical applications, I_{CBO} can be neglected and the transistor can be considered an open circuit (Fig. 2.11c).

2. The second method of achieving cut off is obtained when: $V_{BE} = 0$ and $V_{BC} < 0$

i.e., when the base and emitter are short circuited and the collector junction is reverse biased. For $|V_{BC}| \gg m_c \phi_t$ from (2.46) and (2.47) it follows:

$$I_C = \frac{I_{C0}}{1 - \alpha_N \alpha_I}, \quad (2.59)$$

$$I_E = \alpha_I I_C = \frac{\alpha_I}{1 - \alpha_N \alpha_I} I_{C0}. \quad (2.60)$$

Since $\alpha_N \alpha_I \ll 1$, then: $I_C \approx I_{C0}$, $I_E \approx \alpha_I I_{C0}$. The base current is $I_B = I_E - I_C = -(1 - \alpha_I) I_{C0}$. Since $\alpha_I \ll 1$, $I_B \approx -I_{C0}$. Therefore, when the base and emitter are short circuited ($V_{BE} = 0$) the currents are approximately as if $V_{BE} < 0$ or the emitter was open, i.e.

$$I_C \approx -I_B = I_{CBO}, I_E \approx 0. \quad (2.61)$$

3. Transistor will be cut off when: $I_B = 0$, $V_{BC} < 0$

i.e., if the base is open and the collector junction is reverse biased. By replacing $I_C = I_E = I_{CEO}$ in (2.46) and since $|V_{BC}| \gg m_e \phi_t$ it follows:

$$I_{CEO} = \frac{I_{C0}}{1 - \alpha_N} = (\beta_N + 1) I_{C0}. \quad (2.62)$$

In this case, the transistor can be replaced by the equivalent circuit of Fig. 2.12. Therefore, if the base is open, the collector current is $\beta_N + 1$ times greater than I_{CBO} . It should be emphasized that β_N at small currents is typically from 1 to 5, and $I_{CEO} = (2-6) I_{CBO}$. The open base voltage $V_{BE} = V_{OBE}$ can be obtained from (2.47) by the replacement $I_E = I_C = I_{CEO}$:

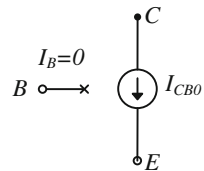
$$V_{OBE} = m_e \phi_t \ln(1 + \beta_N / \beta_I) > 0. \quad (2.63)$$

For instance, for $\beta_N = 3$, $\beta_I = 0.25$ and $m_e = 2$, $V_{OBE} = 133$ mV.

The characteristics of the currents I_C , I_E , I_B versus voltage V_{BE} , for $V_{BC} < 0$ (Fig. 2.13) show that the transistor is cut off when $V_{BE} < V_{OBE}$. In practice it may be assumed that a transistor is cut off if $V_{BE} < V_{BEt}$, where V_{BEt} is the voltage V_{BE} at the knee of the characteristic $I_B = f(V_{BE})$. V_{BEt} is the conduction threshold voltage and for silicon transistors it is typically 0.5–0.6 V.

Very often it is not convenient to realize the cut off state by $V_{BE} < 0$ or $V_{BE} = 0$. The third case ($I_B = 0$) should be avoided since the current I_{CBO} is relatively large and, as will be shown, the voltage limitations of transistors are then the most significant. For this reason the cut off state is often realized by a resistor R between the base and the emitter (Fig. 2.14a). The resistor R is chosen so that $V_{BE} < V_{OBE}$. Then the base current is negative and it is certain that $V_{BE} > 0$. The smaller V_{BE} the

Fig. 2.12 The open base equivalent circuit



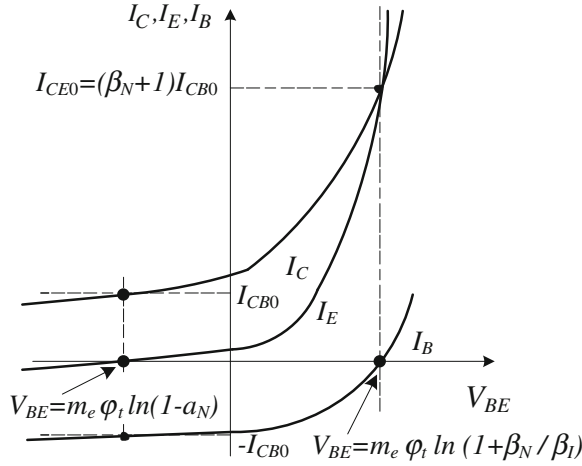


Fig. 2.13 Transistor currents in the cut off region

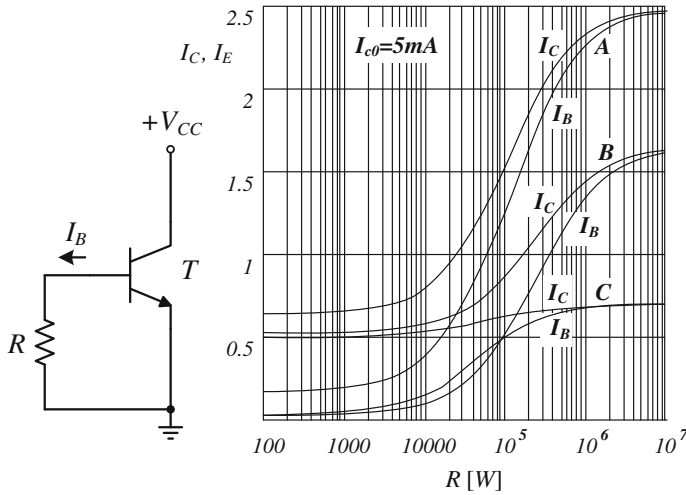


Fig. 2.14 The realization of the cut off state by a resistor (a) and the dependencies of the emitter and collector currents on resistor R for $I_{C0} = 5 \text{ } \mu\text{A}$, (b) with $\alpha_N = 0.8$, $\alpha_I = 0.3$ (A) $\alpha_N = 0.7$, $\alpha_I = 0.1$ (B), and $\alpha_N = 0.3$, $\alpha_I = 0.1$ (C)

smaller collector current. Therefore it is assumed that V_{BE} is approximately zero, i. e. $V_{BE} \ll m_e \phi_t$. Since $|V_{BC}| \gg m_e \phi_t$ the emitter current is:

$$I_E = \alpha_I I_C + I_{EO} \left(e^{V_{BE}/(m_e \phi_t)} - 1 \right) \approx \alpha_I I_C + \frac{I_{EO} V_{BE}}{m_e \phi_t}, \quad (2.64)$$

and the collector current is determined by (2.48). Since

$$V_{BE} = R(I_C - I_E), \quad (2.65)$$

by using (2.64) and (2.48) one obtains:

$$I_C = \frac{\alpha_N m_e \varphi_t + \alpha_I I_{C0} R}{\alpha_N (1 - \alpha_N \alpha_I) m_e \varphi_t + \alpha_I (1 - \alpha_N) I_{C0} R} I_{C0}, \quad (2.66)$$

$$I_E = \alpha_I \frac{\alpha_N m_e \varphi_t + R I_{C0}}{\alpha_N (1 - \alpha_N \alpha_I) m_e \varphi_t + \alpha_I (1 - \alpha_N) I_{C0} R} I_{C0}. \quad (2.67)$$

It is straightforward to show that $V_{BE} = 0$ and $I_B = 0$ are both special cases of the cut off state caused by a resistor between the base and emitter. Namely, from (2.66) and (2.67) it follows that $R = 0$ results in (2.59) and (2.60) and $R \rightarrow \infty$ results in (2.62). On the basis of the variations of collector and emitter currents as functions of R (the R axis is shown in the logarithmic scale) (Fig. 2.14b) it follows that for the resistor R values below several $k\Omega$ the currents I_C and I_E are approximately as if the base and emitter were short circuited. Thus, the practical values of R are within limits from several hundred Ω to several $k\Omega$.

2.2.1.1 The Voltage Limitations

When a transistor is off, the collector junction is always reverse biased and sometimes the emitter junction is reverse biased too. Care must be taken that the reverse voltage is lower than the breakdown voltage. The impurity concentrations in the emitter barrier of diffused transistors are quite high and the emitter-base breakdown voltages are small, typically between 5 and 7 V, rarely 9 V. The reverse voltages of the emitter junction are usually smaller than the breakdown voltage. The reverse voltage of the collector junction is higher. The impurity concentration in the collector barrier is smaller and the breakdown voltage is higher and depends on the connection of the transistor. At high reverse voltages, the process of avalanche multiplication of carriers in the collector barrier appears leading to an abrupt increase of the collector current. In fact, due to the multiplication the parameters α_N and I_{CBO} exhibit sharp increase so the collector current in the common-base connection is expressed by

$$I_C = M \alpha_N I_E + M I_{CBO}, \quad (2.68)$$

where

$$M = \frac{1}{1 - (V_{CB}/BV_{CBO})^n} \quad (2.69)$$

is the multiplication factor. BV_{CBO} is the base-collector breakdown voltage at the open emitter ($I_E = 0$), and n is the parameter depending upon the impurity concentration of the less-doped region. For abrupt and linear p-n junctions n ranges from 2 to 6. If the emitter is open ($I_E = 0$), $I_C = MI_{CBO}$. In the breakdown region $M \rightarrow \infty$ and $I_C \rightarrow \infty$ which is obtained for $V_{CB} = BV_{CBO}$.

When a transistor is in the common-emitter connection, the breakdown phenomena are more complex and the collector current in the breakdown region is:

$$I_C = \frac{M\alpha_N}{1 - M\alpha_N} I_B + \frac{MI_{CBO}}{1 - M\alpha_N}. \quad (2.70)$$

For $I_B = 0$ the breakdown occurs at $M\alpha_N = 1$ resulting in:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta + 1}}. \quad (2.71)$$

Thus, for instance, if $BV_{CBO} = 60$ V, $n = 4$, and $\beta_N = 50$, then $BV_{CEO} = 22.6$ V. Therefore, the breakdown voltage of an open base transistor is several times lower compared to the open emitter situation (Fig. 2.15).

Most often the transistor is cut off by a resistor between the base and emitter (Fig. 2.14a). The base-emitter voltage is then negligibly small and the breakdown voltage of the transistor is equal to the collector-emitter voltage. It is usually denoted by BV_{CER} . By introducing in (2.66) the substitutions $\alpha_N = M\alpha_N$ and $I_{C0} = MI_{C0}$ and from the condition that $I_C \rightarrow \infty$ it follows (Fig. 2.16).

$$BV_{CER} = BV_{CBO} \sqrt[n]{1 - \frac{m\phi_t \alpha_N + RI_{C0}}{m\phi_t \alpha_N + \alpha_t RI_{C0}} \alpha_N \alpha_t}. \quad (2.72)$$

In the limiting cases when $R \rightarrow \infty$ (2.73) transforms into (2.71) and when $R = 0$, $BV_{CER} = BV_{CEK}$ (K -base and emitter short circuited), where

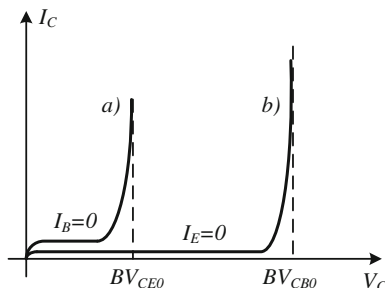
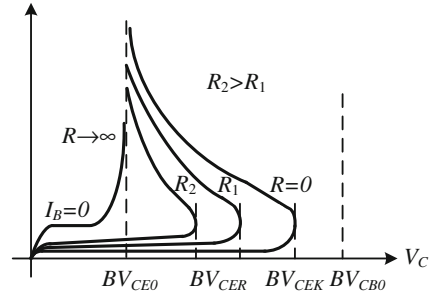


Fig. 2.15 The illustration of the breakdown characteristic of a transistor in common-emitter (a) and common-base (b) connection

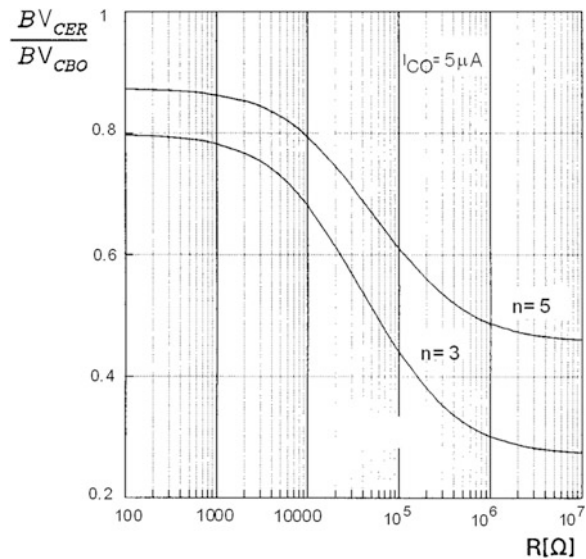
Fig. 2.16 Illustration of the dependence of the breakdown voltage from the resistance R



$$BV_{CEK} = BV_{CBO} \sqrt[n]{1 - \alpha_N \alpha_I}.$$

This expression can also be obtained directly from (2.59). Figure 2.17 shows the normalized voltage BV_{CER} as a function of R , according to (22.72). At small values of R the breakdown voltage is approximately the same as if the base and emitter were short circuited, i.e. $BV_{CER} \approx BV_{CEK}$. Consequently, it may be concluded that the currents and breakdown voltage of a transistor, when the resistor R is within limits from several 100Ω to several $k\Omega$, are nearly the same as if the base and emitter were short circuited (Figs. 2.14 and 2.17). The breakdown voltage is then only 10–20 % lower than the maximum breakdown voltage BV_{CBO} and the collector current is somewhat higher (up to 10 %) than I_{CB0} .

Fig. 2.17 Normalized breakdown voltage as function of R for $I_{C0} = 5\mu A$, $\alpha_N = 0.98$, $\alpha_I = 0.5$, $m = 1.5$ and for $n = 3$ and $n = 5$



Example 2.1 For the switch of Fig. 2.10 determine breakdown voltage in the following cases

- (a) $R \rightarrow \infty$,
- (b) The resistance between the base and the emitter is $R = 20 \text{ k}\Omega$, and $R = 100 \text{ }\Omega$.
The circuit of Fig. 2.10 has: $BV_{\text{CBO}} = 80 \text{ V}$, $\alpha_N = 0.983$, $\alpha_I = 0.1$, $I_{\text{C0}} = 50 \text{ nA}$, $\phi_t = 25 \text{ mV}$ and $n = 4$.

If $R \rightarrow \infty$ base is broken, the collector current is equal to emitter current (I_{CE0}) and using the Ebers-Moll model, the emitter (collector) current is (2.59)

$$I_{\text{CE0}} = \frac{I_{\text{C0}}}{1 - \alpha_N}.$$

In the breakdown region the parameters α_N and I_{C0} are multiplied by a multiplication factor $M = \frac{1}{1 - \left(\frac{BV_{\text{CB}}}{BV_{\text{CBO}}}\right)^n}$, where BV_{CB} is the breakdown voltage of the p-n junction collector–emitter in a general case, and BV_{CBO} is the breakdown voltage of the collector-base p-n junction with the broken emitter. From the breakdown condition $1 - \alpha_N \rightarrow 0$ one obtains (2.71)

$$BV_{\text{CEO}} = \frac{BV_{\text{CBO}}}{\sqrt[n]{\beta_N + 1}} = 28.67 \text{ V}.$$

- (a) If there is a resistor R between the base and the emitter of the transistor, using the Ebers-Moll model of transistor and multiplying in breakdown voltage region coefficients α_N and I_{C0} by the factor of multiplication, the breakdown voltage of p-n junction collector-base (BV_{CER}) is equal to (2.72):

$$BV_{\text{CER}} = BV_{\text{CBO}} \sqrt[n]{1 - \frac{m\phi_t\alpha_N + RI_{\text{C0}}}{m\phi_t\alpha_N + \alpha_I RI_{\text{C0}}} \alpha_N \alpha_I}, \text{ where } m_c = m_e = m.$$

- (b) For $R = 20 \text{ k}\Omega$ is obtained $BV_{\text{CER}} = 75.92 \text{ V}$, and for $R = 100 \text{ }\Omega$ is obtained $BV_{\text{CER}} = 75.96 \text{ V}$.

2.2.2 The Saturation Region

When $V_{\text{BE}} > V_{\text{BEt}}$, the transistor is on and it may be either in the active or in the saturation region. In the active region the collector current is $I_C = \beta I_B + I_{\text{CEO}} \approx \beta I_B$ and:

$$V_{CE} = V_{CC} - \beta R_C I_B. \quad (2.73)$$

(The omission of the index 'N' implies that the normal current gains β and α are considered). Increasing the driving current I_B reduces the V_{CE} voltage down to the limiting value $V_{CE} = V_{CES}$ for $I_B = I_{BS}$ when the operating point is in the position *B* (Fig. 2.10b). If I_B further increases above the value I_{BS} , the collector–emitter voltage and the collector current do not change and are determined by:

$$V_{CE} = V_{CES}, \quad I_{CS} = \frac{V_{CC} - V_{CES}}{R_C} \quad (2.74)$$

It is said then that the transistor is in saturation, since the response (the collector current I_{CS} or the voltage V_{CES} , in saturation) does not change with the excitation (base current). This is because both of the p-n junctions are forward biased and the transistor loses its amplifying ability that it had in the active region owing to the reverse bias of the base–collector junction. A forward bias of the collector junction, i.e.,

$$V_{BC} > V_{BCt} \quad (2.75)$$

is, thus, the condition for the transistor saturation, where V_{BCt} is the conduction threshold of the collector junction. Since $V_{BC} = V_{BE} - V_{CE}$, from (2.73) and (2.75) one obtains that the transistor is in saturation if:

$$I_B \geq \frac{V_{CC} - (V_{BE} - V_{BCt})}{\beta R_C} \quad (2.76)$$

The collector–emitter voltage in saturation is:

$$V_{CES} = V_{BE} - V_{BC}. \quad (2.77)$$

By substitution of (2.77) in (2.76) the saturation condition can be expressed in the following form

$$I_B \geq I_{BS}, \quad (2.78)$$

where

$$I_{BS} = \frac{V_{CC} - V_{CES}}{\beta R_C} = \frac{I_{CS}}{\beta} \quad (2.79)$$

is the base current at the boundary between the active and the saturation region. Because maintaining a transistor in saturation requires a driving current not smaller than I_{BS} , the transistor is usually called a current controlled switch. As a measure of saturation, the factor or degree of transistor saturation is often defined

$$F_s = I_B/I_{BS} = \beta I_B/I_{CS},$$

where I_B is the base current keeping the transistor in saturation. To determine the saturation condition one may use (2.75) or (2.78). It should be emphasized that the condition (2.75) is more general because (2.78) is valid only if the load is not a complex impedance. From (2.77), (2.46), and (2.47) it follows

$$V_{CES} = \varphi_I \ln \frac{\alpha_N [I_B + I_{CS}(1 - \alpha_I)]}{\alpha_I [\alpha_N I_B - I_{CS}(1 - \alpha_N)]}. \quad (2.80)$$

It has been assumed that $m_c = m_e = 1$. For $I_{CS} = 0$ voltage V_{CES} is minimal and determined by

$$V_{CESmin} = V_{CES0} = \varphi_I \ln \frac{1}{\alpha_I}. \quad (2.81)$$

This means that compared to the origin the I_C - V_{CE} characteristics are shifted to the right by the value V_{CES0} (Fig. 2.18). For diffused transistors $0.3 \leq \alpha_I \leq 0.7$, and $9.3 \text{ mV} < V_{CES} < 31.3 \text{ mV}$. These limits should be increased by a factor of 1.2–1.5 because at small currents the correction factor is $m_c > 1$.

The temperature coefficient of the voltage V_{CES} is equal to the difference of the corresponding coefficients of the emitter and the collector diodes, i.e.:

$$\frac{d V_{CES}}{dT} = \frac{d V_{BE}}{dT} - \frac{d V_{BC}}{dT}. \quad (2.82)$$

In view of (2.24)

$$d V_{CES}/dT = V_{BE}/T - V_{BC}/T = V_{CES}/T. \quad (2.83)$$

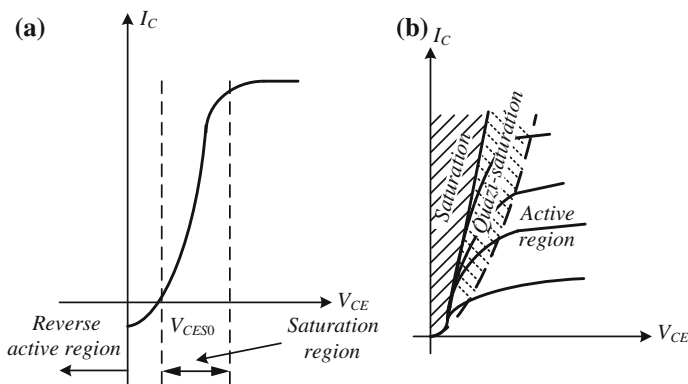


Fig. 2.18 The output characteristics in saturation of a transistor having a small (a) and large (b) collector body resistance

Therefore, the temperature coefficient of the voltage V_{CES} is positive and at room temperature ($T = 300^\circ\text{K}$) it is $dV_{CES}/dT = (0.33 - 0.66) \text{ mV}/^\circ\text{C}$.

The collector–emitter resistance of a transistor in saturation is determined by:

$$r_{ces} = \left. \frac{dV_{CES}}{dI_{CS}} \right|_{I_B=\text{const}} = \frac{\varphi_I}{I_B} \left[\frac{1}{1 + \beta_I + I_{CS}/I_B} + \frac{1}{\beta - I_{CS}/I_B} \right] \quad (2.84)$$

For $\beta_I = 1$, $\beta = 50$, and $I_B = 1 \text{ mA}$ at $I_{CS} = 10 \text{ mA}$, $r_{ces} \approx 2.8 \Omega$ and at $I_{CS} = 40 \text{ mA}$, $r_{ces} \approx 3.2 \Omega$. This resistance should be increased by summing with the resistance of the collector body r_c . The total collector resistance in saturation $r_{cs} = r_{ces} + r_c$ is typically $5\text{--}10 \Omega$ (for low power transistors).

Over the major part of the saturation region the resistance r_{cs} is nearly constant. By approaching the active region (weak saturation), however, the second member in the brackets in (2.84) sharply rises with I_{CS} . At the boundary of the saturation region and the active region $I_{CS}/I_B = \beta$ and $r_{ces} \rightarrow \infty$ which, if the characteristic is ideal, corresponds to resistance r_{ce} of a transistor in the active region. The increase of r_{ces} in weak saturation, particularly for power transistors, is also a consequence of their technological structure. This region is often called the region of quasi-saturation (Fig. 2.18b). Namely, for high voltage power transistors the resistance of the epitaxial layer can be significant. When a transistor is strongly saturated, the collector p-n junction is strongly forward biased and the concentration of charge carriers is very high. The resistance of the epitaxial layer is low and does not influence the characteristics in saturation. In the region of quasi-saturation the collector p-n junction is weakly forward biased and the concentration of charge carriers is reduced which leads to an increase of the resistance. This is particularly characteristic for transistors having a wide epitaxial layer (power and high voltage transistors). In transistors having a narrow epitaxial layer, or having no epitaxial layer, the quasi-saturation region practically does not exist.

A transistor in saturation can be replaced by the collector and emitter diodes (Fig. 2.19a) because both of the p-n junctions are forward biased. The equivalent circuit is shown in Fig. 2.19b. The resistance r_{bs} ranges from several tens Ω up to several hundreds Ω and r_{cs} from several up to 10Ω . Most of the time these

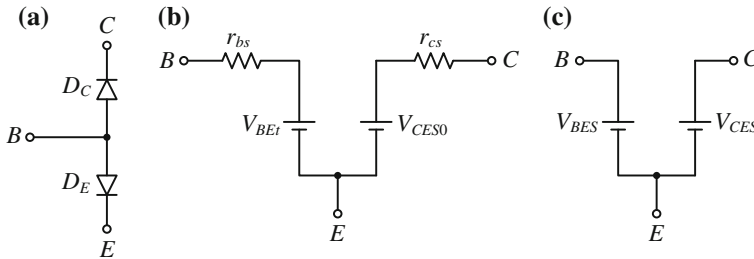


Fig. 2.19 The equivalent circuits of a transistor in saturation

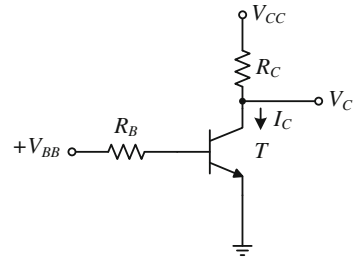
resistances can be neglected and thus the simplified equivalent circuit of a transistor in saturation can be used, as shown in Fig. 2.19c. Typical voltage values are: $V_{BES} = (0.7\text{--}0.8)$ V and $V_{CES} = (0.1\text{--}0.2)$ V.

Example 2.2

- For a switch shown in Fig. 2.20 calculate the collector–emitter voltage when the transistor is in saturation for $R_C \rightarrow \infty$ and $R_C = R_B$.
- Determine the collector–emitter resistance for the transistor in saturation region (r_{CES})

The circuit of Fig. 2.20 has: $R_B = 4.7$ k Ω , $\alpha_N = 0.952$, $\alpha_I = 0.3$, $\phi_t = 25$ mV, $V_{BES} = 0.75$ V and $V_{CC} = V_{BB} = 15$ V.

Fig. 2.20 Simple circuit with the bipolar transistor as a switch



- Based on the Ebers-Moll model, the voltage between the collector and the emitter of a bipolar transistor in the state of saturation (V_{CES}) (2.80) the following expression can be derived:

$$V_{CES} = \phi_t \ln \frac{\alpha_N [I_B + I_{CS}(1 - \alpha_I)]}{\alpha_I [\alpha_N I_B - I_{CS}(1 - \alpha_N)]} = \phi_t \ln \frac{\alpha_N \left[1 + \frac{\beta_N}{F_S}(1 - \alpha_I) \right]}{\alpha_I \left[\alpha_N - \frac{\beta_N}{F_S}(1 - \alpha_N) \right]}, \quad (2.85)$$

where

$$F_S = \frac{I_B}{I_{BS}} = \frac{\beta R_C}{R_B} \frac{V_{BB} - V_{BES}}{V_{CC} - V_{CES}}.$$

For $R_C \rightarrow \infty$, the current $I_{CS} \rightarrow 0$, and on the basis of (2.85) the voltage between the collector and the emitter in the state of saturation is

$$V_{CES} = \phi_t \ln \frac{1}{\alpha_I} = 31 \text{ mV}.$$

For $R_C = R_B$ the factor of transistor saturation $F_S \approx \beta = 20$. Based on expression (2.80), the collector–emitter voltage for a bipolar transistor in the saturation region is $V_{CES} = 44.6$ mV.

- (b) The collector–emitter dynamic resistance for a bipolar transistor in the saturation region r_{CES} is (2.84)

$$r_{CES} = \left. \frac{dV_{CES}}{dI_{CES}} \right|_{I_B = \text{const}} = \frac{\varphi_t}{I_B} \left[\frac{1}{1 + \beta_I + \frac{\beta_N}{F_S}} + \frac{1}{\beta_N - \frac{\beta_N}{F_S}} \right].$$

For $R_C \rightarrow \infty$ the dynamic resistance is

$$r_{CES} = \frac{\varphi_t}{I_B} \left[\frac{1}{1 + \beta_I} + \frac{1}{\beta_N} \right] = 6.18 \, \Omega.$$

For $R_C = R_B$ the collector–emitter resistance is

$$r_{CES} = \frac{\varphi_t}{I_B} \left[\frac{1}{2 + \beta_I} + \frac{1}{\beta_N - 1} \right] = 3.83 \, \Omega.$$

2.2.3 Static Transfer Characteristic

It is customary that the static states of a switching circuit are defined by the voltage transfer characteristic which represents the dependence of the output on the input voltage, i.e. $V_o = f(V_i)$. There are three parts of the characteristic (Fig. 2.20). In the first part $V_i < V_{BEt} \approx 0.5$ V and the transistor is off. In the vicinity of V_{BEt} the transistor is in the region of weak conduction. However, the collector current is still negligible compared to I_{CS} . Let $V_{BE}/(m_e \varphi_t) = 5$. Then, from (2.46) and (2.47)

$$I_C = \frac{1 + \alpha_I e^5}{1 - \alpha_I} I_{CO} \approx \alpha_I e^5 I_{CO}, \quad (2.86)$$

and the output voltage is

$$V_{OH} = V_O(V_{BEt}) = V_{CC} - R_C \alpha_I e^5 I_{CO}. \quad (2.87)$$

Let, e.g. $V_{CC} = 5$ V, $R_C = 1$ k Ω , and $\alpha_I = 0.3$. Then $V_{OH} = V_{CC} - 223 \times 10^{-6} \text{ V} \approx V_{CC}$ for $I_{CO} = 5$ nA and $V_{OH} = V_{CC} - 223 \times 10^{-3} \text{ V} \approx V_{CC}$ for $I_{CO} = 5$ μ A. Thus, the voltage drop across this resistance is negligible compared to V_{CC} . For this

reason, it is taken that for all voltages $V_I < V_{BEt}$ the transistor is off and the output voltage is equal to the supply voltage V_{CC} .

In the second part of the characteristic the transistor is in the active region. According to (2.46), (2.47), and (2.50), the collector current is:

$$I_C = \frac{\alpha_I}{1 - \alpha\alpha_I} I_{C0} e^{\frac{V_I}{m_e \varphi_I}} + \frac{I_{C0}}{1 - \alpha\alpha_I}. \quad (2.88)$$

Since now $\alpha \approx 1$, $\alpha\alpha_I \approx \alpha_I$, the second member in (2.88) is negligible and

$$V_O = V_{CC} - \beta_I I_{C0} R_C e^{\frac{V_I}{m_e \varphi_I}}. \quad (2.89)$$

The output voltage drops quickly with the increase of V_I until the transistor enters the saturation region. The difference

$$\Delta V_I = V_{BESf} - V_{BEt} \quad (2.90)$$

is the transition region width of the transfer characteristic. V_{BESf} is the input voltage for which the transistor is at its boundary between the active and the saturation region. This voltage can be obtained from (2.89) for $V_O = V_{CES}$. This voltage should be increased by the voltage drop across the base resistance r_{bs} . At last one obtains

$$\Delta V_I = \frac{r_{bs} I_{CS}}{\beta} + \varphi_I \ln \frac{I_{CS}}{\beta_I I_{C0}} - V_{BEt}. \quad (2.91)$$

Typically $\Delta V_I = (0.1-0.2)$ V. In general, however, the width of the transition region is defined as the difference between the input voltages for which the voltage gain is -1 , i.e. $dV_O/dV_I = -1$.

The voltage difference between the high and the low output levels is the amplitude of the output voltage, i.e.,

$$V_m = V_{OH} - V_{OL} = V_{CC} - V_{CES} \approx V_{CC}.$$

The input voltage for which the unity gains straight line crosses the transfer characteristic (point T in Fig. 2.21) is called the threshold voltage V_t of the switching circuit. Consequently, here $V_{BEt} < V_t < V_{BESf}$. Owing to the small transition region width ΔV_I it is mainly taken that $V_t \approx V_{BEt}$ and for silicon transistors typically $V_t \approx 0.6$ V. The transfer characteristic (Fig. 2.21) is inverting (low input results in high output and vice versa) and the switching circuit is called an inverter. Since the transistor is a current controlled switch, but the voltage control predominates, a resistor R_B is inserted in the base (Fig. 2.22a).

A realistic inverter circuit, its drive, and the response are shown in Fig. 2.22. The high input level is $V_{IH} = V_{BB1}$. The transistor must then be in the saturation region, i.e.

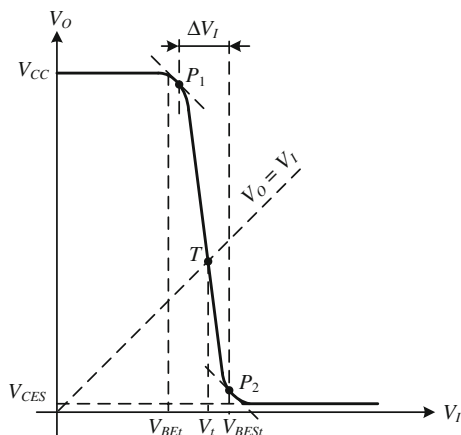


Fig. 2.21 Transfer characteristic

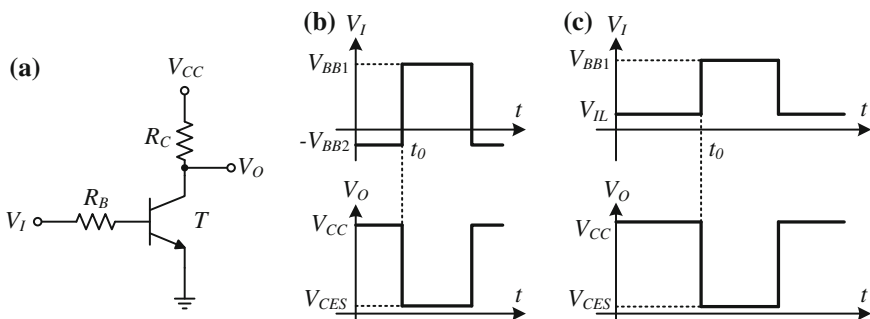


Fig. 2.22 Inverter (a) and idealized pulse waveforms of driving and response voltages (b, c)

$$I_B = \frac{V_{BB1} - V_{BES}}{R_B} \geq I_{BS}. \quad (2.92)$$

From (2.92) and (2.79) it follows:

$$R_B \geq \beta R_C \frac{V_{BB1} - V_{BES}}{V_{CC} - V_{CES}} \quad (2.93)$$

usually $V_{BB1} = V_{CC} \gg V_{BES}$. The current gain β depends on the collector current and temperature (Fig.2.21) and one should perform calculations using its minimum value. Therefore, under the specified operating conditions a transistor will be in saturation if

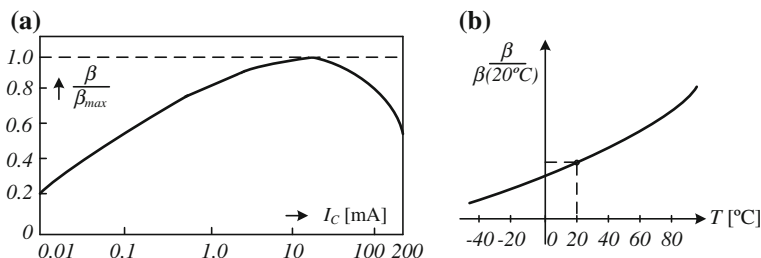


Fig. 2.23 The ratio $\beta/\beta_{\max}$ as function of collector current (a) and temperature (b)

$$R_B \geq \beta_{\min} R_C. \quad (2.94)$$

The temperature characteristic of the current gain β is a growing exponential function (Fig. 2.23b). However, over a wide range of temperatures (-20 to $+60$ °C) it is almost linear and can be approximated by

$$\beta(T) = \beta(T_0) + C_A[1 + \beta(T_0)](T - T_0), \quad (2.95)$$

where T_0 is the room temperature and:

$$C_A = \frac{d\beta}{\beta(T_0)dT} \quad (2.96)$$

is the relative temperature coefficient of the current gain β (it has been assumed that $\beta(T_0) \gg 1$) C_A ranges from 0.1 to 1 % per °C for silicon transistors.

Wherever possible one should try to make the low level input voltage negative (Fig. 2.22b). In practice, however, the input is as shown in Fig. 2.22c, where $V_{IL} < V_{BEt}$ must be satisfied.

2.2.4 Dynamic Inverter Characteristics

The response of an inverter to an abrupt input voltage change is not instantaneous, as shown in Fig. 2.22b, c. In reality, a certain amount of time is always required for the change of the output voltage. In other words, a transistor cannot be instantaneously switched on or off.

It is known that the transistor parameters depend upon the operating frequency. The transient regimes are analyzed at very fast changes of the input voltage, which correspond to very high frequencies. This means that in the analysis of transient regimes the high frequency equivalent circuits and the corresponding parameters should be used. For instance, owing to the influence of the emitter capacitance at high frequencies the common-base current gain is

$$\alpha = \frac{\alpha_0}{1 + j\omega C_e r_e}, \quad (2.97)$$

where α_0 is the low frequency current gain, ω is the circular frequency, C_e and r_e are the respective emitter capacitance and resistance. By putting the time constant

$$C_e r_e = 1/\omega_\alpha \quad (2.98)$$

one obtains

$$\alpha(\omega) = \frac{\alpha_0}{1 + j\omega/\omega_\alpha}. \quad (2.99)$$

Figure 2.24 illustrates the frequency characteristic of the current gain α . At the cut off frequency the gain is, by definition, 3 dB lower, i.e. $\sqrt{2}$ times lower. Thus, ω_α is the circular cut off frequency of a transistor in the common-base connection. The dominant influence on the emitter capacitance, while the transistor is on, is due to the diffusion capacitance. The time constant (2.98) is equal to the base time constant, τ_α . Since the diffusion capacitance is approximately:

$$C_{ed} \approx \frac{W_B^2}{2D_n}, \quad (2.100)$$

then

$$\sigma_\alpha = \frac{1}{\omega_\alpha} \approx \frac{W_B^2}{2D_n}, \quad (2.101)$$

where W_B is the basewidth and D_n is the diffusion constant. Therefore, the narrower the base, the shorter the time constant τ_α , and the higher the cut off frequency ω_α .

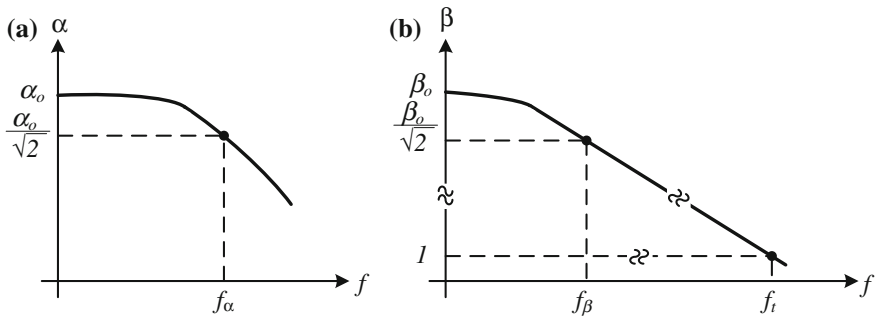


Fig. 2.24 Frequency characteristics $\alpha(\omega)$ (a) and $\beta(\omega)$ (b)

The diffusion constant of electrons in silicon is about 2.5 times higher than that of holes. Thus, an *nnp* transistor under the same conditions possesses about 2.5 times higher cut-off frequency compared to a PNP transistor.

The current gain of a transistor in the common-emitter connection is

$$\beta(\omega) = \frac{\alpha(\omega)}{1 - \alpha(\omega)} = \frac{\beta_0}{1 + j\omega/\omega_\beta}, \quad (2.102)$$

where $\beta_0 = \alpha_0/(1 - \alpha_0)$ is the low frequency signal gain,

$$\omega_\beta = (1 - \alpha_0)\omega_\alpha = \frac{\omega_\alpha}{\beta_0 + 1} \quad (2.103)$$

is the angular cut off frequency of the common-emitter connection, and its time constant is

$$\tau_\beta = 1/\omega_\beta = (\beta_0 + 1)/\omega_\alpha = (\beta_0 + 1)\tau_\alpha. \quad (2.104)$$

The cut off frequency ω_β is thus $\beta_0 + 1$ times lower than ω_α and the time constant is $\beta_0 + 1$ times higher than τ_α . Figure 2.23b shows the *frequency characteristic of the gain β* . The manufacturers often give the unity gain frequency f_T . This is the frequency at which $|\beta(f_T)| = 1$ and f_T is also called the frequency range of the transistor gain. From the condition $|\beta(f_T)| = 1$ and Eq. (2.102) it follows that

$$f_T = \sqrt{\frac{\beta_0 - 1}{\beta_0 + 1}} f_\alpha \approx f_\alpha, \quad (2.105)$$

because $\beta_0 \gg 1$. Typical values for f_T range from several hundreds MHz to several GHz.

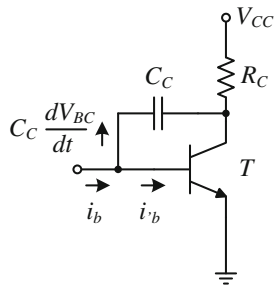
Equations (2.99) and (2.102) can be used for the analysis of the transient modes when the transistor is in the active region. In general, however, a transistor as a switch goes through all regions. For this reason the general charge control method is more suitable for the dynamic analysis of switches. Analogously to diode processes, a change of the charge of minority carriers in the base dQ/dt is caused by the change of the base current, $i_b(t)$, and the recombination of minority carriers in the base $-Q/\tau$, i.e.

$$\frac{dQ}{dt} = i_b(t) - \frac{Q}{\tau}. \quad (2.106)$$

In the active region of a transistor in the common-emitter connection $\tau = \tau_\beta$ and

$$\frac{dQ}{dt} + \frac{Q}{\tau_\beta} = i_b(t). \quad (2.107)$$

Fig. 2.25 Equivalent circuit in the active region



The collector current is proportional to the base charge, i.e.

$$i_c(t) = \frac{\beta}{\tau_\beta} Q(t). \quad (2.108)$$

Equation (2.107) applies for the active region if $R_C = 0$. However, $R_C > 0$ and it does have an influence on the time constant. Namely, in the active region the collector junction is reverse biased and behaves like a capacitor. If the average value of the capacitance of this junction is denoted by C_c , the transistor can be considered as a “pure” transistor plus the capacitor C_c (Fig. 2.25). The current i_b is expressed by (2.107) and

$$i_b(t) = C_c \frac{dV_{BC}}{dt} + \frac{dQ}{dt} + \frac{Q}{\tau_\beta}. \quad (2.109)$$

If the change of the voltage V_{BE} is neglected, then

$$\frac{dV_{BC}}{dt} = -\frac{dV_{CE}}{dt} \approx R_C \frac{di_c}{dt}. \quad (2.110)$$

In view of (2.108), from (2.109) and (2.110) it follows

$$\frac{dQ}{dt} + \frac{Q}{\tau_{\beta_e}} = \frac{\tau_\beta}{\tau_{\beta_e}} i_b(t), \quad (2.111)$$

where

$$\tau_{\beta_e} = \tau_\beta + \beta C_c R_C. \quad (2.112)$$

Thus, the influence of the collector capacitance manifests itself as an increase of the time constant. If a transistor is in the common-base connection, then, according to (2.112) and (2.104)

$$\tau_{ae} = \tau_{\alpha} + C_c R_C. \quad (2.113)$$

The capacitance C_c depends upon the transistor type and usually is within the range from the order of pF to the order of fF . The general solution of (2.111) is given by:

$$Q(t) = e^{-\frac{t}{\tau_{\beta e}}} \left[\int_0^t \frac{\tau_{\beta}}{\tau} i_b(t) e^{\frac{t}{\tau_{\beta e}}} dt + Q(0) \right], \quad (2.114)$$

where $Q(0)$ is the integration constant and represents the charge at the beginning of the analyzed transient process.

2.2.4.1 Transistor Turn On

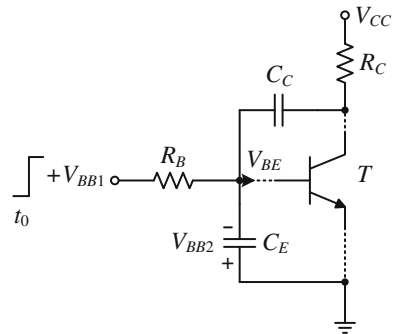
The transient regime of an inverter (Fig. 2.21) caused by an abrupt input drive (Fig. 2.22b) will be considered. Up to the instant t_0 the transistor is off. Both p-n junctions are reverse biased and can be considered capacitors of medium capacitances C_c and C_e . At t_0 the input voltage abruptly changes from $-V_{BB2}$ to $+V_{BB1}$ (Fig. 2.27a). At this instant the transistor turn-on process begins and unfolds in two phases. During the first phase (Fig. 2.27) the capacitor $C_t = C_c + C_e$ must be recharged. The collector current at this instant is zero so that C_c and C_e are practically connected in parallel. At the beginning

$$V_{BE}(t) = V_{BB1} - (V_{BB1} + V_{BB2}) e^{-\frac{t}{C_t R_B}}. \quad (2.115)$$

For $V_{BE}(t_{d1}) = V_{BEt}$ the emitter diode becomes conductive and

$$t_{d1} = C_t R_B \ln \frac{V_{BB1} + V_{BB2}}{V_{BB1} - V_{BEt}} \approx C_t R_B \ln \left(1 + \frac{V_{BB2}}{V_{BB1}} \right). \quad (2.116)$$

Fig. 2.26 Equivalent circuit for delay time t_{d1}



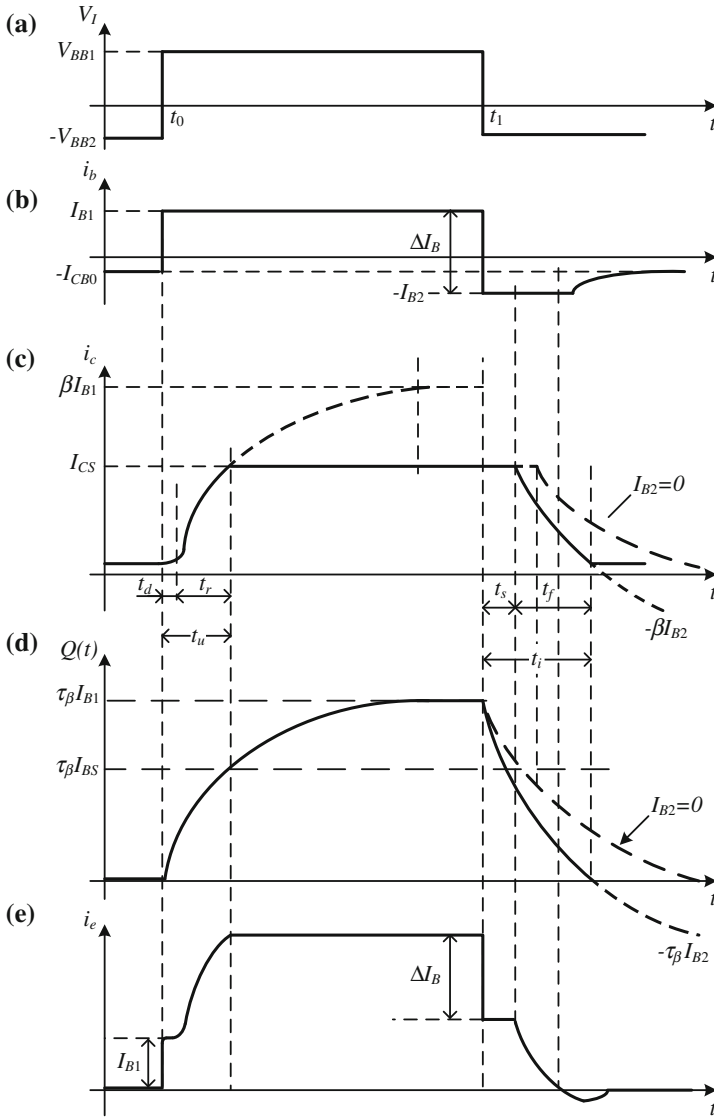


Fig. 2.27 Pulse waveforms of excitation voltage (a), base current (b), collector current (c), base charge (d) and emitter current (e)

After t_{d1} , during $t_{d2} \approx 0.22\tau_a$, the collector current is zero. This delay is the consequence of the finite time required for the transportation of charge carriers through the base. The total delay time of the beginning of the response (collector current or output voltage) is thus

$$t_d = t_{d1} + t_{d2}. \quad (2.117)$$

Usually $t_{d1} \gg t_{d2}$ and $t_d \approx t_{d1}$. After t_d the collector current increases. By introducing in (2.114)

$$i_b(t) = \frac{V_{BB1} - V_{BE}}{R_B} = I_{B1} \quad (2.118)$$

and $Q(0) = 0$, because there are still no excess minority charge carriers, from (2.114) and (2.108) it follows

$$i_c(t) = \beta I_{B1} \left(1 - e^{-\frac{t}{\tau_{\beta e}}} \right). \quad (2.119)$$

The increase of the collector current ends by turning the transistor enters saturation, i.e.

$$i_c(t_r) = I_{CS}. \quad (2.120)$$

From (2.119) and (2.120) the rise time is

$$t_r = \tau_{\beta e} \ln \frac{\beta I_{B1}}{\beta I_{B1} - I_{cs}} = \tau_{\beta e} \ln \frac{I_{B1}}{I_{B1} - I_{BS}}. \quad (2.121)$$

The total turn-on time of the transistor is

$$t_u = t_d + t_r. \quad (2.122)$$

After t_r the collector current is constant (Fig. 2.27c) and the charge in the base increases until a steady state is reached (Fig. 2.27d).

2.2.4.2 Transistor Turn Off

While in saturation, both p-n junctions of the transistor are forward biased. Both the emitter and the collector inject minority carriers into the base. By superimposing the charges of the normal and the reverse active modes the total distribution of charge in the base is obtained (Fig. 2.28a). The shaded part represents the charge in excess compared to the one at the boundary between the active and the saturation states.

The turn-off process of transistor is initiated at the instant $t = t_1$ by a negative change of input from $+V_{BB1}$ to $-V_{BB2}$. As long as the concentration of minority carriers at the emitter-junction boundary is greater than zero a negative base current will flow

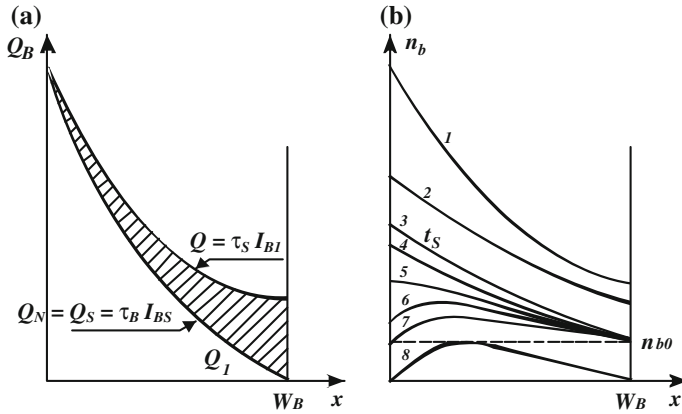


Fig. 2.28 The distributions in base: of the charge in saturation (a) and the concentration of electrons during the turn-off process (b)

$$I_{B2} \approx V_{BB2}/R_B. \quad (2.123)$$

This current “sweeps” the accumulated charge in the base. The turn-off process also unfolds in two phases. During the first phase the collector current remains constant, i.e. $I_C = I_{CS}$ (Fig. 2.27). During that time the excess charge (the shaded part in Fig. 2.28a) which is the consequence of the forward bias of the collector junction is “swept away”. This process lasts as long as the concentration of the minority carriers at the collector junction is greater than zero. The collector current is constant since the slope of the distribution at the end of the base is constant (curves 2 and 3 in Fig. 2.28b). At the end of this interval, which is called the storage time t_s , the concentration of minority carriers at the boundary of the collector junction is zero. Practically, the excess charge has been “swept away” and the transistor “returned” from saturation to the active region.

The change of $Q(t)$ in the base during t_s can be determined from (2.114). For this purpose: $i_b = -I_{B2}$ and the initial charge is $Q(0) = \tau_s I_{B1}$, where τ_s is the time constant of the transistor in saturation. This time constant depends upon time constants in the forward and the reverse modes. Usually $0.5\tau_\beta < \tau_s < 2\tau_\beta$. It is generally taken that $\tau_s \approx \tau_\beta$. During t_s the collector junction is forward biased and $\tau_{pe} \approx \tau_\beta$. Based on this, from (2.114) it follows:

$$Q(t) = -\tau_\beta I_{B2} + \tau_\beta (I_{B1} + I_{B2}) e^{-\frac{t}{\tau_\beta}}. \quad (2.124)$$

From the condition $Q(t) = Q_s = \tau_\beta I_{BS}$ and (2.124) t_s is

$$t_s = \tau_\beta \ln \frac{I_{B1} + I_{B2}}{I_{BS} + I_{B2}}. \quad (2.125)$$

After t_s the collector current decreases. The collector junction is reverse biased and the time constant $\tau_{\beta e}$ is valid. From (2.114) and (2.108) together with the initial condition $Q(0) = Q_s = \tau_{\beta} I_{BS}$ it follows

$$i_c(t) = \beta (I_{B2} + I_{BS}) e^{-t/\tau_{\beta e}} - \beta I_{B2}. \quad (2.126)$$

The turn-off process ends when $i_c(t_f) = 0$ and the fall-off time of the collector current is

$$t_f = \tau_{\beta e} \ln(1 + I_{BS}/I_{B2}). \quad (2.127)$$

The total turn-off time is

$$t_i = t_s + t_f. \quad (2.128)$$

In practice, it is often $V_{BB2} = 0$. This means that the base turn-off current is $I_{B2} = 0$. The process of clearing charge carriers from the base is then slower (dotted lines for the variations of i_c and Q in Fig. 2.27) and is practically due to recombination. The storage time in this case is approximately

$$t_s \approx \tau_{\beta} \ln \frac{I_{B1}}{I_{BS}} = \tau_{\beta} \ln F_s, \quad (2.129)$$

where F_s is the saturation factor. In theory, from the condition $i_c(t_f) = 0$ and for $I_{B2} = 0$, $t_f \rightarrow \infty$. For this reason the condition is $i_c(t_f) = 0.1 I_{CS}$ and

$$t_f \approx 2.3 \tau_{\beta e} = 2.3(\tau_{\beta} + \beta C_C R_C). \quad (2.130)$$

When $V_{BB2} = 0$, the resistance between the base and the emitter should be as small as possible in order to speed up the process of clearing the piled up charge. It should be pointed out that the above analysis is approximate. First of all the base current is not constant throughout the turn-off time. In addition, the time constant of the transistor changes. For $i_c = |I_{B2}|$, the slope of the minority carrier distribution in the base at the junction boundary is zero (curve 5 in Fig. 2.28b). Until then the basewidth is w_B . After that the concentration gradient at the junction boundary changes direction (curve 6 in Fig. 2.28b) and the emitter current becomes negative (Fig. 2.27). At $n_b = n_{b0}$ the effective base width decreases and so does the transistor time constant. All this is very complex for a mathematical description.

A particular attention should be paid to turning off the transistor by a large base current when $|I_{B2}| > I_{CS}$. The minority carrier distribution in the base and the pulse waveforms of the currents for this case are shown in Fig. 2.29. The emitter current is then negative $I_{ES2} = I_{CS} + I_{B2} = I_{CS} - |I_{B2}| < 0$. The minority carrier distribution curves in the base exhibit maxima (curves 2 and 3 in Fig. 2.29a). The minority carrier concentration decreases at both the emitter and the collector junctions. In that case, the equilibrium concentration may be reached at the emitter junction first (Fig. 2.29).

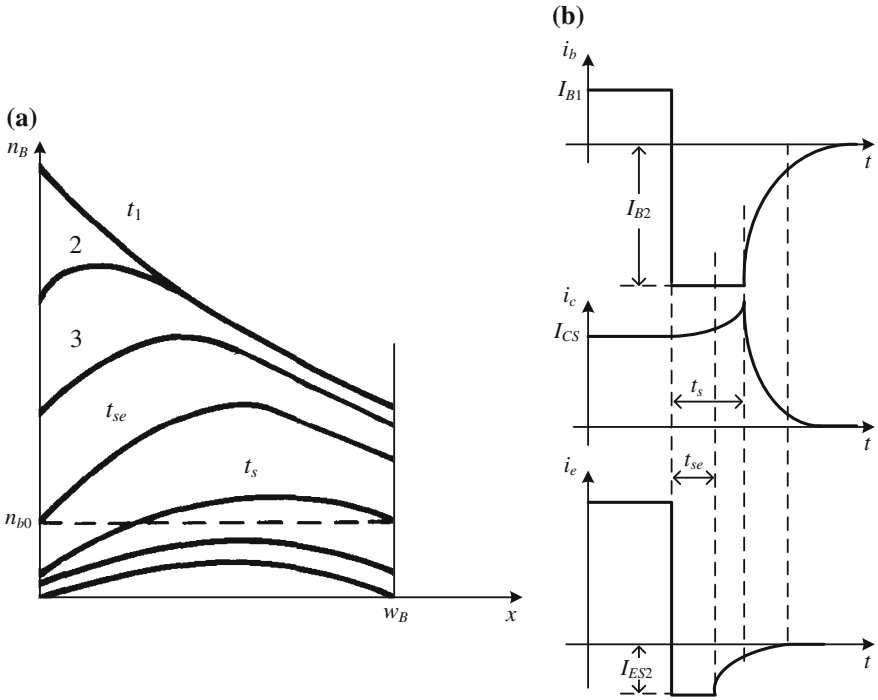


Fig. 2.29 Minority carrier distribution in the base (a) and transistor currents if $I_{B2} > I_{CS}$ (b)

One speaks then about the emitter clearance of the excess charge in the base. Since at t_{se} at the collector junction $n_b > n_{b0}$, the transistor goes to the reverse active mode (the emitter junction reverse biased and the collector junction forward biased). The emitter storage time can be determined from the condition

$$Q(t_{se}) = \frac{\tau_s}{\beta_I} I_{ES2} = \frac{\tau_s}{\beta_I} (I_{B2} - I_{CS}). \quad (2.131)$$

on the basis of (2.124) and (2.131) one obtains

$$t_{se} = \tau_s \ln \frac{I_{B1} + I_{B2}}{I_{B2}/\alpha_I - I_{CS}/\beta_I}. \quad (2.132)$$

The emitter clearance will happen if $t_{se} < t_s$, and from (2.125) and (2.132) it turns out that the base current in that case must be

$$I_{B2} > I_{CS}(1 + \beta_I/\beta). \quad (2.133)$$

After t_{se} the emitter current decreases and the collector current increases (Fig. 2.29b) until the minority carrier concentration at the collector junction equals

the equilibrium concentration. The transistor then goes from the reverse active region to the cut-off region. The currents fall to their steady state values ($I_C \approx I_{CBO}$, $I_B \approx -I_{CBO}$, $I_E \approx 0$). The effective basewidth narrows because both p-n junctions are reverse biased and the transistor time constant is several times smaller than τ_a . This means that the decrease of the currents I_B , I_C , and I_E is very fast.

Example 2.3 For the circuit from Fig. 2.30 and the excitation shown in Fig. 2.31 determine:

- the resistance R_C so the transistor is in saturation with a factor of saturation 5, and
- the transistor turn on (t_{ON}) and the turn off (t_{off}) time.

The circuit of Fig. 2.30 has $R = 2 \text{ k}\Omega$, $\beta_{\min} = 20$, $\tau_\beta = 100 \text{ ns}$, $C_c = 4 \text{ pF}$, $C_e = 10 \text{ pF}$, $V_{BE} = 0.6 \text{ V}$, $V_{BES} = 0.7 \text{ V}$, $V_{BE} = 0.6 \text{ V}$, $V_{CES} = 0.1 \text{ V}$ and $V_{CC} = 12 \text{ V}$.

- The coefficient of saturation is equal to the quotient of the base current that keeps the transistor in the saturation region and the base current of the transistor, which is the boundary between the active and the saturation region:

$$F_S = \frac{I'_{B1}}{I_{BS}}.$$

Fig. 2.30 Bipolar transistor switch

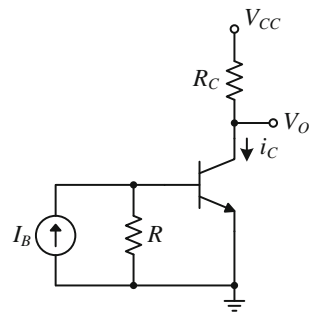
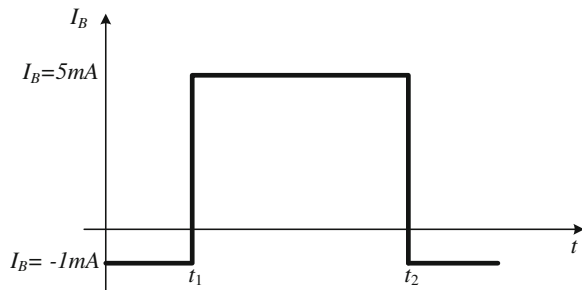


Fig. 2.31 Waveform of current excitation for the circuit shown in Fig. 2.30



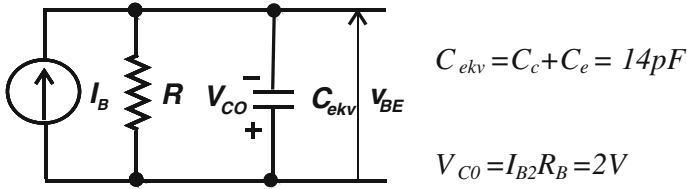


Fig. 2.32 Circuit of charging equivalent input parasitic capacitance while turning on the switch from Fig. 2.30

The base current when the transistor is in the saturation region is (Fig. 2.30)

$$I'_{B1} = I_{B1} - \frac{V_{BES}}{R} = 4.65 \text{ mA}. \quad (2.134)$$

The base current which holds the transistor at the boundary between the active and the saturation region is

$$I_{BS} = \frac{I_{CS}}{\beta} = \frac{V_{CC} - V_{CES}}{\beta R_C}. \quad (2.135)$$

From (2.134), (2.135) and the conditions of the task is obtained that

$$R_C = \frac{F_S(V_{CC} - V_{CES})}{\beta I'_{B1}} = 634 \Omega.$$

(b) The turning on time of the transistor is equal to the sum of t_d and t_r

Interval $t_1 < t < t_1 + t_d$ (time t_d)

To determine the time t_d the equivalent scheme shown in Fig. 2.32 can be used

The voltage between the emitter and the base is equal to (Fig. 2.32)

$$v_{BE}(t) = I_{B1}R - (I_{B1}R + V_{CO})e^{-\frac{t}{\tau_{ekv}}}.$$

From the condition $v_{BE}(t_d) = V_{Bet}$ one obtains

$$t_d = C_{ekv}R \ln \frac{I_{B1}R + V_{CO}}{I_{B1}R - V_{Bet}} = 6.83 \text{ ns}.$$

Interval $t_1 + t_d < t < t_1 + t_d + t_r$ (time t_r)

To determine the time t_r the general charge control method for the dynamic analysis of switches is suitable. Change of the minority carriers concentration in the base dQ/dt is caused by the change of the base current, i_b , and the recombination of minority carriers in the base. The current i_b is constant during this period and approximately equal to

I'_{B1} . In this time interval, the transistor is in the active mode, so the collector p-n junction is reverse biased and the capacitance of the p-n junction has to be taken into account. So, for the determination of the time t_r the following equation is used:

$$\frac{dQ(t)}{dt} = I'_{B1} - \frac{Q(t)}{\tau_{\beta e}}, \quad \text{where} \quad \tau_{\beta e} = \tau_{\beta} + \beta R_C C_C. \quad (2.136)$$

Based on the initial condition $Q(t_1 + t_d) = 0$, the condition for the transistor entering the saturation region $Q(t_1 + t_d + t_r) = \tau_{\beta} I_{BS}$ and on the solution of the Eq. (2.136) the time t_r is calculated as

$$t_r = \tau_{\beta e} \ln \frac{1}{1 - 1/F_S} = 33.4 \text{ ns}.$$

The turning on time of the transistor is equal to: $t_{ON} = t_d + t_r = 40.23 \text{ ns}$.

The turning off time of the transistor t_{OFF} is equal to the sum of t_s and t_f .

Interval $t_2 < t < t_2 + t_s$ (time t_s)

In this interval, the transistor is in saturation, both p-n junctions are forward biased and Eq. (2.106) can be applied. The initial condition is $Q(t_2) = \tau_{\beta} I'_{B1}$, and a prerequisite for the end of this interval is that the transistor is at the boundary between the saturation and active region $Q(t_2 + t_s) = \tau_{\beta} I_{BS}$. By solving Eq. (2.106) with the above mentioned conditions one obtains

$$t_s = \tau_{\beta} \ln \frac{I'_{B1} - I'_{B2}}{I_{BS} - I'_{B2}} = 149.2 \text{ ns}, \quad \text{where} \quad I'_{B2} = I_{B2} + V_{BES}/R.$$

Interval $t_2 + t_s < t < t_2 + t_s + t_f$ (time t_f)

At the beginning of this interval, the transistor is at the boundary between the saturation and the active region. The initial condition is $Q(t_2 + t_s) = \tau_{\beta} I'_{B1}$, and the prerequisite for the end of this interval is that the transistor is turned off $Q(t_2 + t_s + t_f) = 0$. By solving the equations

$$\frac{dQ(t)}{dt} = I'_{B2} - \frac{Q(t)}{\tau_{\beta e}}.$$

with the above conditions one obtains

$$t_f = \tau_{\beta e} \ln \frac{I'_{B2} + I_{BS}}{I'_{B2}} = 130 \text{ ns}.$$

The turning off time of the transistor is $t_{OFF} = t_s + t_f = 279.2 \text{ ns}$.

2.2.4.3 Optimum Drive

It has been shown that the times t_r , t_s , and t_f are dependent on the base currents I_{B1} and I_{B2} . The rise time can be written in the form

$$t_r = -\tau_{\beta e} \ln(1 - I_{BS}/I_{B1}). \quad (2.137)$$

The lower the ratio I_{BS}/I_{B1} the smaller t_r . If $I_{B1} \gg I_{BS}$, (2.137) can be expanded to a Maclaurin series and since it is known that $\ln(1 - x) \approx -x$ for $x \ll 1$, one obtains

$$t_r \approx \tau_{\beta e} I_{BS}/I_{B1} = (\tau_a + C_c R_C) I_{CS}/I_{B1}. \quad (2.138)$$

A small ratio $I_{BS}/I_{B1} = I_{CS}/\beta I_{B1} = 1/F_S \ll 1$ can be accomplished either by a small current I_{CS} or by a large current I_{B1} .

The condition $I_{B1} \gg I_{BS}$ for a small t_r means strong saturation of the transistor ($F_S \gg 1$) which implies a long storage time t_s . On the other hand, from (2.126) it follows that $t_s = 0$ for $I_{B1} = I_{BS}$, i.e., if the transistor is at the boundary between the active and the saturation region. In that case, however, $t_r \rightarrow \infty$. Therefore, the requirements for small t_r and t_s are mutually contradictory. The compromise is the drive shown in Fig. 2.33. While the transistor is being driven on, the base current is $I_B = I_{B1} \gg I_{BS}$, and upon reaching saturation it drops to $I_B = I_{BS}$ (Fig. 2.33). According to (2.127) the larger I_{B2} , the shorter t_f . Therefore, the optimum waveform of the base current is as shown in Fig. 2.33. If $I_{B2} \gg I_{BS}$, then, upon expansion of (2.127) to a Maclaurin series, it is approximately

$$t_f \approx (\tau_a + C_c R_C) I_{CS}/I_{B2}. \quad (2.139)$$

Both t_r and t_s are smaller if I_{BS} or I_{CS} are smaller. This current can be made smaller by increasing the resistance R_C . This, however, helps decreasing t_r and t_f only for small values of R_C (Fig. 2.34) when $C_c R_C \ll \tau_a$. If $C_c R_C \ll \tau_a$, times t_r and

Fig. 2.33 Optimum waveform of base current

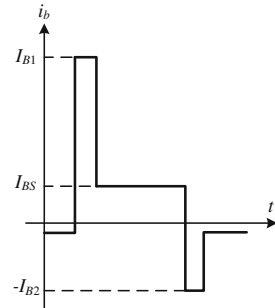
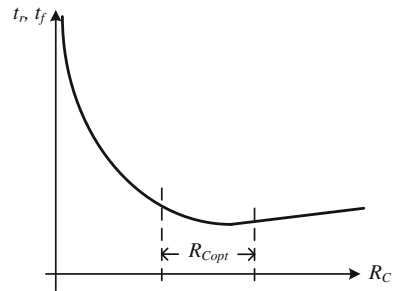


Fig. 2.34 Rise time and fall time as functions of collector load



t_f are almost independent of R_C . In practice, R_C is usually within several hundreds Ω to several $k\Omega$.

2.2.4.4 Speed Up Capacitor

In practice, the base current shown in Fig. 2.33 can only approximately be realized. One of the possibilities is the application of a speed up capacitor (Fig. 2.35a). Usually, R_1 is the internal resistance of the drive and

$$R_1 \ll R_B. \quad (2.140)$$

The variations of the base and the collector current are shown in Fig. 2.36b. The capacitor is a short circuit for abrupt changes and

$$i_b(0) = I_{B1} = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1}. \quad (2.141)$$

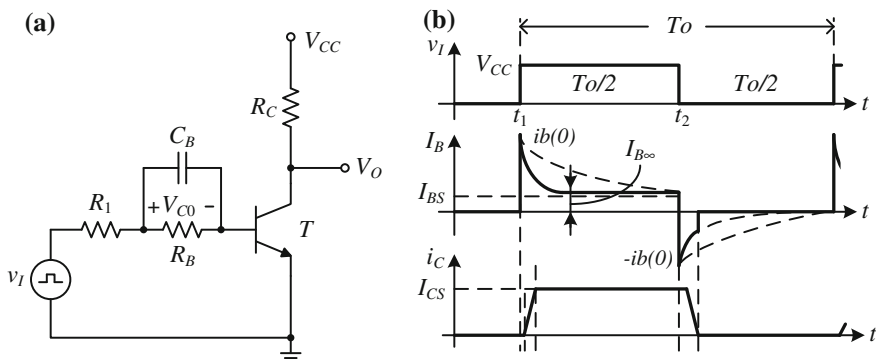
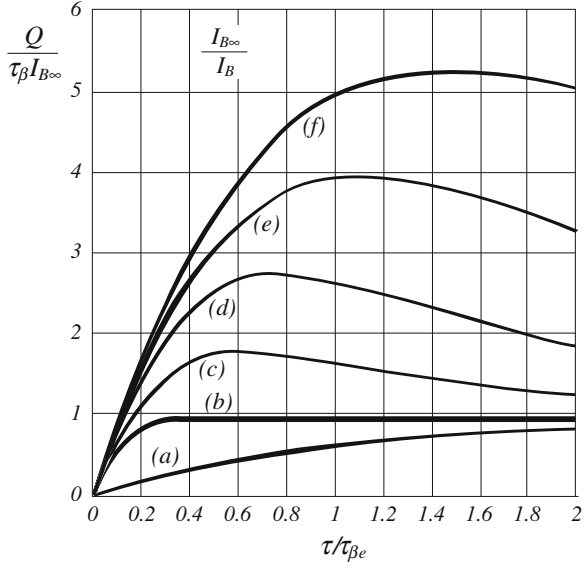


Fig. 2.35 Basic switching circuit comprising a speed up capacitor (a) and the pulse waveforms of the base and collector currents for a pulse drive (b)

Fig. 2.36 Relative base charge as function of time and the ratio $\tau/\tau_{\beta e}$: 0 (a); I_B/I_{B1} (b); 1 (c); 10 (d); 100 (e) with $I_B/I_{B1} = 0.1$



Usually, $R_1 < R_C$, so $i_b(0) \gg I_{BS}$, and according to (2.138)

$$t_r \approx (\tau_\alpha + C_c R_C) R_1 / R_C. \quad (2.142)$$

While the input pulse is on, the capacitor becomes charged and the base current is:

$$i_b = I_{B\infty} = \frac{V_{CC} - V_{BES}}{R_B + R_1} \approx \frac{V_{CC}}{R_B}. \quad (2.143)$$

If $I_B = I_{BS}$, at the instant t_2 the transistor will be at the boundary of the saturation region. However, R_B is usually calculated assuming that the transistor is weakly saturated. Thus

$$R_B = (1.2/1.5)\beta R_C. \quad (2.144)$$

In this way, it is ensured that the transistor is saturated even for the worst case of tolerances of β and R_C . At the instant t_2 the capacitor C_B ensures a negative base current. Since during the previous interval it has been charged to $V_{CO} \approx V_{CC} - V_{BES} \approx V_C$, in the direction marked in Fig. 2.35a, the initial negative base current is approximately given by (2.141). Namely, during the process of clearing the base charge the base-emitter resistance can be neglected. Since the transistor is weakly saturated, the storage time is negligible and the fall time is, according to (2.139), approximately equal to the rise time t_r (2.142). Owing to the capacitor C_B a negative base current is ensured for the fast turning off of the transistor even when $V_{BB} = 0$.

The capacitance of C_B can be determined on the basis of the following two criteria:

- the shortest possible times t_r and t_f and
- the highest possible frequency of the switching circuit.

For the first criterion, the cycle of the triggering pulses, T_0 , from the input generator is known in advance, with $T_0 \gg t_u + t_i$. The capacitance C_B is then determined from the condition that during $T_0/2$ the capacitor is charged while $V_I = V_{CC}$, and discharged while $V_I = 0$. The charging time constant $\tau = C_B(R_1 \parallel R_B) \approx C_B R_1$ is much lower than the discharging time constant. Namely, during the turn-off process, while the piled up base charge is being cleared away, the base-emitter resistance is small and the discharging time constant is $\tau_2 = \tau_1 \approx C_B R_1$. After t_i the base-emitter resistance is very high and the capacitor discharges only through R_B . Since $t_i \ll \tau_1 \ll C_B R_B$ it may be considered that $\tau_2 \approx C_B R_B$ throughout $T_0/2$, while $V_i = 0$. If it is assumed that the duration of the discharging time is five time constants, then from the condition $5C_B R_B < T_0/2$ it follows that

$$C_B < 0.1 \frac{T_0}{R_B}. \quad (2.145)$$

The variation of the base current is represented in Fig. 2.35 by the dotted line. During the transient mode of the transistor, the base current is changed a little compared to the optimum (Fig. 2.33).

Criterion of the Maximum Frequency

$$F_{0\max} = \frac{1}{T_{0\min}} = \frac{1}{t_u + t_i} \quad (2.146)$$

is considerably more general. It is used when the operating frequency of the switching is known in advance. During a positive input pulse, the base current is

$$i_b(t) = I_{B\infty} + (I_{B1} + I_{B\infty})e^{-t/\tau}, \quad (2.147)$$

where I_B and $I_{B\infty}$ are determined, respectively by (2.141) and (2.143) and

$$\tau = C_B \frac{R_B R_1}{R_B + R_1} \approx C_B R_1. \quad (2.148)$$

On the basis of (2.113) and (2.143), the relative base charge is determined by:

$$\frac{Q(t)}{\tau_\beta} = I_{B\infty} + \frac{\tau}{\tau - \tau_{\beta e}} (I_{B1} - I_{B\infty}) e^{-t/\tau} - \left[I_{B\infty} + \frac{\tau}{\tau - \tau_{\beta e}} (I_{B1} - I_{B\infty}) \right] e^{-t/\tau_{\beta e}}. \quad (2.149)$$

This function is represented in Fig. 2.36 for different ratios $\tau/\tau_{\beta e}$. Without the capacitor C_B ($\tau = 0$, curve *a*) the steady state charge $Q_\infty = \tau_\beta I_{B\infty}$ is established exponentially. The rise time in this case is by far the largest. If

$$\tau = \tau_k \geq \frac{I_{B\infty}}{I_{B1}} \tau_{\beta e}. \quad (2.150)$$

then the increase of $Q(t)$ to its steady state value is very fast. For $\tau > \tau_k$, $Q(t)$ exhibits a maximum (curves *c*, *d*, *e*). If the storage time t_s should be minimal, the positive input pulse must be present until a steady state in the base ($Q_\infty = \tau_\beta I_{B\infty}$) is established. From that point of view, the optimum is $\tau = \tau_k$ (curve *b* in Fig. 2.36). According to this, and bearing in mind (2.141) and (2.143) the optimum capacitance is

$$C_{\text{Bopt}} = \tau_{\beta e} / R_B. \quad (2.151)$$

It is said then that the compensation of the charges in the base and the capacitor is achieved. If it is assumed that after a steady state in the base is established the transistor is in weak saturation, i.e., $R_B \approx \beta R_C$, then, bearing in mind (2.112)

$$C_{\text{Bopt}} = C_c + \tau_\alpha / R_C. \quad (2.152)$$

It may be concluded that in the case $\tau \gg \tau_k$ (curves *d* and *e*) the storage time t_s can be very large if condition $T_0 > t_r$ is not satisfied. Thus, C_B according to (2.152) is the optimum value with respect to the maximum frequency of the switch.

2.2.5 Nonsaturated Switch

Another type of the switching circuit comprising an optimum drive is shown in Fig. 2.37a. The diode *D* keeps the base-collector voltage at the value $V_{BC} = V_D$ when the transistor is on. If $V_D < V_{BCr}$, where V_{BCr} is the threshold voltage of the collector p-n junction, then the transistor will be in the active region. A majority of the circuits of this type uses Schottky diodes because $V_{DS} \approx 0.4 \text{ V} < V_{BCr}$. This diode keeps the transistor in the active region, but close to saturation since

$$V_{oL} = V_{BE} - V_D = 0.7 - 0.4 = 0.3 \text{ V} \approx V_{CES},$$

thus these circuits are often called the circuits based on the nonsaturated switch circuits. On the other hand, when the diode becomes conductive, it activates the

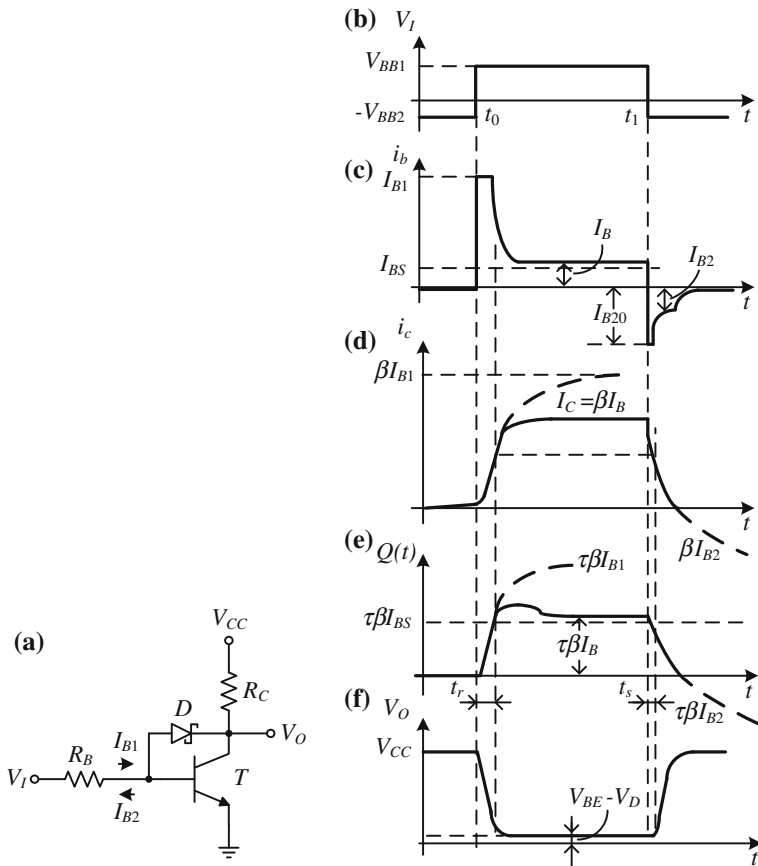


Fig. 2.37 Nonsaturated switch (a) and pulse waveforms of input (b) and output (f) voltages, base (c) and collector (d) currents, and base charge (e)

negative feedback loop which does not allow the transistor to go to saturation. For this reason these circuits are sometimes called the switching circuits comprising nonlinear feedback.

Let the drive be abrupt (Fig. 2.37b). For $t < t_0$ the transistor and the diode are off and $V_O = V_{CC}$. Upon a positive voltage step at the input at instant $t = t_0$, the transistor is switched on by the constant base current given by (2.118). The diode is off and the collector current is determined by (2.119). The output voltage is

$$V_O(t) = V_{CC} - \beta I_{B1} R_C (1 - e^{-t/\tau}), \quad (2.153)$$

where:

$$\tau'_{\beta e} = [\tau_{\beta} + \beta R_C (C_c + C_d)], \quad (2.154)$$

and C_d is the average capacitance of the reverse biased diode. The diode is turned on at instant t_1 when

$$V_d(t_1) = V_{BE} - V_O(t_1) = V_{Dt}. \quad (2.155)$$

From (2.154) and (2.155) it follows that

$$t_1 = \tau'_{\beta e} \ln \frac{\beta I_{B1}}{\beta I_{B1} - \frac{V_{CC} - (V_{BE} - V_{Dt})}{R_C}}. \quad (2.156)$$

Since the current I_{B1} through R_B is constant, upon switch-on of the diode, the base current will decrease by an amount corresponding to the diode current

$$I_{B1} = I_D + I_B. \quad (2.157)$$

After t_1 the current through R_C

$$I_{RC} = \frac{V_{CC} - (V_{BE} - V_D)}{R_C} \approx I_{CS} \quad (2.158)$$

is constant because the variations of V_{BE} and V_D are negligible. Since $V_{CE} = V_{BE} - V_D = 0.7 - 0.4 = 0.3$ V is only by 0.1 or 0.2 V greater than V_{CES} , it means that the transistor is nearly in the saturation region and that $I_{RC} \approx I_{CS}$. It can, therefore, be said that the switch-on of the diode ends the switch-on of the transistor. Indeed, expressions (2.121) and (2.156) are approximately the same since $I_{RC} \approx I_{CS}$. Thus, $t_1 = t_r$ is the rise time of the collector current.

The diode keeps the transistor in the active region, thus

$$I_C = \beta I_B = I_D + I_{RC}. \quad (2.159)$$

By combining (2.157) and (2.159) it follows that

$$I_B = \frac{I_{RC}}{\beta + 1} + I_B \frac{1}{\beta + 1}. \quad (2.160)$$

Since $I_{RC} \approx I_{CS} = \beta I_{BS}$, the base current is

$$I_B = \alpha I_{BS} + \frac{I_{B1}}{\beta + 1}. \quad (2.161)$$

This means that the base current is somewhat higher than I_{BS} and also than the collector current $I_C = I_{RC} + I_D > I_{CS}$ (Fig. 2.37d), and the transistor is certainly in the active region (I_{BS} and I_{CS} are the saturation currents of the transistor without the

diode). The waveform of the base current during the turn-on process is optimal (Figs. 2.37 and 2.33). Irrespective of the value of I_{B1} the transistor after t_r is close to the boundary between the active and the saturation region. This means that the turn-on may be established by a large base current

$$I_{B1} \gg \frac{V_{CC} - (V_{BE} - V_D)}{\beta R_C}, \quad (2.162)$$

and bearing in mind (2.138)

$$t_r \approx \tau_\alpha + (C_c + C_d) R_C I_{RC} / I_{B1}. \quad (2.163)$$

On the basis of (2.163) and (2.118) it follows that

$$R_B \ll \beta R_C \frac{V_{BB1} - V_{BE}}{V_{CC} - (V_{BE} - V_D)}. \quad (2.164)$$

If $V_{BB1} = V_{CC} \gg V_{BE}$, then $R_B \ll \beta R_C$. Usually, R_B and R_C are of the same order of magnitude, it is even possible that $R_B < R_C$.

After a negative step change of the input voltage at $t = t_1$, the base current becomes negative (Fig. 2.37c) and the transistor is turning off. The output voltage remains constant for some time until the collector current becomes equal to the current through R_C . During this time, the diode is conducting and

$$I_{B20} = I_{B2} + I_D = I_{B2} + \alpha(I_{B1} - I_{BS}), \quad (2.165)$$

where

$$I_{B2} \approx V_{BB2} / R_B. \quad (2.166)$$

Since the initial charge is $Q(0) = \tau_\beta I_B$, from the condition $Q(t_s) = \tau_\beta I_{BS}$ and on the basis of (2.114) the storage time is:

$$t_s = \tau_\beta \ln \frac{I_{B1} + I_{B2}}{\alpha I_{B1} + I_{B2} + I_{BS} / \beta + 1}. \quad (2.167)$$

The condition $I_{BS} / (1 + \beta) \ll \alpha I_{B1} + I_{B2}$ is always satisfied and

$$t_s = \tau_\beta \ln \frac{I_{B1} + I_{B2}}{\alpha I_{B1} + I_{B2}}. \quad (2.168)$$

Because $\alpha \approx 1$, $t_s \rightarrow 0$. If $V_{BB2} = 0$, then $I_{B2} = 0$ and:

$$t_s = \tau_\beta \ln 1 / \alpha = \tau_\beta \ln(1 + 1 / \beta) \approx \tau_\beta / \beta = \tau_\alpha. \quad (2.169)$$

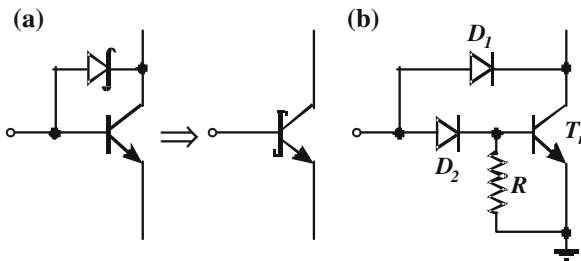


Fig. 2.38 Schottky transistor (a) and a nonsaturated switch comprising a silicon diode (b)

Therefore, although the transistor is in the active region, there exists a storage time but it is negligible.

After t_s , the diode is off and the fall-off time of the collector current is determined by (2.127) or (2.130) but C_c should be replaced by $C_c + C_d$.

The nonsaturated switches are most widely used in digital circuitry. A Schottky diode with a transistor makes a Schottky transistor (Fig. 2.38a). A common property of these circuits is high speed. However, the dissipation of the transistor is increased because while conducting it is in the active region, which is a weakness of this type of circuit.

If instead of a Schottky diode a silicon diode is used, it is necessary to use another diode (Fig. 2.38b). The collector junction here is not biased ($V_{BC} = -V_{D2} + V_{D1} \approx 0$) and the low level output voltage $V_{OL} = V_{BE}$ is increased. The resistor R reduces the base-emitter resistance when the transistor is off.

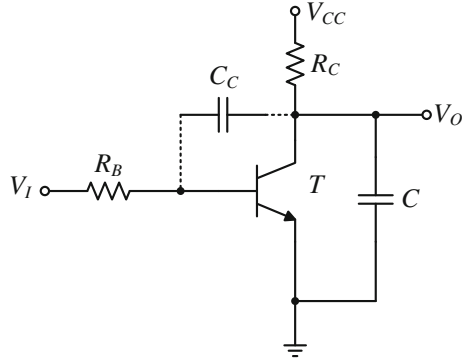
2.2.6 Capacitively Loaded Inverter

The output of an inverter is often loaded by a capacitor (Fig. 2.39). The influence of this capacitor on the transient mode is very noticeable. First of all, the transistor cannot go to saturation until this capacitor is discharged. The high level of the output voltage is not reached when the transistor is turned off, but when the capacitor is charged.

Let the drive be abrupt (Fig. 2.37b). Upon a positive voltage step at the input, the transistor turn-on process starts. Taking into account the collector junction capacitance, the collector current is

$$i_c(t) = \frac{V_{CC} - V_O}{R_C} - C \frac{dV_O}{dt} + C_c \frac{dV_{BC}}{dt} = \frac{\beta}{\tau_\beta} Q(t), \quad (2.170)$$

Fig. 2.39 Capacitively loaded inverter



where the charge $Q(t)$ in the base is determined by Eq. (2.109). If the variation of the voltage V_{BE} is neglected, then $dV_{BC}/dt = dV_O/dt$ and from (2.109) and (2.170) one obtains

$$\tau_\beta \tau \frac{d^2 V_O}{dt^2} + (\tau_{\beta e} + \tau) \frac{dV_O}{dt} + V_O = V_{CC} - \beta R_C I_{B1} \quad (2.171)$$

where

$$\tau = R_C(C_C + C), \quad (2.172)$$

and $\tau_{\beta e}$ is determined by (2.112). The solution of Eq. (2.171) can be written in the form

$$V_O(t) = A_1 e^{p_1 t} + A_2 e^{p_2 t} + V_{CC} - \beta R_C I_{B1}, \quad (2.173)$$

where p_1 and p_2 are the roots of the characteristic equation

$$p^2 + \frac{\tau_{\beta e} + \tau}{\tau_\beta \tau} p + \frac{1}{\tau_\beta \tau} = 0. \quad (2.174)$$

The constants A_1 and A_2 are determined from the initial conditions

$$V_O(0) = V_{CO} = V_{CC}; \quad (dV_O/dt)_{t=0} = 0,$$

thus

$$A_1 = \frac{p_2 \beta R_C I_{B1}}{p_2 - p_1}, \quad A_2 = \frac{p_1 \beta R_C I_{B1}}{p_1 - p_2}. \quad (2.175)$$

The rise time t_r in this case is determined from the condition that the collector junction is forward biased, i.e.,

$$V_{BC}(t_r) = V_{BE} - V_O(t_r) = V_{BC1},$$

that is

$$V_O(t_r) = V_{BE} - V_{BC1} = V_{CES}. \quad (2.176)$$

Equation (2.173) is transcendent and in general cannot be solved explicitly. If, however, the condition

$$x = 4\tau_\beta\tau / (\tau_{\beta e} + \tau)^2 \ll 1, \quad (2.177)$$

is fulfilled, then the roots of the characteristic equation are:

$$p_1 \approx \frac{\tau_{\beta e} + \tau}{\tau_\beta\tau}, \quad p_2 \approx \frac{1}{\tau_{\beta e} + \tau}. \quad (2.178)$$

Since the condition (2.177) applies, $|p_1| \gg |p_2|$ and the influence of the root p_1 can be neglected. Then, (2.173) reduces to

$$V_O(t) = V_{CC} - \beta I_{B1} R_C \left(1 - e^{-\frac{t}{\tau + \tau_{\beta e}}} \right), \quad (2.179)$$

and on the basis of (2.172) one obtains

$$t_r = \tau_{\beta c} \ln \frac{\beta I_{B1}}{\beta I_{B1} - (V_{CC} - V_{CES})/R_C} = \tau_{\beta c} \ln \frac{\beta I_{B1}}{\beta I_{B1} - I_{CS}}, \quad (2.180)$$

where

$$\tau_{\beta c} = \tau_{\beta e} + \tau = \tau_\beta + (\beta + 1) C_c R_C + C R_C. \quad (2.181)$$

By comparing (2.180) and (2.121) it may be noticed that the influence of the capacitance C reduces to the increase of the time constant by $C R_C$. Of course, this conclusion is correct only if condition (2.177) applies. The left-hand side in (2.177) is maximal for $\tau = \tau_{\beta e}$, amounting

$$x_{\max} = \frac{\tau_{\beta e}}{\tau_\beta + \beta C_c R_C}. \quad (2.182)$$

Thus, $x_{\max} < 1$ meaning that (2.180) applies for a wide range of C values. The maximum error is around the capacitance value

$$C = \tau_\beta / R_c + (\beta - 1) C_c \quad (2.183)$$

which is obtained for $\tau = \tau_{\beta e}$.

The capacitor C does not have any influence on the storage time t_s , because in that interval $V_o = V_{CES} = \text{const.}$ During t_f Eq. (2.171) applies but I_{B1} should be replaced by $I_{B2} = V_{BB2}/R_B$. It can be shown that if (2.177) applies

$$V_O(t) \approx V_{CC} + \beta R_c I_{B2} - R_c (I_{CS} + \beta I_{B2}) e^{-t/\tau_{\beta e}}. \quad (2.184)$$

Charging of the capacitor ends when $V_O = V_{CC}$ and from (2.179) one obtains:

$$t_f \approx [\tau_\beta + (\beta + 1) C_c R_c + CR_C] \ln(1 + I_{BS}/I_{B2}). \quad (2.185)$$

If $V_{BB2} = 0$, i.e. $I_{B2} = 0$, then t_f is determined from the condition $V_O = 0.9V_{CC}$, and

$$t_f \approx 2.3 \cdot [\tau_\beta + (\beta + 1) C_c R_c + CR_C]. \quad (2.186)$$

By comparing t_r and t_f of the inverter with and without a capacitor, it may be concluded that the influence of C reduces to increasing the time constant of the transistor. It should be emphasized that (2.185) and (2.186) are approximate since it is possible that the transistor is off ($i_c = 0$) before the capacitor is charged. Then t_f consists of two intervals: the first t_1 ending at $i_c(t_f) = 0$ and the second when C is being charged through the resistor R_C .

In practice it is often

$$CR_C \gg \tau_\beta + (\beta + 1) C_c R_c. \quad (2.187)$$

In such a case, the transistor can be considered an ideal switch. During the turn-on process the operating point will instantaneously move from the position A to the position B (Fig. 2.40a). The transistor is in the active region and the collector current is $I_C = \beta I_{B1}$ (Fig. 2.40b). The fall time of the collector voltage t_r is determined by (2.180) where, in view of (2.187), $\tau_{\beta c} \approx CR_C$.

For a negative input voltage step the transistor is instantaneously turned off ($i_c = 0$ Fig. 2.40b). The capacitor C charges through R_C and

$$t_f \approx 3R_C C. \quad (2.188)$$

For fast switching circuits, this time is unacceptably large. For this reason, more complex inverters, having lower output resistance when the output voltage is high, are used.

Two versions of such circuits are most frequently used (Fig. 2.41). In the circuit of Fig. 2.41a when T_{r1} is off, T_{r2} is on in the active region. The output resistance is $R_{OH} = R_C/(1 + \beta_2)$ and the rise time of the output voltage is

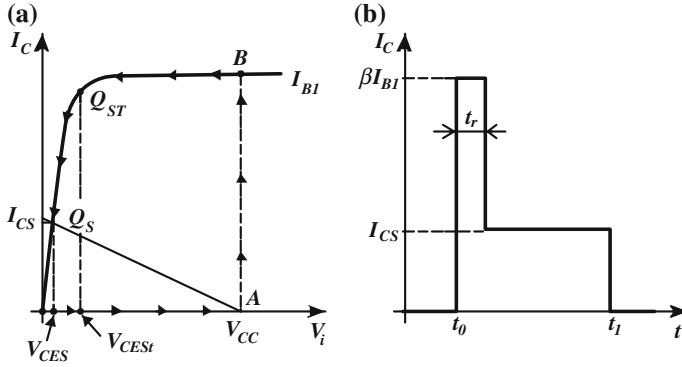


Fig. 2.40 Path of the operating point (a) and change of collector current when $CR_C \gg \tau_\beta + (\beta + 1)C_c R_C$ (b)

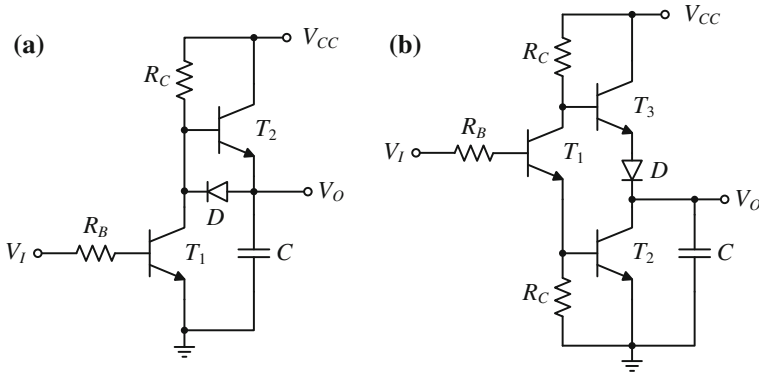


Fig. 2.41 Inverters with low output resistance in both static states

$$t_f \approx 3CR_C / (\beta_2 + 1). \quad (2.189)$$

The shortcoming of this circuit is that the low level of the output voltage is increased. Namely, when T_{r1} is in saturation, the diode D is conducting, T_{r2} is off and

$$V_{OL} = V_D + V_{CES1}. \quad (2.190)$$

For this reason, the more complex inverter of Fig. 2.41b is more frequently used. While T_{r1} and T_{r2} are in saturation, T_{r3} is off. The only purpose of the diode D here is that I_{r3} is to be off while T_{r1} and T_{r2} are conducting. If T_{r1} and T_{r2} are off, T_{r3} is in the active region and the output resistance is $R_{OH} \approx R_C / (1 + \beta_3)$, and the charging time of the capacitor is determined by (2.189).

2.2.7 Inductively Loaded Switch

In practice, the switch is sometimes inductively loaded. Typical examples of such loads are electromagnetic relays, motors, and various types of pulse circuits having transformer coupling. Figure 2.42a shows an inverter having an inductive load. Most often the collector winding is inductively coupled with a secondary winding driving a load whose resistance referred to the primary is denoted by R_0 . The peculiarity of an inductive load is that for fast variations (high frequencies) it behaves like a large resistance and in the quasi-stationary states it accumulates the electromagnetic energy which may exert a considerable influence upon the converter characteristics. The collector current i_c is determined by (2.119). For the circuit of Fig. 2.42a, it is

$$i_c(t) = \frac{V_{CC} - V_O}{R_0} + \frac{1}{L} \int_0^t (V_{CC} - V_O) dt. \quad (2.191)$$

Upon differentiation of (2.191) one obtains a differential equation whose solution, with initial condition $V_O(0) = V_{CC}$, is

$$V_O(t) = V_{CC} - \frac{\tau}{\tau - \tau_{\beta e}} \beta I_{B1} R_0 (e^{-t/\tau} - e^{-t/\tau_{\beta e}}), \quad (2.192)$$

where

$$\tau = L/R_0. \quad (2.193)$$

The time t_r required by the transistor to go to saturation is determined from condition (2.176). Equation (2.192), however, is transcendent and in general can

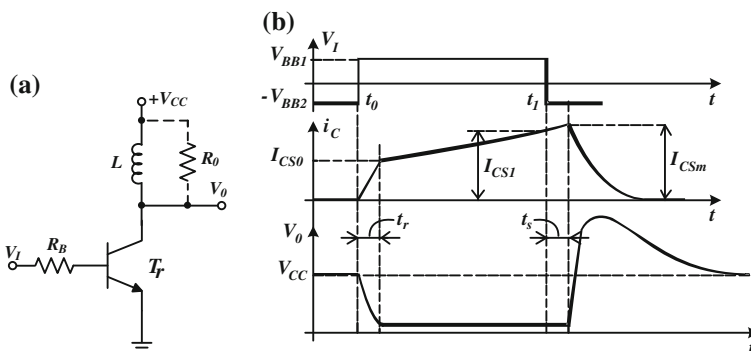


Fig. 2.42 Inverter having an inductive load (a) and the responses of collector current and voltage to a pulse drive (b)

not be solved explicitly. On the other hand, usually $\tau \gg \tau_{\beta e}$, i.e. $t_r \ll \tau$. Then $\exp(-t/\tau) \approx 1$ and

$$V_O(t) \approx V_{CC} - \beta I_{B1} R_0 (1 - e^{-t/\tau_{\beta e}}). \quad (2.194)$$

Now, from (2.176) and (2.194) it follows that

$$t_r \approx \tau_{\beta e} \ln \frac{\beta I_{B1}}{\beta I_{B1} - I_{CSO}}, \quad (2.195)$$

where

$$I_{CSO} = \frac{V_{CC} - V_{CES}}{R_0}. \quad (2.196)$$

Therefore, t_r is the same as if the collector load were $R_C = R_0$. This is due to the fact that the resistivity of the winding during t_r is very high and its influence can be neglected.

However, the situation $\tau \ll \tau_{\beta e}$ is possible. This occurs when the resistance R_0 is very high ($R_0 \rightarrow \infty$) as in the case of electromagnetic relays. Then $t_r \ll \tau_{\beta}$, and $\exp(-t/\tau) \approx 1$ so

$$V_O(t) \approx V_{CC} - \frac{\beta I_{B1} L}{\tau_{\beta}} (1 - e^{-t/\tau}). \quad (2.197)$$

By taking $\ln(1 - x) \approx -x$ for $x \ll 1$, from (2.195) it is approximately

$$t_r \approx \tau_{\beta} \frac{V_{CC}}{\beta I_{B1} R_0} = \tau_{\alpha} \frac{V_{CC}}{I_{B1} R_0}. \quad (2.198)$$

Therefore, if $R_0 \rightarrow \infty$, then $t \rightarrow 0$. This means that a transistor loaded by an electromagnetic relay is practically turned on instantly.

After t_r the transistor is in saturation. The voltage across the winding $V_{CC} - V_{CES}$ is constant and the winding current will increase linearly. The collector current (Fig. 2.42b) is

$$i_c(t) = I_{CSO} + \frac{V_{CC} - V_{CES}}{L} t. \quad (2.199)$$

During the time interval $t_1 - t_0 = T_1$, the transient regime in the winding does not have to be completed. More frequent is the other case (Fig. 2.42b). Then the

resistance R_B is determined from the condition that for $t = T_1$ the transistor is weakly saturated, i.e.

$$I_{B1} = \frac{V_{BB1} - V_{BES}}{R_B} \geq \frac{1}{\beta} I_{CS1} = \frac{1}{\beta} \left[I_{CS0} + \frac{V_{CC} - V_{CES}}{L} T_1 \right], \quad (2.200)$$

giving

$$R_B \leq \beta \frac{V_{BB1} - V_{BES}}{\frac{V_{CC} - V_{CES}}{R_0} + \frac{V_{CC} - V_{CES}}{L} T_1}. \quad (2.201)$$

At an instant $t = t_1$, when the input voltage becomes negative, the output voltage remains constant while the excess charge piled up in the base is cleared. This is the storage time t_s , during which the collector current increases according to (2.199). Since the base charge is controlled by the base current, the change of $Q(t)$ is as for the inverter loaded by R_C . Therefore, the time t_s is determined by (2.125) and

$$I_{BS} = \frac{I_{CSm}}{\beta} = \frac{1}{\beta} i_c (T_1 + t_s). \quad (2.202)$$

Usually $t_s \ll T_1$ and the maximum collector current is

$$I_{CSm} = I_{CS0} + \frac{V_{CC} - V_{CES}}{L} (T_1 + t_s) \approx I_{CS0} + \frac{V_{CC} - V_{CES}}{L} T_1. \quad (2.203)$$

This current must be lower than the maximum permitted collector current ($I_{CSm} < I_{CD}$), resulting in the condition

$$L > \frac{V_{CC} - V_{CES}}{I_{CD} - I_{CS0}} T_1. \quad (2.204)$$

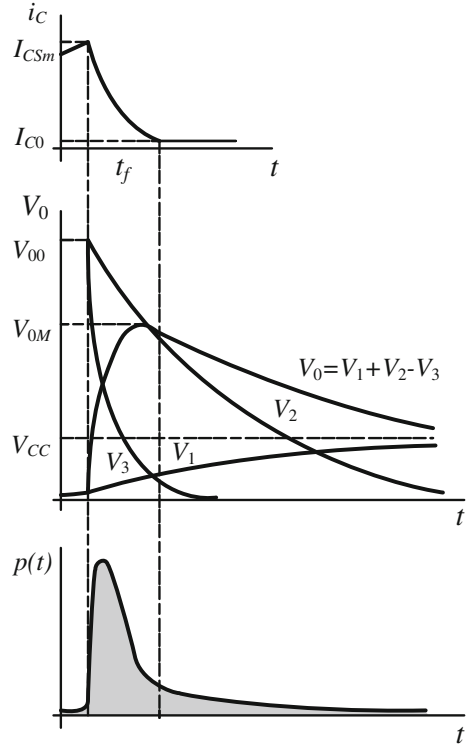
After t_s expires, the collector current decreases and is determined by (2.126). By introducing (2.126) in (2.191), differentiating the obtained equation and solving it for V_o , and using the initial condition $V_o(0) = V_{CES} \approx 0$, one obtains

$$V_o(t) = V_{CC}(1 - e^{-t/\tau}) + \frac{R_0(I_{CSm} + \beta I_{B2})}{\tau - \tau_{\beta e}} \tau (e^{-t/\tau} - e^{-t/\tau_{\beta e}}). \quad (2.205)$$

If the factor in front of the second bracket is denoted by V_{O0} , then (2.205) can be written as:

$$v_o(t) = V_{CC}(1 - e^{-t/\tau}) + V_{O0} e^{-t/\tau} - V_{O0} e^{-t/\tau_{\beta e}} = v_1 + v_2 - v_3. \quad (2.206)$$

Fig. 2.43 Collector current, output voltage V_o , and power of dissipation P during the turn-off process of transistor



The dependence (2.206) for $\tau \gg \tau_{\beta e}$ is shown in Fig. 2.43 and the following conclusions may be drawn. The output voltage increases faster than the collector current decreases. During the fall time t_f , given by (2.127), a situation when $V_o \gg V_{CC}$ is possible. The maximum output voltage is approximately

$$V_{OM} \approx V_{CC} + R_0(V_{CC} T_1/L + \beta I_{B2}). \quad (2.207)$$

Owing to this the dissipation of the transistor $P(t) = i_c(t)V_o(t)$ is rather high (Fig. 2.43).

Example 2.4 For the circuit of Fig. 2.44

- Explain how the accumulated electromagnetic energy returns to the source
- Determine the maximum inverse voltage that appears at the diode D_2 .
- Determine the time of core transformer demagnetization t_x assuming that all the energy accumulated in the magnetization inductance returns to the source.
- Show the waveforms of the voltage on the transistor collector, the voltage on the secondary winding and the current through that winding using PSPICE software package.

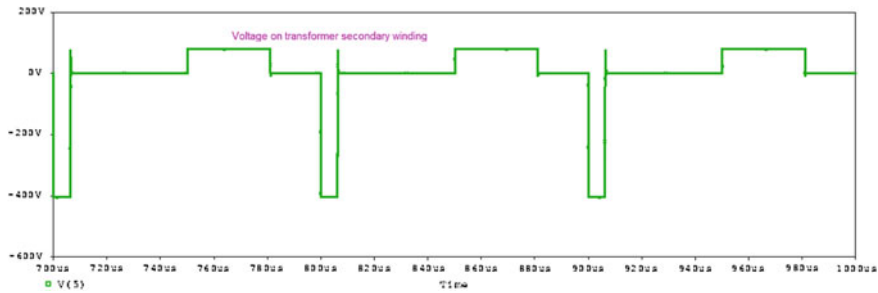


Fig. 2.46 Waveform of voltage on transformer secondary winding

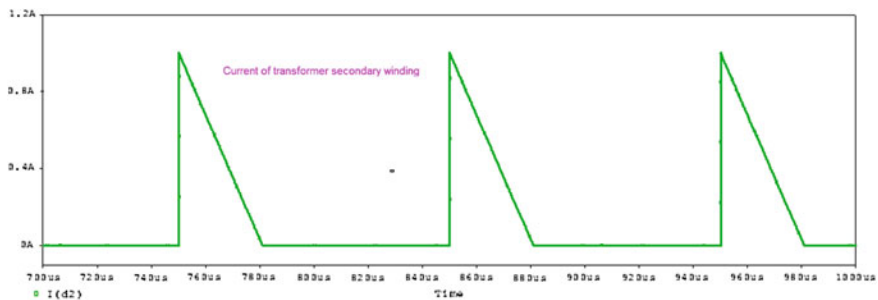


Fig. 2.47 Waveform of current through transformer secondary winding

$$V_{D,inv} = V_{CC} - (-NV_{CC}) = (1 + N)V_{CC} = 480 \text{ V}.$$

Assuming that all accumulated energy in the magnetizing inductance returns to the source, the following expression can be written (Figs. 2.46 and 2.47)

2.2.7.1 Transistor Protection

The voltage V_{OM} must be lower than the collector-base breakdown voltage

$$V_{OM} < BV_{CBO}. \quad (2.208)$$

Otherwise, the transistor must be protected. The switching circuits in relays and in blocking generators are protected by adding a diode (Fig. 2.48a). When $V_o > V_{CC} + V_{Dt}$, the diode is conducting and it limits the output voltage (Fig. 2.48b). The use of a Schottky diode is recommendable. The collector current (Fig. 2.48b) increases exponentially because the resistance of the winding, r_L , cannot be neglected.

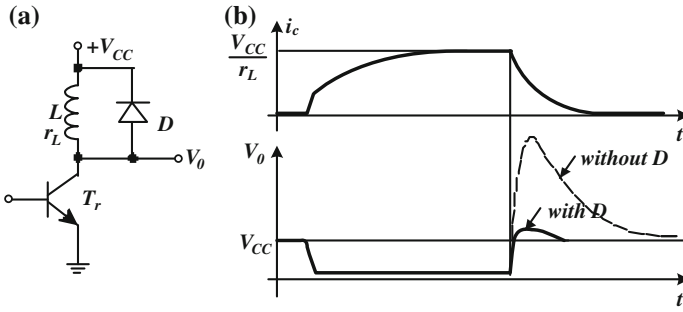


Fig. 2.48 Protection of transistor (a) and pulse waveforms of the collector current and output voltage when a relay is the load (b)

The increased dissipation during the turn-off process of the transistor is another problem. The dynamic losses are exactly then at the maximum. In order to reduce them, the increase of the collector voltage should be slowed down until the current falls to zero. This is accomplished by using the so called dv/dt or snubber circuits (Fig. 2.49a). These circuits are often referred to as the circuits for shaping the transistor load line or the transistor turn-off protection circuits. An efficient snubber circuit should: limit the maximum collector voltage below the breakdown voltage, slow down the output voltage ascent until collector current falls and ensure that the total losses in the transistor and the dv/dt circuit are minimal. All this, to a good degree, is provided by the DRC dv/dt circuit (Fig. 2.49a). During the turn-off process the diode is conducting and the capacitor C is charged, thus slowing down the rate of ascent of the output voltage. An accurate analysis would be quite complicated. Therefore only the approximate relations satisfactory for practical

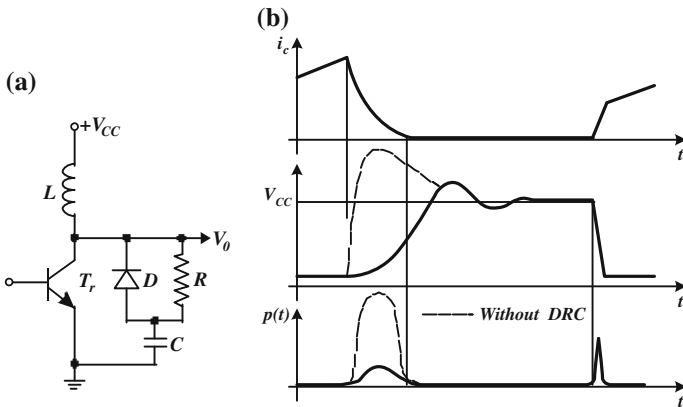


Fig. 2.49 Protection DRC circuit during transistor turn-off process (a) and the corresponding pulse waveforms (b)

calculations are given here. The accumulated electromagnetic energy is transferred to the capacitor, so it can be written that

$$\frac{1}{2} L I_{LM}^2 = \frac{1}{2} C V_{OM}^2, \quad (2.209)$$

where $I_{LM} = I_{CSM}$ is the maximum current of the winding. From (2.209) and (2.199) it follows that the maximum output voltage is

$$V_{OM} = V_{CC} \frac{\tau + T_1}{\sqrt{LC}}. \quad (2.210)$$

where $\tau = L/R_o$. On the other hand, if t_r and t_f are the maximum rise time of the output voltage and the maximum fall time of the collector current, respectively, then it can be written that

$$\frac{1}{2} C V_{OM}^2 = \frac{I_{CSM} V_{OM} (t_r + t_f)}{2}. \quad (2.211)$$

On the basis of (2.211) and (2.209) the capacitance is approximately

$$C = (t_r + t_f)^2 / L. \quad (2.212)$$

In practice the values of the capacitance C are between several nF and several hundreds nF . When the transistor is on, the diode is off and the capacitor discharges through the resistor R . If the discharge time is taken to be $3RC$, then it has to be:

Fig. 2.50 Turn-on protection circuit at a switch with bipolar transistor

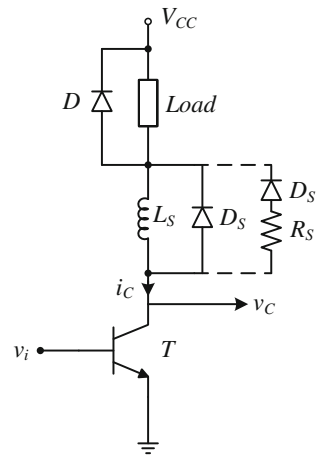
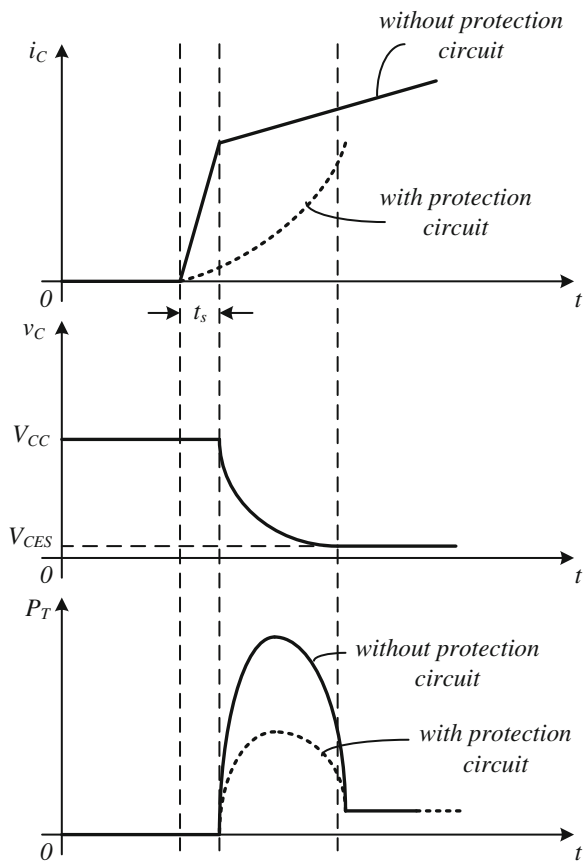


Fig. 2.51 Waveforms of the collector current, the collector voltage and power dissipation on bipolar transistor during the switch turn on process without turn on protection circuits and with a turn on protection circuit



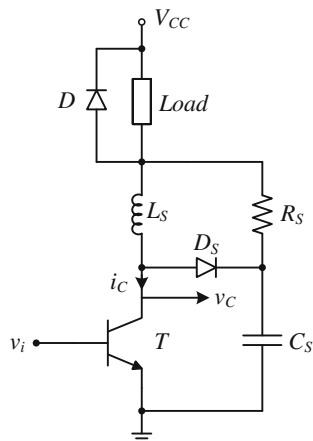
$$R \leq \frac{T_{1min}}{3C}, \quad (2.213)$$

where T_{1min} is the minimum conduction time of the transistor.

Besides the turn-off, there is the turn-on protection circuit (Fig. 2.50). The aim of this protective circuit is to reduce the speed of increase of the collector current and thus to reduce the dissipation on the transistor when the switch is turning on (Fig. 2.51). This protection circuit consists of the inductance L_S connected in the collector circuit of the switching transistor and the diode D_S connected in anti-parallel with the inductance L_S .

Due to a rather large time constant $\tau = L_S/r_S$ (r_S —series connection of the diode resistance in on state and the resistance of the inductor L_S), the resistance R_S can be connected in series with the diode D_S . The goal is to increase the time constant, so the inductor can ensure the use of accumulated energy in the time interval when the transistor T is turned off. In this case it is necessary to take into account the maximum collector voltage of the transistor, because the discharge current of the

Fig. 2.52 Combined protection circuit of switch with bipolar transistor



inductance L_S generates voltage on the resistor R_S which increases the total voltage on the collector of the transistor.

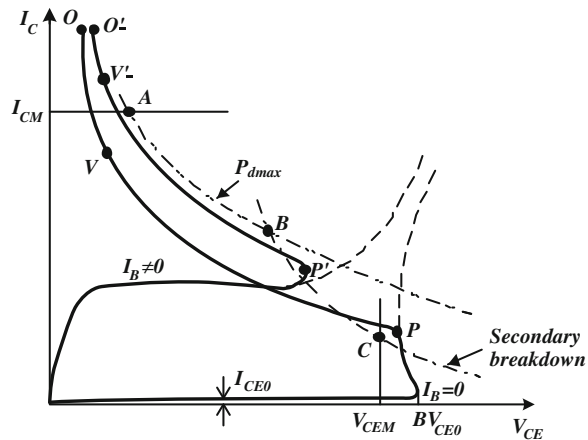
There is also a combined protection circuit that reduces losses in the bipolar transistor when the switch is turning on and turning off (Fig. 2.52). The function of the turn-on protection circuits is assumed by the inductance L_S , the diode D_S and the resistor R_S . On the other hand, the role of the turn-off protective circuits is played by the capacitance C_S , the diode D_S and the resistor R_S . These elements ensure a protective function in the same manner as already described for the turn-on and turn-off protection circuits.

2.2.8 Transistor Selection

The key element in the pulse converters and voltage stabilizers is the switching transistor. As a rule, it is in a heavy duty operating mode (high current while on, high voltage while off, and significant voltages and currents during transients). For this reason considerable attention should be paid to the design of the optimum driving and dv/dt circuits and to the selection of the transistor. If the transistor is to operate reliably, its limitations must be strictly taken into consideration. This primarily concerns the limitations as regards the voltage, current, and dissipation.

The maximum voltage is limited by the breakdown voltages BV_{CB0} and BV_{CE0} (Sect. 2.2.1.1). In power transistors a secondary breakdown may appear. It manifests itself by an abrupt decrease of the collector–emitter voltage accompanied by a simultaneous increase of the collector current (Fig. 2.53). It occurs when both the voltage and the current are large simultaneously. The secondary breakdown starts when the current concentrates to a small area of the junction which leads to a considerable rise in temperature, creating a so called “hot spot”. This gives rise to

Fig. 2.53 Output characteristics of a power transistor in the region of secondary breakdown



the thermal regenerative process which is a characteristic of power transistors. However, in addition to the thermal instability at high collector currents, an electrical instability appears there, which creates the conditions for avalanche injection of majority carriers at the collector junction. This is particularly marked in the high voltage switching transistors having a lightly doped collector region. The ionic electric field appears exactly at the surface between the light doped regions and causes the avalanche injection of the charge carriers. In order to eliminate as much as possible the mechanisms leading to thermal and electrical instabilities, efforts are being made to eliminate any crystal defects, metallic impurities, interstitials, etc. In addition, a maximally efficient heat removal should be ensured. Figure 2.53 shows the transistor output characteristics for $I_B = 0$ and $I_B \neq 0$.

In Fig. 2.53 the characteristics are extended by dotted lines in order to show what they would be like if there were no secondary breakdown which appears at the points P and P' . Between the points V and O and V' and O' the collector-emitter resistance is very low. If the transistor were then switched off, it would return to the original characteristics without a visible damage. If, however, the current is not limited and the operating point reaches the position O or O' , the junction temperature may reach the melting point causing failure and permanent damage to the transistor. Figure 2.53 also shows the limitations: the maximum current I_{CM} , the maximum voltage V_{CEM} ($V_{CEM} < BV_{CEO}$), the maximum dissipation, and the hyperbola limiting the appearance of the secondary breakdown. They all make the region of reliable operation of the transistor as represented by the surface $V_{CEM}-C-B-A-I_{CM}$. Therefore, at high V_{CE} the limitation is the breakdown voltage, at low V_{CE} the limitation is the maximum current, and between the points A and B the limitation is the maximum dissipation.

The maximum permitted dissipation is determined by the maximum junction temperature which is for silicon transistors between 170 and 200 °C. Namely, the power $P = V_{CE}I_C$ generated in the transistor is converted to heat. For this reason the

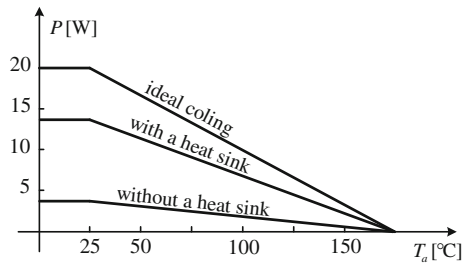


Fig. 2.54 An illustration of the dependence of the permitted power on temperature for different thermal resistances

temperature of the crystal is always higher than that of the environment. At excessive temperatures the transistor will either be suddenly destroyed or its characteristics will degrade gradually.

The heat developed in the transistor is transferred through the case and the heat sink to the environment. In steady state:

$$P_d = VI = \frac{T_j - T_a}{R_{jc} + R_{ca}}, \quad (2.214)$$

where T_j and T_a are the temperatures of the junction and ambient temperature, respectively. R_{jc} is often called the internal thermal resistance. It is constant and ranges from several tenths of $^{\circ}\text{C}/\text{W}$ for low power transistors up to several tens of $^{\circ}\text{C}/\text{W}$ for high power transistors. The external thermal resistance depends upon the means of heat transfer from the case to the environment. It is highest when the case is free in the air. The heat transfer can be considerably improved by means of heat sinks. In principle, heat sink is a metal surface on which the transistor is mounted. In this way R_{ca} is considerably decreased. Good dimensioning and mounting of a heat sink are very important, particularly if the dissipation is high. As a rule, as soon as the power generated in a transistor exceeds 100 mW, an adequate heat sink should be used.

Manufacturers often give diagrams showing the dependence of the maximum permitted power on ambient temperature for different values of R_{ca} . A typical example of such a diagram is shown in Fig. 2.54. Ideal cooling is obtained when the external thermal resistance is zero ($R_{ca} = 0$) and the case temperature is equal to the ambient temperature ($T_c = T_a$). Such cooling is possible if the transistor is for example immersed in oil. At low temperatures up to 25 $^{\circ}\text{C}$ the permitted power is constant.

Manufacturers give the Safe Operating Area (SOA) for a given ambient temperature. SOA respects all the limitations mentioned previously. It is different for DC and pulse operating modes (Fig. 2.55a). The narrower the pulse, the wider the area of reliable operation.

Manufacturers often give SOA separately when the device is conducting (Fig. 2.55a) and also when it is off (Fig. 2.55b).

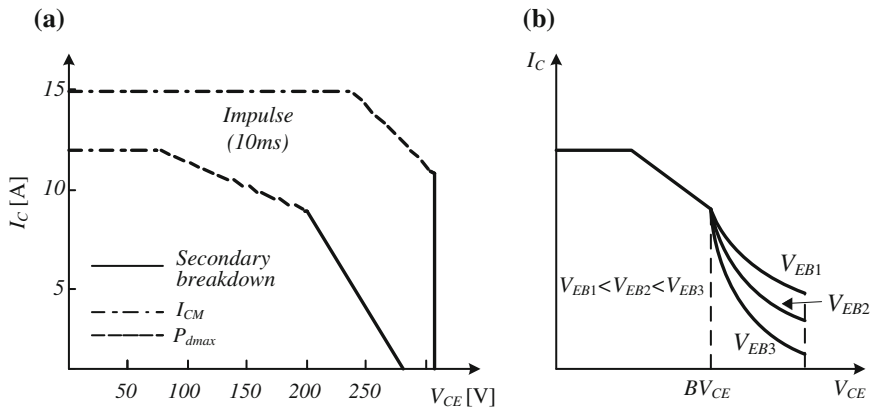


Fig. 2.55 Safe Operating Area at forward bias (a) and reverse bias of the emitter p-n junction (b)

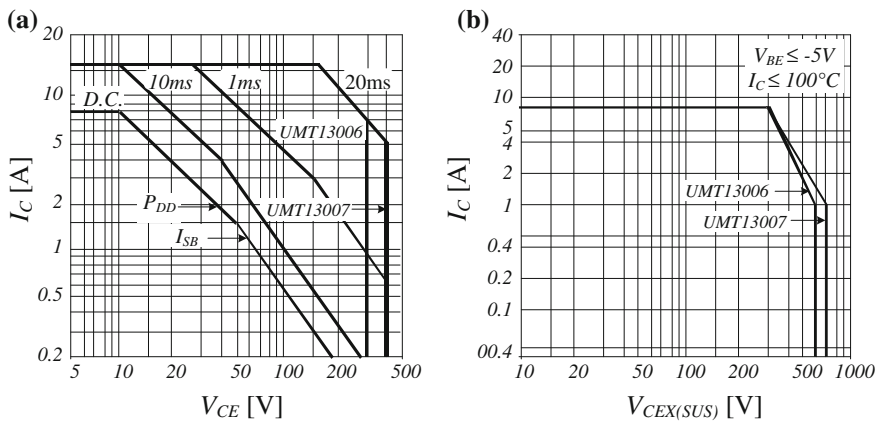


Fig. 2.56 SOA of switching transistors UMT 13006 and 13007 manufactured by UNITRODE, when on (a) and when off (b)

The region of operation at reverse bias is extended because the collector current is then very low and the breakdown voltage is higher. This region is often called the Reverse-Bias Safe Operating Area (RBSOA). Figure 2.56 shows SOA and RBSOA of the power transistors UMT 13006 and UMT 13007.

The dependencies of the current gain and saturation voltage on the collector current (Fig. 2.57) are very important for the selection of a good transistor. They are important since here β is lower and V_{CES} is higher than the corresponding parameters of low power transistors (below 1 W). The maximum frequency of the switching transistors depends on the turn-on and turn-off times. These characteristics too are usually given as functions of the collector current (Fig. 2.58) for a specified test circuit. The curves in Fig. 2.55 are given for an inverter comprising resistors $R_B = 5 \text{ V}/I_B$ and $R_C = 125 \text{ V}/I_C$ for $I_C/I_B = 5$ (Fig. 2.56).

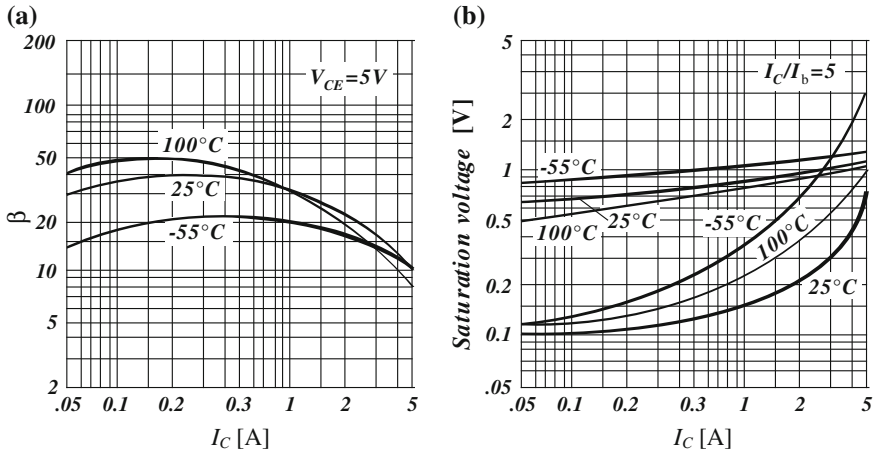


Fig. 2.57 Current gain β (a) and saturation voltages V_{BE} and V_{CE} (b) as functions of collector current for power transistors UMT 13006 and UMT 13007

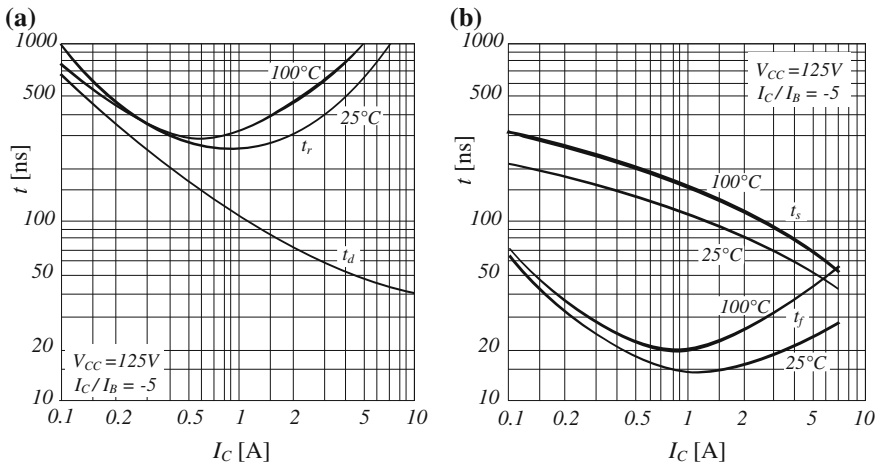


Fig. 2.58 The transient times at turn-on (a) and turn-off (b) as functions of collector current for transistors UMT 13006 and UMT 13007 for a pulse drive by $V_{BB1} = +6\text{ V}$ and $V_{BB2} = -4\text{ V}$

The minimum cycle of the control pulses of a switching transistor should be five to ten times longer than the sum of the turn-on and the turn-off times, i.e. $T_{\min} = (5-10)(t_d + t_r + t_s + t_f)$.

For an optimum use of a power transistor the snubber and driving circuits should be designed very carefully. An optimum driving circuit should have the following properties:

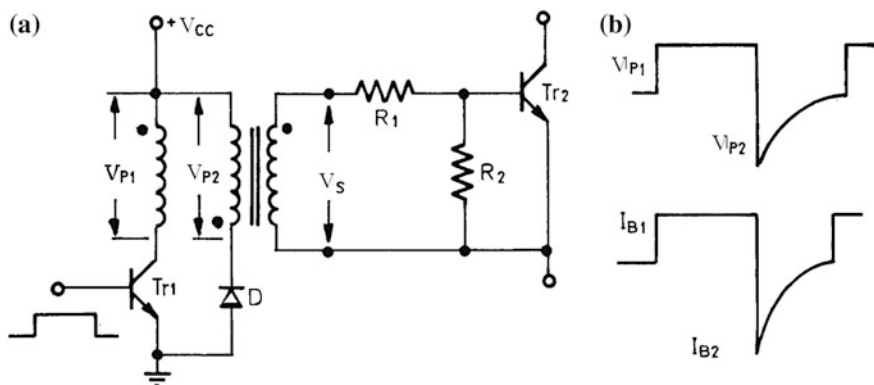


Fig. 2.59 Transformer driving circuit (a) and pulse waveforms of voltage V_{p1} and base current (b)

- The driving current should be sufficiently high to render dynamic losses as low as possible. Upon turn-on of the transistor, the driving circuit should provide the control of the degree of saturation.
- In order to render the falloff time of the collector current as short as possible and to minimize dynamic losses, turning off of the transistor should be “forced” by a large negative current. In doing so, care should be taken that the emitter clearance does not occur. It is desirable that the emitter junction is reverse biased while the transistor is off. If this is not possible, then the emitter-base resistance should be low so that the collector current is approximately I_{CO} and the breakdown voltage is maximal.
- The consumption of the driving circuit should be as low as possible.
- The circuit should be as simple as possible.

Usually the optimum drive is accomplished by a speed up capacitor. Its capacitance is determined by the criterion of the minimum duration of the transient mode (Sect. 2.2.4). Very often, for very powerful converters the power and the control parts are galvanically separated by a transformer coupling in the driving circuit. In that case the role of the speed up capacitor may be taken over by the third winding (Fig. 2.59a).

During the turn-off process of the transistor T_{r1} , the previously accumulated energy in the transformer primary is returned to the power source V_{CC} via the third winding. Since this winding is wound up in the opposite direction compared to the other two, a negative voltage is induced in the secondary and it provides a negative base current of the power transistor T_{r2} which is quickly turned off. The resistance R_1 is determined from the condition that at the end of the interval of conduction the transistor T_{r2} is in weak saturation. T_{r2} is actively cut off by the resistor R_2 . Typically, its value is from 50 to 100 Ω .

2.2.9 Driver Circuits

In order to improve the dynamic characteristics of the switch adequate excitation and driver circuits are used. The Baker clamp circuit is shown in Fig. 2.60. This circuit not only ensures better dynamic characteristics but also when the transistor is in off state, causes that both of the p-n junctions are reversely biased. The diode D_2 and D_1 provide the collector p-n junction voltage around 0 V.

The transistor does not enter saturation, but works instead in the active region close to the saturation region, so that it has a shorter turn off time for the same excitation ($t_S = 0$). When the input voltage is negative, the base is not broken, but the diode D_3 provides a negative polarization of the emitter p-n junction.

A Totem pole drive is shown in Figure 2.61. The dynamic characteristics of the switch are significantly improved by such a circuit. In this driver circuit using a speed up capacitor and a complementary pair of transistors T_2 and T_3 an

Fig. 2.60 Baker clamp circuit

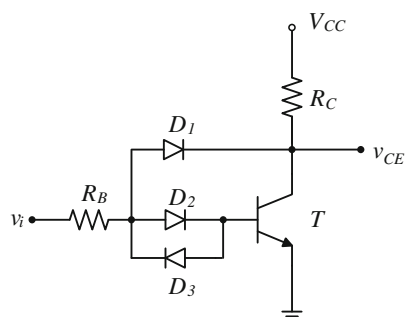
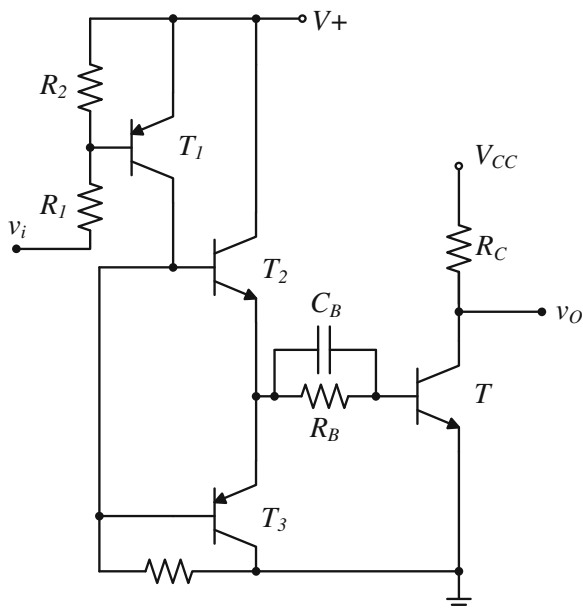


Fig. 2.61 Totem pole driver



approximately $\beta + 1$ times higher base current is obtained during the transistor transition processes compared to the case when only a speed up capacitor is used. The circuit works as follows. When the input v_i is low, the transistor T_1 leads and its collector current excites the transistor T_2 . The transistor T_2 provides the base current through the speed up capacitor which turns on the transistor T .

When the transistor T turns off the input v_i is high, and the transistor T_1 is turned off, as well as the transistor T_2 . The voltage on the speed up capacitor C_B provides direct polarization of the transistor T_3 and ensures the flow of the base current of the transistor T , which turns it off.

2.3 Power MOS Transistor as Switch

MOS transistors are increasingly replacing bipolar transistors in the pulse power supplies. A significant advantage of a MOS power transistor over a bipolar one is in that their input resistance is very high (of the order of 10^8 – $10^9 \Omega$) so that the input currents are of the order of nA. Thanks to this the consumption of the driving circuit is negligible, since for control purposes it is necessary to provide only the corresponding gate—source voltage. For this reason these transistors are called the voltage controlled components. Since the MOS transistors are unipolar, they do not incorporate the effect of storage of minority charge carriers, and consequently there is no storage time in the turn-off process. The duration of the transient mode is almost one order of magnitude shorter compared to that of the bipolar transistors. Thanks to this, the operating frequency is increased from several tens of kHz for bipolar transistors to hundreds (100–200) kHz for MOS transistors. The drain current is characterized by a negative temperature coefficient, so the MOS transistors are thermally very stable. Therefore, the conditions for the appearance of the secondary breakdown are reduced to minimum. The main shortcoming of the MOS transistors is a higher on-resistance and therefore a higher quasi-stationary dissipation. Table 2.2 presents the comparative characteristics of the bipolar and MOS power transistors.

Owing to large voltages and currents in the operating modes of power transistors there exist significant peculiarities in the manufacturing technology of the conventional MOS transistors. Fortunately, the static V-I characteristics are of nearly of the same form for all of them:

$$I_D = \beta_n f(V_{gs}, V_{ds}), \quad (2.215)$$

where $f(V_{gs}, V_{ds})$ is the function of the bias voltages depending upon the position of the operating point, and

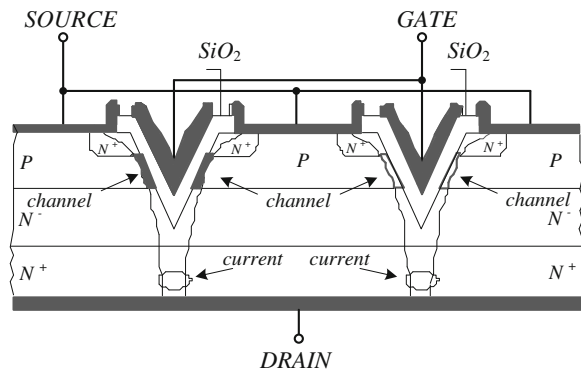
Table 2.2 Comparative characteristics of the power bipolar and MOS transistors

Parameter	Bipolar	MOS
Input resistance	Low	High (of the order $10^9 \Omega$)
Drive	Current controlled	Voltage controlled
Gain	100–2000	Not defined
Turn-on time	(50–500) ns	(10–200) ns
Turn-off time	(500–2000) ns	(10–600) ns
Charge carriers	Minority	Majority
Storage time	(1–5) μ s	Does not exist
Cut off frequency	Below 100 MHz	Of the order of GHz
Substrate resistance	0.3 Ω	(0.03–2) Ω
SOA	Poor (the appearance of the secondary breakdown)	Good (there is no secondary breakdown)
Thermal stability	Circuit additions required	No additions required
Parallel operation	With special coupling only	No additions required
Adjustable to LSI circuits	No	Yes
Driving signal	(0.1–10) A	Max 100 mA at $R_c = 50 \Omega$, $V_G = 5$ V
Driving circuit	Complex	Simple
Reverse voltage	High ($V_R > 1,500$ V)	Low ($V_R < 1,000$ V)
Transfer characteristic ($I_C = f(V_{BE})$, $I_D = f(V_{GS})$)	Exponential	At small currents quadratic, at high currents linear
Transconductance	High	Low

$$\beta_n = \frac{\mu_n \epsilon_{ox}}{2t_{ox}} \frac{W}{L} \quad (2.216)$$

is a constant of MOS transistors expressed in A/V^2 and does not have the meaning of the gain as it does for bipolar transistors. This constant thus depends on electron mobility in the channel μ_n , the dielectric constant of the oxide ϵ_{ox} , the thickness of the oxide below the gate t_{ox} , the width W and the length L of the channel. The parameters μ_n and ϵ_{ox} are constants of the technological process. Therefore, the drain current can be increased if the width of the channel, W , is increased, the length of the channel, L , is decreased, or the thickness of the oxide, t_{ox} , is decreased. The decrease of t_{ox} is limited by the gate breakdown voltage. If the length of the channel is decreased below a certain limit, the drain-source breakdown voltage will be decreased because the breakdown would occur as a punch-through. In this way instead of increasing the power one would decrease it. At the beginning of the development of the power MOS transistors (the first ones appeared in 1978) large drain currents have been obtained by increasing the channel width. However, this does have its shortcomings. First of all, this increases the necessary surface of the silicon wafer which reduces the production yield.

Fig. 2.62 Cross section of a power VMOS transistor



Currently, MOS power transistors are produced by connecting in parallel a large number of transistors on the same wafer. Usually this is done by using the so called vertical structure where the contacts of the drain and the source are on the opposite sides and the current flows vertically through the substrate. This allows a higher density of MOS cells since the depletion region spreads through the substrate vertically not laterally.

The VMOS transistor was among the first MOS power transistors based on the above principle (Fig. 2.62). The letter V originates from the shape of the profile of the grooves made in silicon by etching. The deficiency of these transistors is related to the problems of controlling this technical process. In addition, the channel is in the (111) plane so the mobility of carriers is reduced by 25 % and a higher threshold voltage is required. These are the main reasons that the production of these transistors has exhibited a decline.

2.3.1 Power VDMOS Transistor

To make a short channel one needs a double diffusion: a deep diffusion of *p*-type impurities first and then a shallow diffusion of *n*-type impurities. Both diffusions are carried out through the same opening. The length of the channel is the difference between the lateral diffusions of the *p*-type and *n*-type impurities, i.e. $L = X_{jp} - X_{jn}$. There are two types of these transistors lateral—LDMOS and vertical—VDMOS. At present the use of the polysilicon-gate VDMOS (Vertical Double-diffused MOS) prevails (Fig. 2.63).

The gate and the source contacts are on the upper side and the drain is on the lower side of the silicon wafer. The source and the drain are separated by a low doped *n* type epitaxial layer so that the breakdown voltage BV_{DS} is quite high (several hundreds V). The length of the channel is shorter than 1 μm and the drain current of the transistor is large (several tens A). The source and substrate are short circuited so that these transistors always operate at $V_{BS} = 0$. The substrate and the

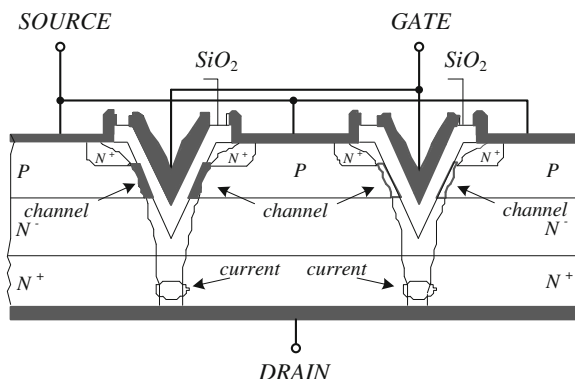


Fig. 2.63 Cross section of a polysilicon gate VDMOS power transistor

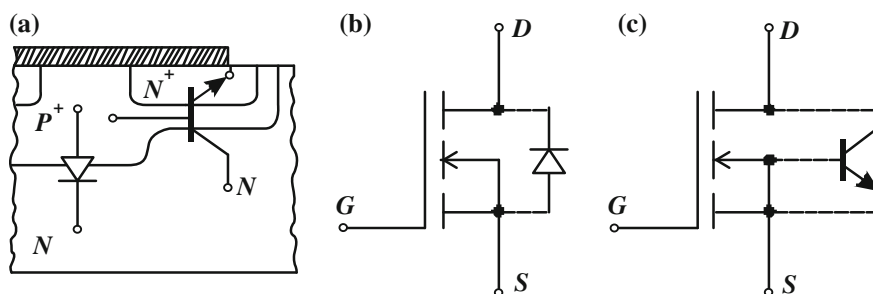
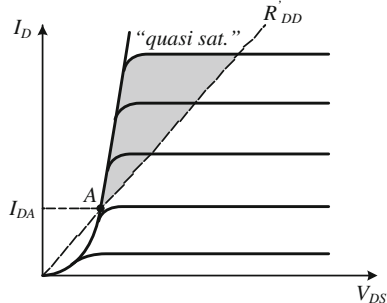


Fig. 2.64 Parasitic elements (a) and symbols of VDMOS transistors including parasitic diode (b) and parasitic transistor (c)

drain make a parasitic diode (Fig. 2.64) which is reverse biased and has no influence in the normal mode, at $V_{DS} > 0$. If $V_{DS} < 0$ this diode will conduct and limit the drain-source voltage to approximately -1 V. In some applications this is used for transistor protection. Besides the diode, there is a parasitic vertical *NPN* transistor (Fig. 2.64c). However, the base and the emitter are short circuited and the transistor effect does not appear.

A power VDMOS consists of a large number (several tens of thousands) of basic cells—small transistors connected in parallel. Their positioning can be of any polygonal form. It turns out that the hexagonal form is optimal and such VDMOS is called **HEXFET**. Some other commercial names are also used. For instance, *Siemens'* name is **SIPMOS** (**SI**emens **P**ower **MOS**), *Motorola's* is **TMOS**. *T* in this name illustrates the flow of current that proceeds through the channel horizontally and then turns vertically towards the drain. Thus a letter *T* is formed by the current flows of two neighboring elements (Fig. 2.63).

Fig. 2.66 Output characteristics of IGBT



are connected as in a VDMOS transistor. If, on the other hand, R_{BE} and α_{npn} are sufficiently high, the structure from Fig. 2.65 behaves like an MOS thyristor (Fig. 2.67a, b). The thyristor effect already appears at gate voltages of the order of 3 V. Then, the PNP transistor starts conducting first, and it is followed by the *NPN* transistor. The positive feedback will act if $\alpha_{npn} + \alpha_{pnp} > 1$. The advantage of an MOS thyristor over a standard thyristor is that it can be switched on by a very low power. Another type of *BiMOS* switch is the cascade connection of the MOS and the bipolar transistors (Fig. 2.67c). This is often called the emitter switch.

The switch is controlled by the gate of the MOS transistor, M_n . When M_n is off, the bipolar transistors are also off. Since the emitter is now “open”, the breakdown voltage of the transistor T_{r1} is maximal and amounts to BV_{CBO} . On the other hand, during the turn-off all current flows into the base circuit since $I_E = 0$. Thanks to this the storage and the falloff times of the collector current are very short. The drain-source voltage of T_{r1} when off is practically V_{BB} . This means that one can use a low breakdown voltage MOS transistor (up to several tens of V), so its on resistance is very small (less than 0.1Ω). If M_n is on, T_{r1} is also on because of the base current from the battery V_{BB} . Therefore, in this switch the use is made of the advantages that include a low breakdown voltage *MOSFET*, simple control, a low R_{DS} resistance, and a high speed as well as the advantages of the common-base bipolar

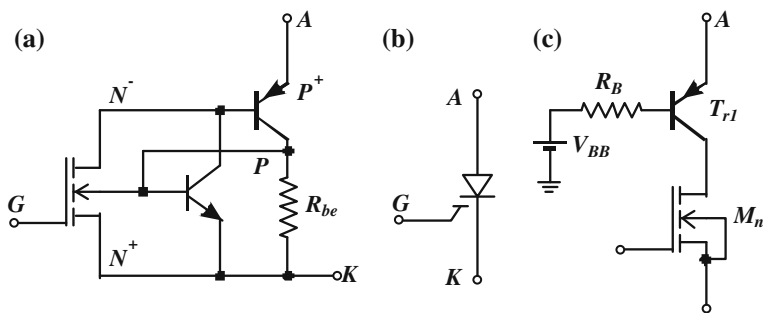


Fig. 2.67 Equivalent circuit (a), symbol of MOS thyristor (b), and emitter BiCMOS switch (c)

transistor (high breakdown voltage and high speed). A serious shortcoming of this switch is that it can be realized only by discrete components. Two transistors are therefore required, one bipolar and one *MOS*.

2.3.3 Static Parameters

The static characteristics of the standard *MOS* transistors (long channel transistors) can be described by the following equations

$$I_D = \beta_n [2(V_{GS} - V_{tn}) V_{DS} - V_{DS}^2], \quad V_{DS} < V_{GS} - V_{tn} \quad (2.217)$$

in the nonsaturated (Ohmic) region, and by

$$I_D = \beta_n (V_{GS} - V_{tn})^2, \quad V_{DS} > V_{GS} - V_{tn} \quad (2.218)$$

in the saturated region (constant current region). V_{tn} is the threshold voltage of the transistor (the gate-source voltage at which the inversion layer, i.e. a channel, is formed). The constant β_n is given by (2.216). The boundary between the saturated and the nonsaturated region is determined by

$$V_{DS} = V_{GS} - V_{tn}. \quad (2.219)$$

Due to a very short length of the channel, the characteristic $I_D = f(V_{DS})$ of power *MOS* transistors is somewhat modified. At small values of the voltage V_{DS} (2.217) applies to a good approximation. In this part the function $I_D = f(V_{DS})$ is almost linear. Since the channel is very short, it is subjected to a very high electric field and the electron mobility is decreased. At a certain critical field K_c the critical speed is reached and after that the drain current is almost constant. The voltage $V_{DSC} = LK_c$, at which the saturation is reached, is lower than the voltage V_{DS} determined by (2.217) except for small values of V_{GS} .

The static output characteristics are shown in Fig. 2.68a. For $V_{GS} < V_{tn}$ the transistor is off. The drain current I_{DSS} is then equal to the reverse saturation current of the diode between the drain and the source. I_{DSS} is of the order of μA and usually can be neglected. The breakdown occurs at a voltage BV_{DS} equal to the breakdown voltage of the mentioned diode. Its value is within limits of several tens of V up to several hundreds of V (500–600 V). The appearance of the second breakdown is possible owing to the parasitic bipolar structure, but this occurs very rarely.

The transfer characteristic $I_D = f(V_{GS})$, at $V_{DS} = \text{const.}$ (Fig. 2.68b), at the beginning of the active region (between the points A and B) is parabolic and afterwards it is approximately linear. Here also the power and the standard *MOS* transistors are different.

The linearity of the function $I_D = f(V_{GS})$ in the saturation region is particularly significant when the *MOS* transistor is used in power amplifiers.

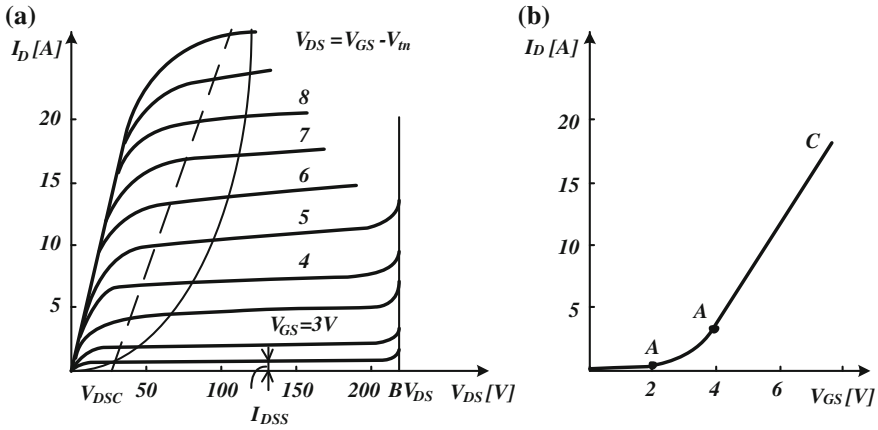


Fig. 2.68 Static characteristics of a power MOS transistor—output (a) and transfer (b)

For the switching functions of the MOS transistor only the cut off and the linear (Ohmic) regions are of interest. When off, the transistor can be replaced by a current generator I_{DSS} (Fig. 2.69a). Typically the threshold voltage V_{tn} is from 2 to 4 V and its temperature coefficient k_t is negative, ranging from 4 to 6 mV/°C. It can, thus, be written that V_{tn} temperature is

$$V_{tn} = V_{tn0} - k_t(T - T_0), \quad (2.220)$$

where T and T_0 are the actual and the room temperature, respectively, and $V_{tn0} = V_{tn}(T_0)$.

The output voltage V_{DS} of a turned-on transistor should be as small as possible. Then, $V_{GS} - V_{tn} \gg V_{DS}$ and the quadratic member in (2.217) can be neglected

$$I_D \approx 2\beta_n(V_{GS} - V_{tn})V_{DS}. \quad (2.221)$$

The constant β_n depends on temperature because electron mobility is a function of temperature

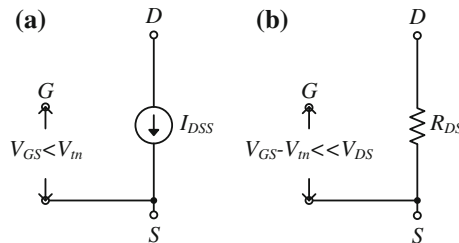


Fig. 2.69 Equivalent circuits of a power MOS transistor in the on (a) and off (b) states

$$\mu_n(T) = \mu_{0n} (T/T_0)^{-n}, \quad (2.222)$$

where n is within limits $1.52 < n < 2.5$, $\mu_{0n} = \mu_n(T_0)$, and T_0 [K] is the room temperature. Now, on the basis of (2.214) and (2.218)

$$\beta_n(T) = \beta_{n0} (T/T_0)^{-n}, \quad (2.223)$$

where $\beta_{n0} = \beta_n(T_0)$. Finally, it turns out that the drain current versus temperature is

$$I_D = 2 \beta_{n0} (V_{GS} - V_{tn0}) V_{DS} (T/T_0)^{-n} \left[1 + \frac{k_t}{V_{GS} - V_{tn0}} (T - T_0) \right]. \quad (2.224)$$

The temperature coefficient of this current is obtained by differentiating (2.224) over T , at $V_{GS} = \text{const.}$ and $V_{DS} = \text{const.}$

After rearrangement one obtains:

$$\frac{dI_D}{dT} = 2 \beta_{n0} V_{DS} \left[\left(1 - n + n \frac{T_0}{T} \right) k_t - \frac{n}{T} (V_{GS} - V_{tn0}) \right]. \quad (2.225)$$

Figure 2.70 shows the function $I_D = f(V_{GS})$ and the normalized temperature coefficient of this current as functions of V_{GS} at different temperatures for $V_{DS} = 0.5$ V. It can be seen that at low values of I_D the temperature coefficient is positive, whereas at higher values of I_D it is negative. The zero temperature coefficient is at V_{GSO} which is obtained by equating (2.225) to zero

$$V_{GSO} = V_{tn} + \frac{T}{n} k_t. \quad (2.226)$$

For instance, for $n = 2$, $k_t = -6$ mV/°C, $V_{tn0} = 2$ V, and at room temperature $T = 300$ K from (2.226) it follows $V_{GSO} = 2.9$ V. In practice, as a rule, when a

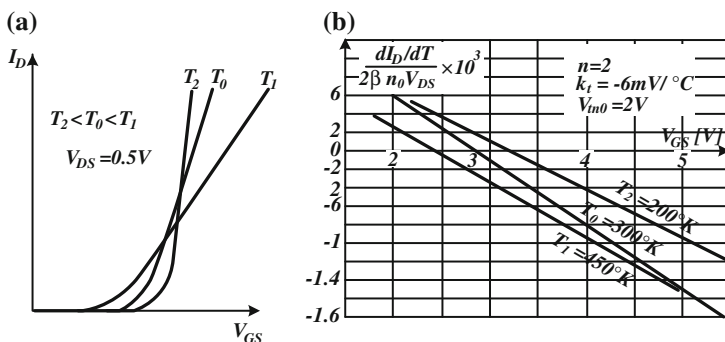


Fig. 2.70 Drain current (a) and normalized temperature coefficient of drain current (b) as functions of V_{GS} at different temperatures according to (2.220) and (2.221), respectively

transistor is on, $V_{GS} \gg V_{GSO}$ and the drain temperature coefficient is negative. This is an important property. Thanks to this, *MOS* components are temperature self-compensating. This means that a positive internal thermal feedback cannot possibly arise which leads bipolar transistors to the secondary breakdown. In other words, *MOS* transistors are not prone to the “thermal run-away”.

The most important parameter of an *MOS* power transistor while conducting is the on resistance, R_{DS} . It consists of several components such as the resistance of the metal and the metal contacts of the source, the resistance of the n^+ regions of the drain and source. Those prevailing, however, are the channel resistance, R_{DL} , and the resistance of the drain region, R_{DD} . Therefore

$$R_{DS} = R_{DL} + R_{DD}. \quad (2.227)$$

Using (2.217), the channel resistance is:

$$R_{DL} = \frac{1}{dI_D/dV_{DS}} \approx \frac{1}{2\beta_n(V_{GS} - V_{tn})} \quad (2.228)$$

and it decreases with increasing V_{GS} . However, the influence of R_{DD} is more important, i.e. $R_{DD} \gg R_{DL}$. This is the resistance of the n -epitaxial layer of the drain, determined by

$$R_{DD} \approx \frac{1}{q\mu_n N_D} \frac{d}{S}, \quad (2.229)$$

where N_D is the donor concentration in the n -layer of the drain, d is the thickness of this layer, and S is the total surface of the *MOSFET*. Since the breakdown voltage BV_{DS} also depends on μ_n and N_D of the epitaxial layer, then also $R_{DD} = f(BV_{DS})$. For instance, for *SGS* power transistors it is approximately

$$R_{DD}(BV_{DS}) = R_{DD}(BV_{DSO}) \left(\frac{BV_{DS}}{BV_{DSO}} \right)^K, \quad (2.230)$$

where the constant K depends on the voltage range of BV_{DS} :

- $K = 1.8$ for low voltage transistors (50–100 V),
- $K = 2.5$ for high voltages (100 up to 500 V) and
- $K = 2.7$ for breakdown voltages greater than 500 V.

BV_{DSO} is the lowest breakdown voltage in the range considered. For *SGS* power *MOS* transistors with breakdown voltages from 500 up to 1000 V

$$R_{DD}(1000 \text{ V}) = R_{DD}(500 \text{ V}) \left(\frac{1000 \text{ V}}{500 \text{ V}} \right)^{2.7} = 7.3 R_{DD}(500 \text{ V}). \quad (2.231)$$

Thus, the resistance R_{DD} , and consequently the resistance R_{DS} increase exponentially with the breakdown voltage. For instance, R_{DS} is typically from several tenths of Ω to several Ω if $BV_{DS} < 100$ V, whereas for transistors having a breakdown voltage in the range of $300 \text{ V} < BV_{DS} < 500$ V this resistance is from several Ω up to 10Ω .

The resistance R_{DS} is highly temperature dependent. Namely, in view of (2.228), (2.229), (2.223), and (2.220) one can write

$$\begin{aligned} R_{DL} &= \frac{1}{2\beta_{n0}(V_{GS} - V_{tn0})} \frac{(T/T_0)^n}{1 + \frac{k_t}{V_{GS} - V_{tn0}}(T - T_0)} = \\ &= R_{DL}(T_0) \frac{(T/T_0)^n}{1 + \frac{k_t}{V_{GS} - V_{tn0}}(T - T_0)}, \end{aligned} \quad (2.232)$$

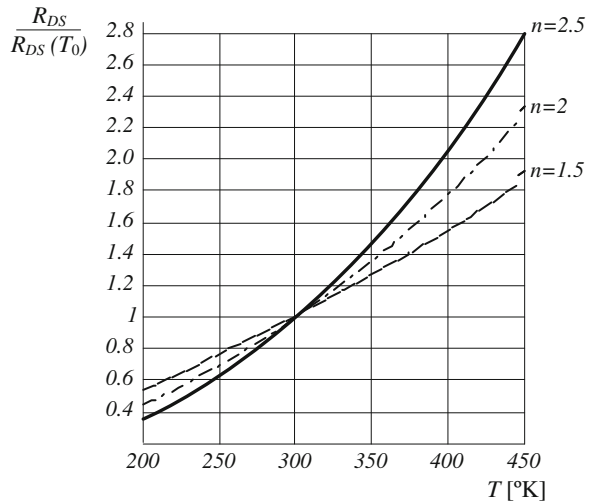
$$R_{DD} = \frac{d}{qN_d S \mu_{n0}} \left(\frac{T}{T_0}\right)^n = R_{DD}(T_0) \left(\frac{T}{T_0}\right)^n. \quad (2.233)$$

Since $k_1(T - T_0)/(V_{GS} - V_{tn0}) \ll 1$, then

$$R_{DS} = [R_{DL}(T_0) + R_{DD}(T_0)] (T/T_0)^n = R_{DS}(T_0) (T/T_0)^n. \quad (2.234)$$

Figure 2.71 shows the normalized drain-source on resistance R_{DS} as a function of temperature for different values of the constant n . For instance, for $n = 2$ an increase of temperature from 300 to 450 K results in the increase of the resistance R_{DS} 2.25 times. It should be emphasized that the voltage V_{DS} of a conducting transistor is almost temperature-independent because R_{DS} increases with temperature and I_D decreases with temperature.

Fig. 2.71 Normalized drain-source on-resistance of an MOS transistor as a function of temperature for $n = 1.5$, $n = 2$, $n = 2.5$ if $T_0 = 300$ K



2.3.3.1 Dynamic Parameters

The parasitic inter-electrode capacitances have a dominant influence on the transient mode of *MOS* switching circuits (Fig. 2.72a). At the places where the metallic electrode of the gate overlaps with the diffused n^+ regions of the source and drain, parasitic capacitances C_{gs} and C_{gd} exist between the gate and the source and between the gate and the drain, respectively. In addition, there is also a capacitance C_{ds} of the reverse biased drain-substrate p-n junction (the source and the substrate of power *MOS* transistors are short circuited). All these capacitances are dependent on the drain-source voltage. Owing to the large surface areas of power transistors, the average values of these capacitances are quite high, typically from a hundred to several hundreds of pF.

For power transistors, the manufacturers give data for the input

$$C_{iss} = C_{gs} + C_{gd}, \quad (2.235)$$

feedback

$$C_{rss} = C_{gd} \quad (2.236)$$

and output capacitance

$$C_{oss} = C_{ds} + C_{gd}. \quad (2.237)$$

The dependencies of these capacitances on voltage V_{DS} are shown in Fig. 2.72b. All this applies only for the static conditions. During transients, however, the input and the output capacitance are increased due to Miller's effect. The transient mode will be analyzed on an example of a switch loaded by a resistor R_D (Fig. 2.73a). It is assumed that the generator with an internal resistance R_g produces a driving voltage V_g , which undergoes step changes.

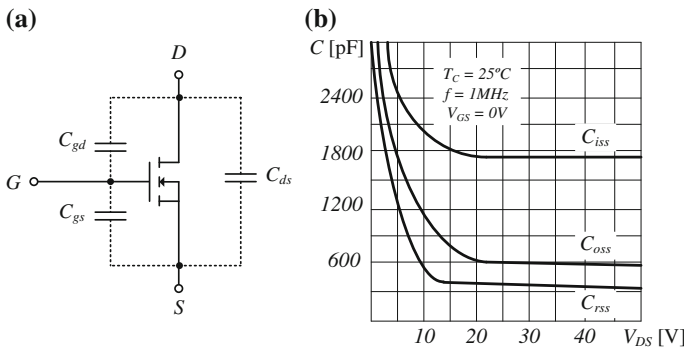


Fig. 2.72 Inter-electrode capacitances (a) and dependencies of input, feedback, and output capacitances on the drain-source voltage (b)

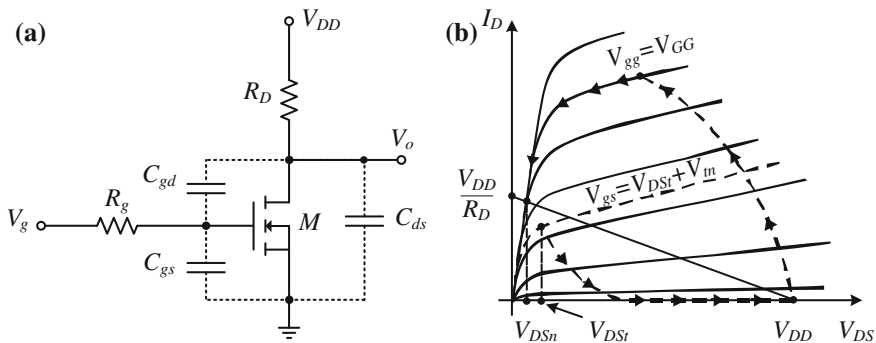


Fig. 2.73 Inverter based on a power MOS transistor (a) and the trajectory of the operating point during transient (b) denoted by dotted lines

The channel of power MOS transistors is very short so that the transition time of the electric charge between the source and the drain is negligible. In other words, this means that the transition mode is determined primarily by the charging and discharging times of the inter-electrode capacitances.

Figure 2.74 shows the pulse waveforms of the responses of the voltages gate-source, drain-source, and drain current to a step-voltage drive. At the instant t_1 when $V_g = V_{GG}$ the input capacitance C_{iss} starts charging,

$$v_{gs}(t) = V_{GG} \left(1 - e^{-\frac{t}{C_{iss}R_g}} \right). \quad (2.238)$$

As long as $V_{GS} < V_{tn}$, the transistor is off, i.e. $I_D = 0$ and $V_{DS} = V_{DD}$. Therefore, there is a delay in the turn-on process of the transistor. From (2.238) and condition $V_{GS}(t_{dr}) = V_{tn}$, it follows that

$$t_{dr} = C_{iss} R_g \ln \frac{V_{GG}}{V_{GG} - V_{tn}}. \quad (2.239)$$

After t_{dr} the drain current increases rapidly. The voltage V_{DS} slowly decreases until the operating point reaches the Ohmic region. Then both the drain current and the drain-source voltage decrease rapidly as the resistance R_{DS} is very small (several tenths of Ω up to several Ω). The trajectory of the operating point in Fig. 2.73b is denoted by dotted lines. Thus, time t_r can be determined from the condition that the voltage drain-source is at the boundary between the active and the saturation region. In practice, however, the approximate expression

$$t_r \approx 2.2 R_g C_{iss}. \quad (2.240)$$

is often used. Upon application of a negative drive at ($t = t_2$), the voltage V_{DS} and the current I_D are changed little. Here too, similarly to bipolar transistors, there exists a delay time, which is not caused by the piled-up charge but by the fact that

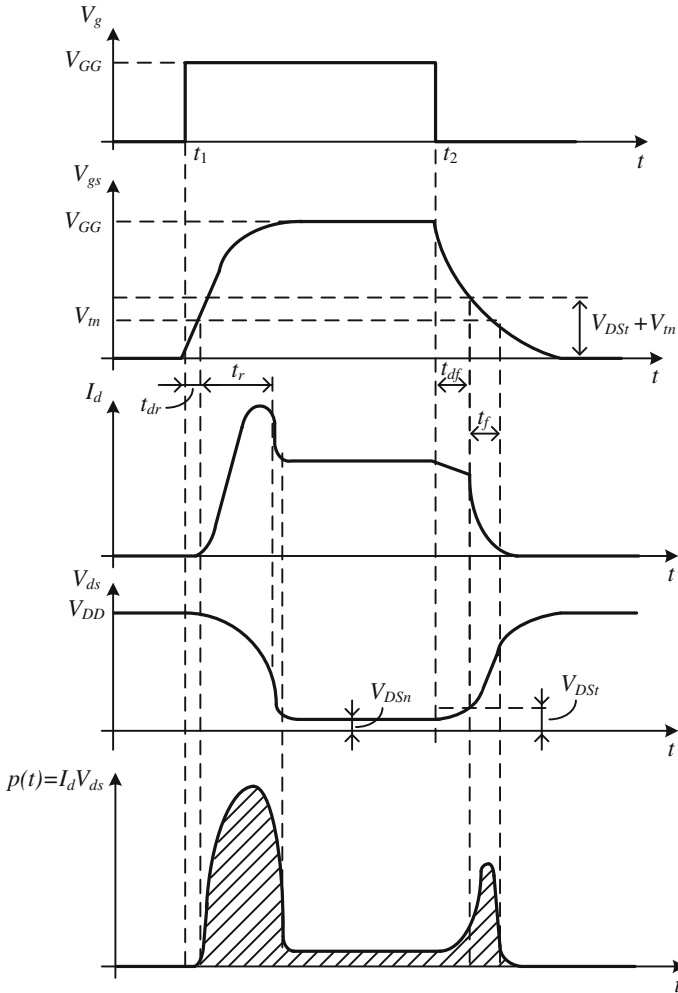


Fig. 2.74 Pulse waveforms of voltages V_{GS} and V_{DS} , current I_D , and dissipation $P(t)$ for a step drive if the internal resistance of the generator is R_g

the transistor remains in the saturated region as long as $V_{DS} < V_{GS} - V_{in}$. Because in that region the characteristic is almost identical for different values of V_{GS} , the current I_D and the voltage V_{DS} will change very little. The delay time t_{df} at the falloff of V_{GS} can be determined from the condition

$$v_{gs}(t_{df}) = V_{GG} e^{-\frac{t_{df}}{C_{iss} R_g}} = V_{DS_t} + V_{in}, \quad (2.241)$$

where V_{DS_t} is the voltage V_{DS} at the boundary between the active and the saturated region. From (2.237) one obtains

$$t_{df} = C_{iss} R_g \ln \frac{V_{GG}}{V_{DSf} + V_{tn}}. \quad (2.242)$$

After t_{df} the current I_D decreases and the voltage V_{DS} increases. When $V_{GS}(t) = V_{tn}$, the transistor is at the turn-on/turn-off threshold, thus $I_D \approx 0$. The falloff time of the drain current is determined by

$$t_f = C_{iss} R_g \ln(1 + V_{DSf}/V_{DSf}). \quad (2.243)$$

After t_f the output capacitance is charged by the load current.

During both delays, t_{dr} and t_{df} , power dissipation in the transistor is small so that these times are not critical. During t_r and t_f power dissipation is significant (Fig. 2.74) and it is important that these times are short. Obviously, the rate of change of the voltage V_{GS} will have a considerable influence on the transient mode. For this reason, one should keep the resistance R_g as low as possible.

If the voltage V_{GS} changed abruptly like V_g ($R_g = 0$), the delay times and t_f would be negligible. The time t_r would be determined by the time of discharging the output capacitance C_{oss} by a large drain current of the transistor in the saturation region.

Finally, it should be emphasized that the waveforms in Fig. 2.74 are approximate and that they illustrate only qualitatively the transient process. Namely, the Miller's effect and the voltage dependencies of the inter-electrode capacitances have not been taken into account. For instance, during t_r and t_f the capacitance C_{gd} due to Miller's effect is transferred to the input with a multiplying factor of $(1 + A_v)$, where $A_v = |dV_{DS}/dV_{GS}|$ is the voltage gain. Then $C_{iss} = C_{gs} + (1 + A_v)C_{gd}$, and its dependence on V_{GS} at $V_{DS} = 5$ V and $V_{DS} = 10$ V is shown in Fig. 2.75.

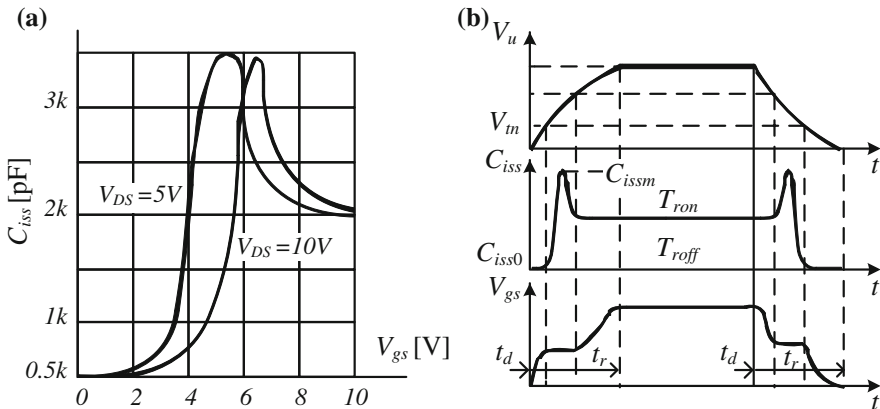


Fig. 2.75 Input capacitance of transistor MTM5N40 as a function of gate-source voltage (a) and real variations of input capacitance and gate-source voltage for an exponential drive (b)

The real variation of the voltage V_{GS} is shown in Fig. 2.75b. Namely, after t_d , the voltage across the capacitor C_{gs} remains for some time almost constant because the input current re-polarizes the feedback capacitance C_{gd} .

Even though the mentioned effects have not been taken into account in the derived equations, they are significant because they indicate the character of the dependence of the transient mode.

2.3.3.2 Driving Circuits

On the basis of the previous analysis, it may be concluded that the drive will be optimal if the following conditions are met:

- the internal resistance of the driving generator is very low,
- the driving generator has a large current capacity so that it can very quickly charge and discharge the input capacitance of the transistor, and
- the voltage of the driving generator V_{GG} is sufficiently high so that the transistor is fully on (the operating point is in the region of constant resistance R_{DS}).

It is difficult to meet all these conditions. The driving circuits are, as a rule, much simpler than they are for bipolar transistors. Since the static input resistance of an *MOS* transistor is very high, it can be driven directly by the output of a *CMOS* buffer (Fig. 2.73). For this purpose, the *CMOS* buffers having equal sink and source currents, like *CD4007*, *CD4041*, and *CD4069*, are recommended. Otherwise, the rise and the fall time of the drive of the power *MOS* transistor will be different.

Here, only the changes of the output voltage $V_o = V_{GS}$ of a *CMOS* buffer-inverter will be considered as their influence on the transient mode of a power transistor is the greatest. The corresponding inter-electrode capacitances are denoted in Fig. 2.76a. Their variations with the voltage V_{DS} will be neglected.

All inter-electrode capacitances can, by means of Miller's theorem, be reduced to the equivalent input and output capacitances (Fig. 2.76b). According to this theorem, if two branches are coupled by a capacitance C , they can be decoupled in such a way that C is referred to the input capacitance C_{e1} and the output capacitance C_{e2} ,

$$C_{e1} = C(1-A_v), \quad C_{e2} = C(A_v-1)/A_v,$$

where A_v is the voltage gain. The total voltage changes at the input and at the output of a *CMOS* inverter are equal, but of the opposite signs, so $A_{v1} = -1$. If the gain of a power transistor is denoted by A_{v2} , one obtains

$$C_I = C_{gsn} + C_{gsp} + 2(C_{gdn} + C_{gdp}) \quad \text{and} \quad (2.244)$$

$$C_O = C_{dsn} + C_{gsp} + 2(C_{gdn} + C_{gdp}) + C_{gs} + (1 + |A_v|) C_{gd}. \quad (2.245)$$

The capacitances of a *CMOS* transistor are at least two orders of magnitude lower, thus their influence on the transient mode can be neglected. Therefore,

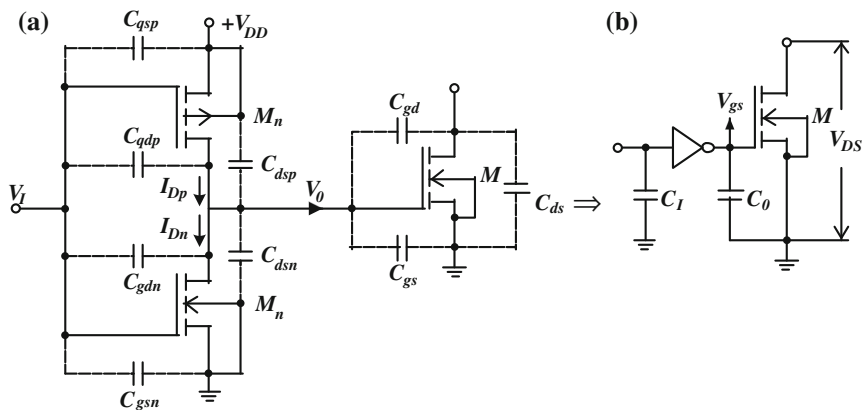


Fig. 2.76 CMOS inverter driving circuit (a) including the parasitic capacitances and the equivalent circuit for analyzing the transient mode (b)

$$C_O \approx C_{gs} + (1 + |A_v|) C_{gd} . \quad (2.246)$$

On the other hand, the charging and discharging times of the input capacitance C_I can also be neglected. This means that the gate voltage of a CMOS inverter will be abrupt if the input voltage change V_I is abrupt. In this case, the trajectory of the operating point of a CMOS inverter during transient mode is as shown in Fig. 2.77a.

While $V_I = 0$ ($t < t_1$) M_n is off and M_p is on, so $V_O = V_{GS} = V_{DD}$. At $t = t_1$ M_p is switched off and M_n is switched on. Practically, it may be considered that the channel of the PMOS transistor is instantaneously cut off, and $I_{Dp} = 0$. The capacitor C_O is being discharged by the current of the NMOS transistor, and

$$V_{gs} = V_{DD} - \frac{1}{C_i} \int_0^t I_{dn} dt \quad (2.247)$$

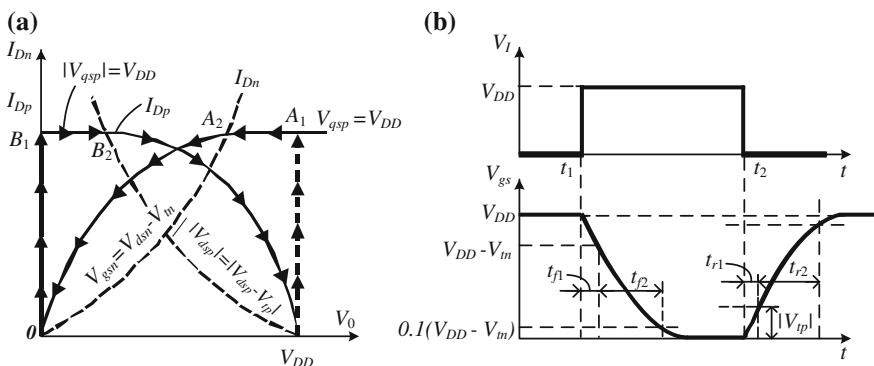


Fig. 2.77 Trajectory of the operating point of a CMOS inverter (a) and its output voltage (b) for a step input drive

At $t = t_1 + 0$ the operating point is in the position A_1 (Fig. 2.77a). Thus, M_n is in the saturated region and

$$I_{dn} = \beta_n (V_{DD} - V_{tn})^2. \quad (2.248)$$

From (2.243) and (2.244) it follows that

$$V_{gs} = V_{DD} - \frac{\beta_n (V_{DD} - V_{tn})^2}{C_o} t. \quad (2.249)$$

This variation of the voltage V_{GS} proceeds during the time t_{f1} , while M_n is in the saturated region (between points A_1 and A_2). This time is determined from the condition:

$$V_{gs}(t_f) = V_{DD} - V_{tn} \quad (2.250)$$

and the Eq. (2.245).

Finally,

$$t_{f1} = \frac{C_o}{\beta_n (V_{DD} - V_{tn})} \frac{V_{tn}}{V_{DD} - V_{tn}}. \quad (2.251)$$

For $t > t_{f1}$ M_n is in the nonsaturated region, and:

$$V_{gs}(t) = V_{DD} - V_{tn} - \frac{\beta_n}{C_o} \int_0^t [2(V_{DD} - V_{tn}) V_{gs} - V_{gs}^2] dt \quad (2.252)$$

Upon differentiation of (2.248), after the separation of the variables V_{GS} and t and reintegration, it follows that

$$V_{gs}(t) = \frac{2(V_{DD} - V_{tn})}{1 + e^{t/\tau_n}}, \quad (2.253)$$

where the time constant is

$$\tau_n = \frac{C_o}{2 \beta_n (V_{DD} - V_{tn})}. \quad (2.254)$$

The transient mode ends when the capacitor C_o is fully discharged ($V_{GS} = 0$). Theoretically this implies an infinite time. For this reason, the practical condition for the completion of the transient mode is when the voltage across the capacitor reaches 10 % of the voltage at the start of the considered interval, i.e.,

$$V_{gs}(t_f) = 0.1(V_{DD} - V_{tn}). \quad (2.255)$$

From (2.253) and (2.255), it follows that

$$t_{f2} = 2.9 \tau_n. \quad (2.256)$$

The total fall time of V_{gs} is $t_f = t_{f1} + t_{f2}$. In view of (2.251) and (2.256)

$$t_f = 2\tau_n \left(1.45 + \frac{V_{tn}}{V_{DD} - V_{tn}} \right). \quad (2.257)$$

From $t = t_2$, when again $V_1 = 0$, the process of charging of C_O starts, but this time by the current I_{Dp} of the transistor M_p . Namely, it may be assumed that M_n is off instantaneously, and

$$V_{gs}(t) = V_{co} + \frac{1}{C_i} \int_0^t I_{dp} dt \quad (2.258)$$

where $V_{Co} = V_{GS}(t_2 - 0) = 0$ is the initial voltage across the capacitor C_o . The operating point follows the trajectory $O - B_1 - B_2 - V_{DD}$ (Fig. 2.77a). Thus, the rise time of the voltage V_{GS} consists of two-time intervals, t_{r1} and t_{r2} . During the first interval, M_p is saturated and

$$I_{dp} = \beta_p (V_{DD} + V_{tp})^2. \quad (2.259)$$

Now, on the basis of (2.258) and (2.259) and from condition $|V_{DSp}| = |V_{GSp} - V_{tp}|$ or $V_{GS}(t_{r1}) = |V_{tp}|$, there follows:

$$t_{r1} = \frac{C_O}{\beta_p (V_{DD} + V_{tp})} \frac{|V_{tp}|}{V_{DD} + V_{tp}}. \quad (2.260)$$

During the interval, t_{r2} M_p is in the active region, so

$$I_{dp} = \beta_p [2(V_{DD} + V_{tp})(V_{DD} - V_{gs}) - (V_{DD} - V_{gs})^2]. \quad (2.261)$$

On the basis of (2.258) and (2.259) and with the initial condition $V_{Co} = V_{GS}(t_{r1}) = |V_{tp}|$ one obtains

$$V_{gs} = V_{DD} - 2 \frac{V_{DD} + V_{tp}}{1 + e^{t/\tau_p}}, \quad (2.262)$$

where

$$\tau_p = \frac{C_O}{2 \beta_p (V_{DD} + V_{tp})}. \quad (2.263)$$

According to (2.262) the steady state, when $V_{gs} = V_{DD}$, will be reached after an infinite time. For this reason, t_{r2} will be determined using a practical condition, according to which

$$V_{DD} - V_{gs}(t_{r2}) = 0.1(V_{DD} + V_{tp}). \quad (2.264)$$

Thus, like in the case of the determination of t_{f2} , t_{r2} is the interval during which the operating point completes 90 % of the trajectory while M_p is in the active region. Now, from (2.262) and (2.264)

$$t_{r2} = 2.9\tau_p. \quad (2.265)$$

The total rise time $t_{r1} + t_{r2}$ is thus

$$t_r = 2\tau_p \left(1.45 + \frac{|V_{tp}|}{V_{DD} + V_{tp}} \right). \quad (2.266)$$

If the CMOS transistors are symmetrical, i.e., $\beta_n = \beta_p$ and $V_{tn} = |V_{tp}|$, then $\tau_n = \tau_p$ and $t_f = t_r$. Typical for the CD4000 series of CMOS integrated circuits is that $V_{tn} = |V_{tp}| = 1.5$ V and the supply voltage is within limits $3 \text{ V} < V_{DD} < 18 \text{ V}$. The practical values are, however, $V_{DD} > 5 \text{ V}$. Now, the rise and the fall time are:

$$t_r = k_{vp} \tau_p, \quad t_f = k_{vn} \tau_n, \quad (2.267)$$

where the constants k_{vn} and k_{vp} depend on V_{DD} and range from 3.1 up to 3.75. The denominators in (2.254) and (2.263) are respectively equal to the reciprocal values of the channel resistance of NMOS and PMOS transistors in the active region. Therefore, it can be written that

$$t_f = k_{vn} C_O R_{DSN}, \quad t_r = k_{vp} C_O R_{DSP}. \quad (2.268)$$

The manufacturers give the output currents I_{DSN} and I_{DSP} for certain values of V_{DSN} , V_{DSP} , and V_{DD} . Most often $V_{DSN} = |V_{DSP}| = 0.5 \text{ V}$. On this basis, one can calculate the approximate values of the resistances R_{DSN} and R_{DSP} . Namely

$$R_{DSN} \approx V_{DSN}/I_{DSN}, \quad R_{DSP} \approx V_{DSP}/I_{DSP}. \quad (2.269)$$

Thus, e.g. for CMOS inverters CD4069 at $V_{DD} = 10 \text{ V}$ and $V_{DSN} = |V_{DSP}| = 0.5 \text{ V}$, $I_{DSN} = |I_{DSP}| = 2.6 \text{ mA}$, and

$$t_f = t_r = 3.6 C_O * 0.5 / 2.6 \approx 0.7 C_O [\text{ns}]; C_O \text{ in } [\text{pF}].$$

On the basis of the previous simple expressions the rise and the fall time of the gate-source voltage of a power MOS transistor can easily be calculated. If the reduction

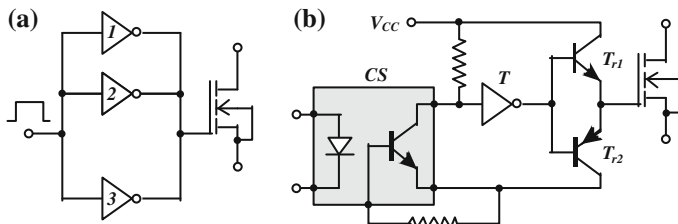


Fig. 2.78 Driving circuit for M CMOS inverters (a) and for a complimentary pair of bipolar transistors (b) when galvanically separated from the control circuit by an opto-coupler

of these times is required, two alternatives (Fig. 2.78) are recommended. In the first instant, the M inverters are connected in parallel. Then, the transistor resistances and times t_r and t_f are also M times lower, i.e.,

$$t_f = k_{vn} C_O \frac{V_{DSN}}{M I_{DSN}}, t_r = k_{vp} C_O \frac{V_{DSP}}{M I_{DSP}} \quad (2.270)$$

In the second alternative (Fig. 2.75b), a complimentary pair of these transistors is used. The current gains of these transistors should be as high as to ensure faster charging or discharging of the capacitor C_O . The method of galvanic isolation of the control circuit of the DC/DC converter from the driving circuit is also shown (Fig. 2.75b). The isolation is carried out by an opto-coupler (OC). Pulse transformers are also used for this purpose. The Schmitt trigger reshapes the pulses of the opto-coupler output and filters out the slow-varying noise components. Thanks to the regenerative character of the Schmitt trigger operation the drive of the bipolar transistors as a function of time is almost ideal.

Example 2.5 Compare the dynamic characteristics of the switch from Fig. 2.73a with those from Fig. 2.79 for the same excitation using PSPICE software package. The supply voltage is $V_{DD} = 100$ V, $\beta_n = \beta_p = 100$ and the excitation voltage is the pulse with an amplitude 15 V, frequency 50 kHz and $R_g = 100 \Omega$.

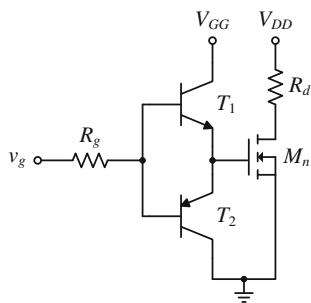


Fig. 2.79 Inverter with MOS transistor and a pair of complementary bipolar transistors in excitation circuit

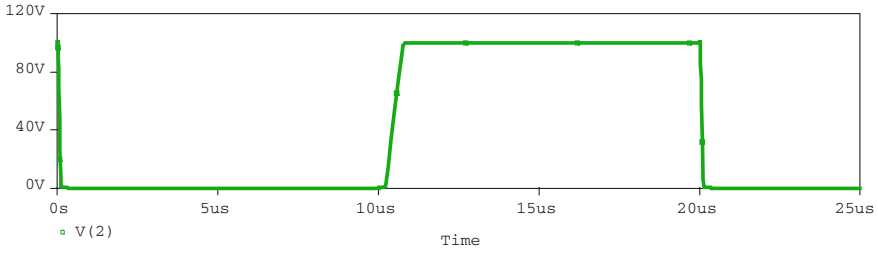


Fig. 2.80 Waveform of output voltage for a switch with MOS transistor and a circuit to speed up transition processes

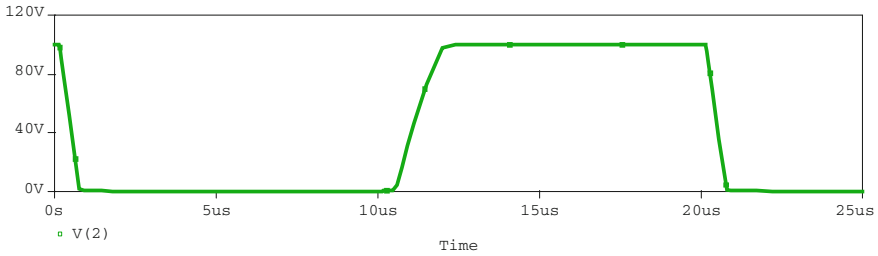


Fig. 2.81 Waveform of output voltage for a switch with MOS transistor and without circuit to speed up transition processes

- (a) Comparison of dynamic characteristics of the switch from Fig. 2.73a with those from Fig. 2.79 for the same excitation and using PSPICE software package are presented in Figs. 2.80 and 2.81.

2.3.4 Safe Operation Area

In the course of transistor selection, care must be taken that the operating point does not leave the safe operation area. Like in the case of the bipolar transistors this area is limited by the breakdown voltage, the maximum current, the permitted dissipation and, for MOS transistors also by the maximum on resistance (Fig. 2.82).

The maximum drain voltage is determined by the drain-source breakdown voltage BV_{DS} when the gate and source are short circuited. As already mentioned, the secondary breakdown is a rare phenomenon in MOS transistors. Also, care must be taken with the maximum gate voltage BV_{GS} even though this parameter is not included in the *SOA* definition. BV_{GS} is the breakdown voltage of the gate oxide that results in a permanent damage to the transistor. The thickness of the oxide is around $0.1\ \mu\text{m}$ and the gate breakdown voltage is $20\ \text{V} < BV_{GS} < 40\ \text{V}$. In low power transistors, a Zener diode is built into protect the gate against breakdown.

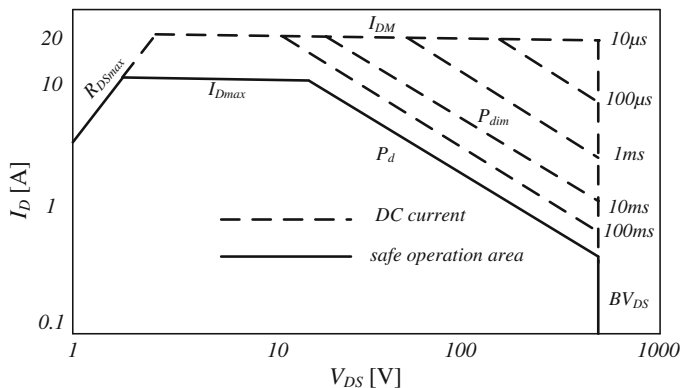


Fig. 2.82 Safe operation area of a power MOSFET

The gate-source capacitance of MOS transistors intended for currents of several A and higher is large (from several hundreds to several thousands pF) so that these devices do not need a Zener diode. Practical experience, however, shows that the gate breakdown is the most frequent cause of failure. For this reason, an external protection of the gate by fast diodes is recommendable. This is particularly relevant for circuits likely to undergo fast variations of currents and voltages with significant amplitudes (spikes). It is good practice that the driving circuit is sufficiently powerful in order to be able to share the load of possible “spikes”.

The maximum drain current is limited by the maximum junction temperature and depends on the case temperature T_c , or on the power of dissipation P_d and the cooling efficiency. The junction temperature can be written as:

$$T_j = T_c + R_{jc} P_d, \quad (2.271)$$

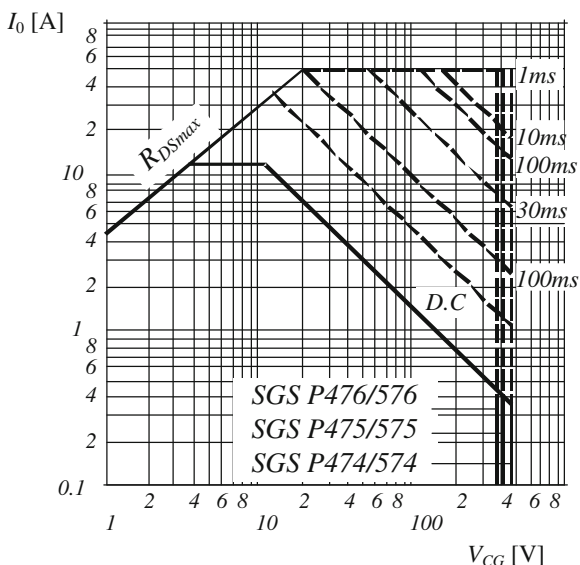
where R_{jc} is the junction-case thermal resistance. Since the power of dissipation in a transistor is $P_d = I_D^2 R_{DS}$, the maximum transistor current is

$$I_{Dmax} = \sqrt{\frac{T_{jmax} - T_c}{R_{DS} R_{jc}}}. \quad (2.272)$$

In the pulse mode of operation, the maximum current is increased because the temperatures of the crystal and the case are decreased.

The maximum dissipation is limited by the thermal stability. Namely, the greatest losses are in the resistance R_{DS} . As shown (Fig. 2.71), this resistance increases exponentially with temperature. Due to this dissipation increases and it is possible that, if cooling is not properly designed, a thermal instability may occur causing junction burn up. In the pulse mode, the permitted dissipation depends upon the duty cycle. For shorter pulses, the permitted dissipation is higher (Fig. 2.83).

Fig. 2.83 Safe operation areas of power VDMOS transistors manufactured by SGS



The maximum value of the resistance R_{DS} also limits the safe operation area. This limitation becomes significant at high drain currents and it is proportionally less significant as R_{DS} is lower.

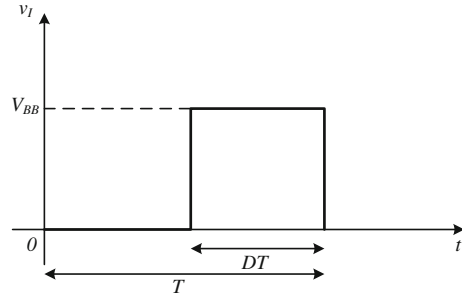
Figure 2.83 shows the operating areas of three types of power MOS transistors manufactured by SGS. The differences are only in the values of breakdown voltages.

It should be emphasized that the catalogue data on SOA curves are not very reliable in practical applications. First of all, they do not include limitations due to the gate voltage. They also do not take into account the speeds of the current or voltage changes, etc. The restrictions given are primarily the boundaries beyond, which the reliable operation of the device cannot be guaranteed. In any specific case, the designer should determine the safe operation area taking into account the device ratings and the peculiarities of the application.

Problems

- 2.1 It is known that $\alpha_F = 0.99$, $\alpha_R = 0.01$, $BV_{CBO} = 80$ V and $n = 4$. Determine the breakdown voltage of a bipolar transistor with ZE, if:
 - (a) both p-n junctions are reversely biased,
 - (b) the base is broken, and
 - (c) the base and the emitter are short-circuited.
- 2.2 For the circuit from Fig. 2.48a determine the minimum value of resistance R in the circuit to avoid transistor breakdown. The parameters of the circuit are: $V_{CC} = 15$ V, $BV_{CBO} = 60$ V, $L = 10$ mH, $f = 20$ kHz, $V_{CES} = 0.2$ V and $D = 0.5$. Assume that the transistor turn off time is much shorter than the time constant L/R_0 . The transistor excitation signal is shown in Fig. 2.84.

Fig. 2.84 Excitation signal for the circuit from Fig. 2.48a



2.3 For the circuit from Fig. 2.48a determine:

- (a) the required on time of the switch for which the peak energy stored in the inductor is 1 J, and
- (b) the value of the resistance R_0 connected in a series with the diode D to obtain a switching frequency of 100 kHz.

The circuit has $V_{CC} = 12$ V and $L = 10$ mH. Assume that the transistor and the diode are ideal.

- 2.4 Design the turn off snubber circuit shown in Fig. 2.49a if $V_S = 150$ V, $I_L = 10$ A and $t_f = 0.6$ μ s. The switching frequency is $f = 100$ kHz, and the duty factor is $D = 0.4$. The voltage on the switch should reach V_S , when the current through the switch reaches 0. A time equal to 5 time constants is necessary to discharge the capacitor when the switch is closed.
- 2.5 For the circuit from Fig. 2.60 determine the resistance R_B so that $I_{D1} = 2I_{D2}$ in steady state if $V_{CC} = 60$ V, $R_C = 50$ Ω , $\beta = 20$ and $V_{pn} = 0.7$ V. The excitation signal is a pulse with an amplitude of 10 V.
- 2.6 Determine the turn on time for the switch from Fig. 2.73 if $C_{iss} = 5$ nF, $V_{CC} = 80$ V, $R_D = 10$ Ω and $R_g = 100$ Ω . The excitation signal is a pulse with $V_{GG} = 15$ V.
- 2.7 Determine the turn off time for the switch from Fig. 2.79 if the supply voltage is $V_{DD} = 100$ V, $\beta_n = \beta_p = 100$ and the excitation voltage is a bipolar pulse with an amplitude of 15 V, frequency 50 kHz and $R_g = 100$ Ω .

Chapter 3

Regenerative Switches

A special group of semiconductor switches are those comprising elements with such properties that each change of state is accompanied by positive feedback, or by a regenerative (cumulative) process. Their static I–V characteristic has the shape of the letter “S” (Fig. 3.1), so they are often called the “S” elements. Their $I = f(V)$ function consists of three distinct regions. In the first region, specified by $V < V_p$ and $I < I_p$, the switch is off and this is the high-resistance region. P is the breaking point and its coordinates are the breakpoint voltage V_p and the current I_p . The breakpoint current is the lowest current for which $dV/dI = 0$. The third region is the low-resistance region and it is specified by $I > I_v$ and $V_v < V < V_p$. V is the lowest point of the characteristic. V_v and I_v are the minimum voltage and the minimum current, respectively. I_v can be defined as the minimum current for which $dV/dI = 0$.

The region of negative differential resistance is between the points P and V , since a current increase is accompanied by a corresponding decrease of the voltage. This is the region of instability and the operating point cannot remain in it. Namely, at the points P and V , where $dV/dI = 0$, the regenerative process supporting the change of the state of the switch is initiated. Thus, each change of state from the region I to the region III and vice versa is accompanied by a regenerative (cumulative) process.

In the analysis of the circuits containing the regenerative switches, the I–V characteristic is usually approximated by linear segments in each region (Fig. 3.2). Figure 3.2 also shows the corresponding equivalent circuits of the switch in the stable regions (I and III). The resistances R_1 and R_2 in the off and on (saturation) states are determined by the slopes of the linear segments in the corresponding regions.

The resistance of the switch in the off state is defined as

$$R_I = \frac{V_p}{I_p - I_I}, \quad (3.1)$$

where I_I is the current of the switch at $V = 0$. Usually this current is negative and is often called the reverse current. Its value varies from switch to switch from several nA to several tenths of μA . The resistance R_1 ranges from 100 k Ω to 100 M Ω . Since, as a rule, regenerative switches are very powerful (currents in the on state

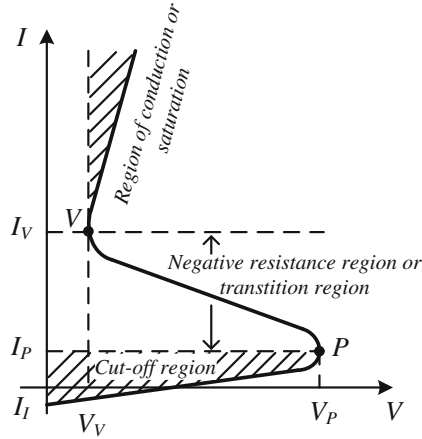


Fig. 3.1 Static characteristic of a regenerative switch

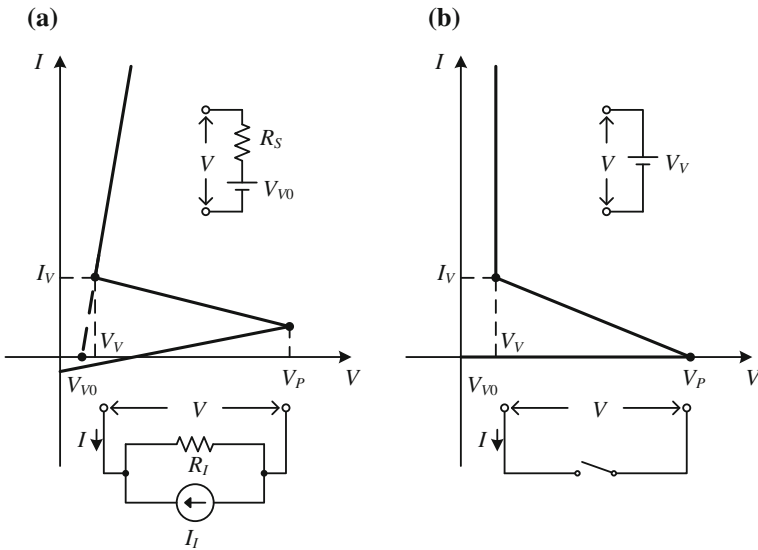


Fig. 3.2 Linearized characteristics and the corresponding equivalent circuit for a regenerative switch (a, b)

reach 100 A), R_1 and I_1 can usually be neglected. Then, the switch can be considered open and its characteristic in the open state coincides with the “ V ” axis (Fig. 3.2b).

The resistance of the switch in the on state is defined as

$$R_S = (V_V - V_{V0})/I_V, \quad (3.2)$$

where V_{V0} is the minimum conduction voltage (for the conduction current $I = 0$) (Fig. 3.2a). The equivalent circuit of the switch is made of a series connection of the resistance R_S and the voltage generator V_{V0} (Fig. 3.2a). Usually $V_{V0} \approx V_V$ and the corresponding linear segment are vertical with respect to the “ V ” axis (Fig. 3.2b). Practically, the resistance R_S is within the limits of several tenths of Ω to 10 Ω and can be neglected. This means that a switch in the on state can be replaced by a voltage generator V_V (Fig. 3.2b). The voltage V_V is typically 1 V, seldom (2–3) V as it is for unijunction transistors.

3.1 Unijunction Transistor

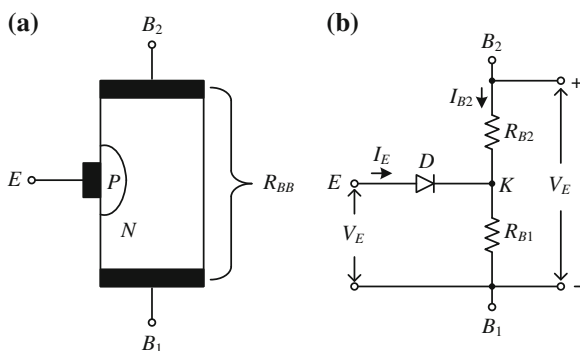
The unijunction transistor, or UJT, is one of the oldest semiconductor elements. Compared to the standard transistor a UJT has only one p-n junction. Cross-sections of some early designs are shown in Fig. 3.3a. The substrate is n -type semiconductor containing a low concentration of impurities. At two ends of the substrate there are metallic contacts of the bases B_1 and B_2 . Approximately halfway, somewhat closer to the base B_2 , a heavily doped p -type emitter region is diffused. Since, there is only one p-n junction (like in a diode) and two bases, in the early days it was often called the two-base diode.

The principle of operation and the basic characteristics of UJT will be described using the model Fig. 3.3b. The diode replaces the p-n junction and R_{B1} and R_{B2} are the respective resistances between the base contacts and the p-n junction. The total resistance of the n -type substrate between the base contacts is

$$R_{BB} = R_{B1} + R_{B2} \quad (3.3)$$

typically 5–10 k Ω .

Fig. 3.3 Cross-section (a) and model of unijunction transistor (b)



The input static characteristic $I_E = f(V_E)$ will be analyzed first. The supply voltage is fed between the two bases so $V_{B1B2} > 0$. If $V_E = 0$, the diode D is reverse biased because the cathode voltage is

$$V_k = R_{B1} \frac{V_{B2B1}}{R_{BB}}. \quad (3.4)$$

The input current is equal to the reverse saturation current of the diode, i.e., $I_E = -I_{EO}$ and, depending on the UJT type, it ranges from several tens of nA to 10 μ A. Now, let V_E increase. As long as the diode does not turn-on, its I - V characteristic is the input characteristic of the UJT in the off state. At $V_E = V_K$ the input current is $I_E = 0$. When the input voltage becomes higher than V_K by the threshold voltage of the diode V_{Dt} , the diode starts conducting. The holes from the p -type region of the emitter are injected into the n -type region of the substrate. Since, $V_{B2B1} > 0$, the electric field in the n -type substrate directs holes toward the base B_1 . Owing to this in the region of B_1 free electrons are generated in order to preserve the charge neutrality. The conductivity of the semiconductor material is given by

$$\sigma = q(n\mu_n + p\mu_p), \quad (3.5)$$

where $q = 1.6 \times 10^{-19}$ (C) is the electron charge, μ_n and μ_p are the respective electron and hole mobilities. Since, direct polarization of the p-n junction increases the electron and hole concentrations in the B_1 region, the conductivity of the region increases and the resistivity R_{B1} decreases. Owing to this V_K decreases and the voltage across the diode increases. This leads to an enhanced injection of holes from the p -type region and a further decrease of the resistance R_{B1} . The resulting process of resistivity modulation has a regenerative character. Since, the voltage V_K decreases while the input current increases, the input static characteristic in that region have a negative differential resistance. The regenerative process ends with R_{B1} in saturation. Namely, owing to the increased concentrations of electrons and holes their mobilities are reduced, and after a certain period of time an equilibrium is established between the increasing concentrations n and p and the decreasing mobilities μ_n and μ_p . The modulation of resistivity is thus completed. Further on the resistivity remains constant, with a value ranging from several Ω up to several tens of Ω . Now UJT is conducting and its input characteristic $I_E = f(V_E)$ are close to the characteristic of the conducting emitter-base diode B_1 with base B_2 open ($I_{B2} = 0$).

The regenerative process is thus initiated by the start of the diode conduction when $dV/dI = 0$ (point P in Fig. 3.4a). Therefore, the breakpoint voltage is

$$V_P = V_K + V_{Dt} = \eta V_{B2B1} + V_{Dt}, \quad (3.6)$$

where

$$\eta = R_B \frac{1}{R_{BB}} = R_B \frac{1}{R_{B1} + R_{B2}} \quad (3.7)$$

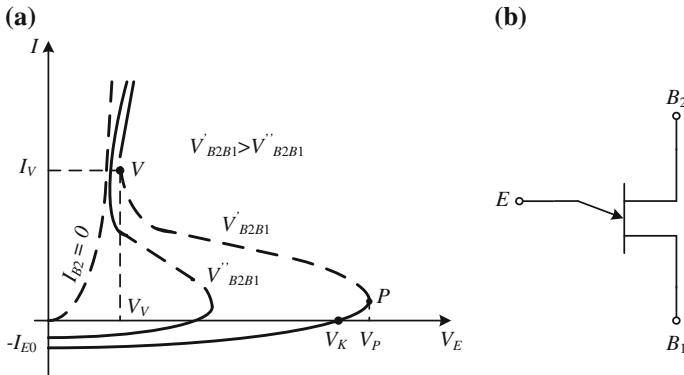
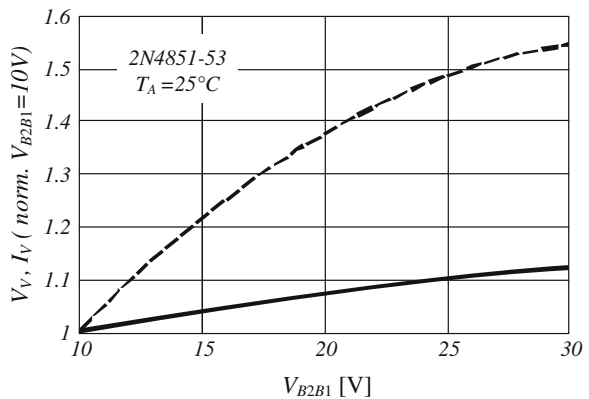


Fig. 3.4 Static characteristic (a) and symbol of the unijunction transistor (b)

Fig. 3.5 Normalized I_V and V_V as functions of base-to-base voltage V_{B2B1}



is the resistance ratio ranging from 0.4 to 0.8. The breakpoint current I_P is typically several hundreds of nA up to 10 μA (Fig. 3.5).

As previously stated, the I_E - V_E characteristics of UJT in the saturation region are almost as the I - V characteristic of the E - B_1 diode with $I_{B2} = 0$. UJT will remain in this region as long as the current I_E does not drop to the minimum conduction current I_V . Then the process of regenerative modulation of the resistivity of base B_1 restarts. For $I_E = I_V$, due to the reduction of emitter current, the concentrations n and p have dominant influence on the resistance R_{B1} . Since now the concentrations n and p are decreasing, R_{B1} will increase. Owing to this the voltage V_K increases and the current I_E decreases still more. The process ends with the reverse biased diode D and the re-established value of R_{B1} of the UJT in the cut off region. The range of values of the current I_V is from several hundreds of μA to 10 mA and the minimum conduction voltage V_V is typically 2–3 V. Both I_V and V_V are dependent on the base-to-base voltage V_{B2B1} . For instance, for UJT type 2N4851-51 an increase of the base-to-base voltage from 10 to 30 V causes the minimum conduction current I_V to rise by a factor of 1.55.

The static I–V characteristic and the symbol of UJT are shown in Fig. 3.4. The part of this characteristic in the region of negative differential resistance is shown by dotted lines because this is the unstable region, i.e., the operating point is fleeting. At the edges of this region the regenerative process of the resistivity modulation is initiated. When UJT is cut off, this process arises at $V_E = V_P$ and UJT is on when $I_E = I_V$. Consequently, the basic parameters of a UJT are the breakpoint voltage V_P and minimum conduction current I_V .

3.1.1 Temperature Characteristics

The reverse emitter current I_{EO} and the reverse saturation current of the diode increase with temperature. The temperature characteristics of both the current I_V and the voltage V_V for a UJT type 2N4851-3 (Fig. 3.6) are decreasing functions of temperature.

The breakpoint voltage is also temperature dependent. The constant η decreases with temperature. Since, temperature variations of R_{B1} and R_{B2} are approximately the same, the temperature coefficient of the constant η is by more than one order of magnitude smaller than the corresponding coefficient of the resistance R_{BB} and usually it can be neglected. Thus, from (3.6) it follows

$$\frac{dV_P}{dT} \approx \frac{dV_{Df}}{dT} < 0 \quad (3.8)$$

Therefore, V_P decreases with temperature. Manufacturers of UJT quote that (3.8) is approximately $-2.7 \text{ mV}/^\circ\text{C}$.

Since, the functional parameters of the circuits using UJT are most sensitive to variations of V_P , this voltage should be temperature stabilized. The standard practice is to add a resistance R (Fig. 3.7). Now

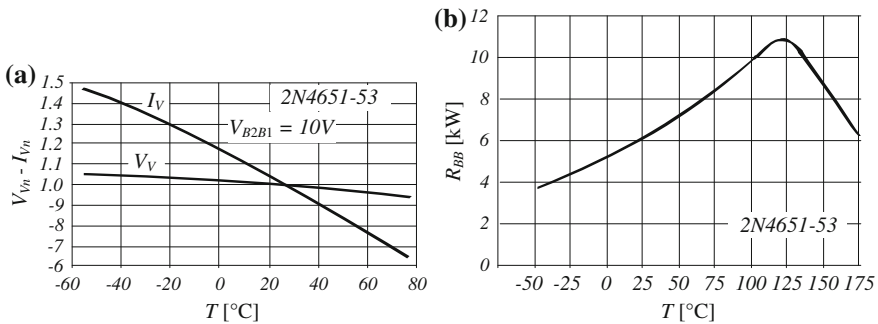


Fig. 3.6 I_V and V_V normalized at $T = 25^\circ\text{C}$ as functions of temperature at $V_{B2B1} = 10 \text{ V}$ (a) and base-to-base resistance R_{BB} of UJT 2N4851-3 as function of temperature (b)

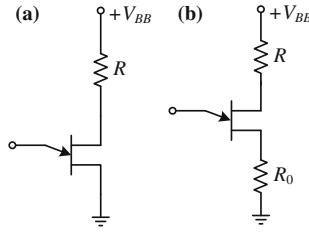


Fig. 3.7 Practical UJT circuits for breaking voltage stabilization (a) and limitation of current I_E in the state of conduction (b)

$$V_p = \eta \frac{V_{BB}}{1 + R/R_{BB}} + V_{Dt}. \quad (3.9)$$

Over the temperature range -55 to $+125$ °C the resistance R_{BB} varies approximately linearly (Fig. 3.6b) and can be expressed as

$$R_{BB}(T) = R_{BB}(T_0)[1 + (T - T_0)\alpha_r], \quad (3.10)$$

where T_0 is the room temperature. The temperature coefficient α_r is approximately 8×10^{-3} (°C $^{-1}$). Therefore, R/R_{BB} reduces, the first member in (3.9) increases with temperature and it could compensate the negative variation of 8×10^{-3} (°C $^{-1}$) voltage V_{Dt} .

If one assumes that η , V_{BB} , and R are temperature independent, by differentiating (3.9) in terms of T , one obtains

$$\frac{dV_p}{dT} = \frac{\eta V_{BB}}{(1 + R/R_{BB})^2} \frac{R}{R_{BB}^2} \frac{dR_{BB}}{dT} + \frac{dV_{Dt}}{dT}. \quad (3.11)$$

In practice it is always $R \ll R_{BB}$. By equating (3.11) to zero, one obtains the resistance R which results in a complete temperature compensation of the breakpoint voltage V_p

$$R \approx -\frac{dV_{Dt}/dT}{\alpha_r} \frac{R_{BB}}{\eta V_{BB}}. \quad (3.12)$$

Let $dV_{Dt}/dT = -2.7$ mV/°C and $\alpha = 8 \times 10^{-3}$ (°C $^{-1}$). Then

$$R \approx 0.34 \frac{R_{BB}}{\eta V_{BB}}. \quad (3.13)$$

The practical values of the resistance R range from several hundreds Ω up to 1 k Ω .

In order to limit the emitter current when the UJT is turned on, a resistance R_0 is inserted in the circuit of the base B_1 (Fig. 3.7b). Typical values of this resistance are from several tens of Ω up to 100 Ω . In this case the breakpoint voltage is

$$V_p = \eta V_{BB} \frac{1 + R_0/R_{B1}}{1 + (R + R_0)/R_{BB}} + V_{Dr}. \quad (3.14)$$

By assuming that the temperature coefficients of R_{B1} and R_{B2} are equal and that $R + R_0 \ll R_{BB}$, the resistance R_i at which $dV_p/dT = 0$ is determined by the equation

$$R = \frac{1 - \eta}{\eta} R_0 - \frac{dV_{Dr}/dT}{\alpha_r} \frac{R_{BB}}{\eta V_{BB}}. \quad (3.15)$$

Therefore, when R_0 is used, the resistance R should be increased by a factor $R_0(1 - \eta)/\eta$.

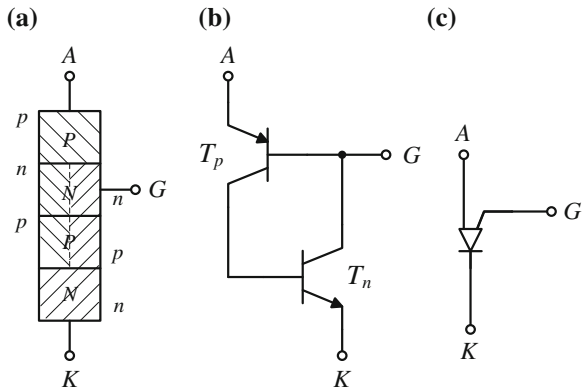
3.1.2 Programmable Unijunction Transistor

The programmable unijunction transistor (PUT) is a regenerative switch having adjustable (programmable) basic parameters. It belongs to the group of four-layer structures (Fig. 3.8a), but its static characteristics and applications are identical to those of the UJT. It can be modeled by a pair of complimentary bipolar transistors (Fig. 3.8b). The notation of terminals (A—anode, K—cathode, and G—gate) is analogous to that of thyristors.

A complete PUT is obtained by adding the resistors R_1 and R_2 (Fig. 3.9). This element is completely equivalent to a unijunction transistor and its terminals are denoted in the same way. In order to explain its principle of operation, let the input voltage (the emitter voltage of the PNP transistor) increase from 0 to V_{BB} . At $V_E = 0$, T_p is certainly cut off. At the same time the transistor T_n is also cut off. The gate voltage is

$$V_G = \frac{R_1}{R_1 + R_2} V_{BB}. \quad (3.16)$$

Fig. 3.8 Structure (a), model (b), and symbol of PUT (c)



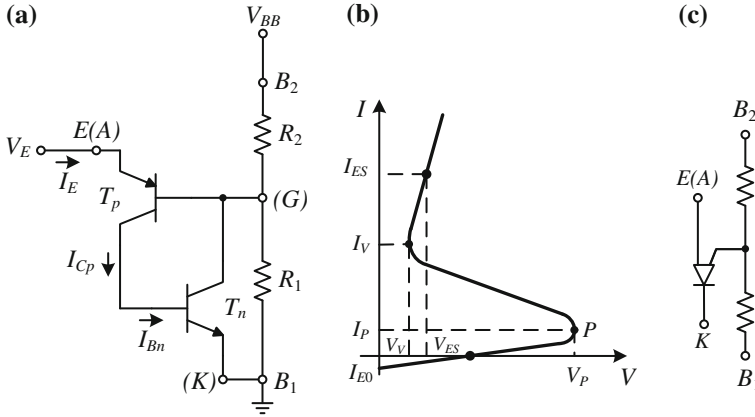


Fig. 3.9 Complete model of PUT (a), its I-V characteristic (b), and a four terminal PUT (c)

Since, $V_{BEp} = V_E - V_G$, for $V_E < V_G$ the emitter junction of the transistor T_p is reverse biased and the emitter current is $I_{EO} \approx (\alpha_{PI}/\alpha_{PN})I_{CO}$, where α_{PI} and α_{PN} are the respective common base reverse and direct current gains of the PNP transistor. T_p starts conducting at $V_E = V_G + V_{EBt}$. Since, $I_{Cp} = I_{Bn}$, T_n is also turned on. For any increase of I_{Cp} by ΔI_{Cp} , the current I_{Cn} will increase by $\beta_n \Delta I_{Cp}$. The base current of T_p is increased by approximately the same amount causing an increase of current I_{Cp} of $\beta_p \Delta I_{Bp}$. Consequently, the current feedback loop is closed which ends by turning the PUT on when both transistors go into saturation. The breakpoint voltage is

$$V_P = \frac{R_1}{R_1 + R_2} V_{BB} + V_{EBt}. \quad (3.17)$$

The input voltage of a PUT in saturation is

$$V_{ES} = V_{EBSp} + V_{CESn} = V_{ECSp} + V_{BESn} = 0.7/1 \text{ V}. \quad (3.18)$$

The resistance in this region is only several Ω and usually can be neglected.

During the decrease of the input current PUT will remain in the saturation region as long as the transistor T_n is in saturation. T_p is the first to cross from the saturation to the active region. Then $I_{Bn} = I_{Cp} = \alpha_p I_E \approx I_E$. When T_n is in the active region, the regenerative process arises again, leading to the turning off of both transistors. Therefore, the minimum conduction current is the saturation base current of the transistor T_n , i.e., $I_V = I_{BSn}$. If the base current of the transistor T_p is neglected, and taking into account that $V_{CESn} < V_{BB}$, it can be written that

$$I_V = I_{BSn} = \frac{V_{BB}}{\beta_n R_2}. \quad (3.19)$$

The minimum conduction voltage is

$$V_v = V_{EBP} + V_{CESn} \approx V_{ES}. \quad (3.20)$$

The essence of the programmability of PUT is in the fact that the basic parameters V_P and I_V can be adjusted by changing the resistances R_1 and R_2 . Some manufacturers make resistors on a single-crystal substrate. Such PUTs have four terminals (Fig. 3.9c).

The programmability is accomplished by adding external resistors in the base circuit of B_2 or B_1 .

The breakpoint voltage is temperature dependent because V_{EBt} is temperature sensitive. Temperature compensation can be accomplished in several ways (Fig. 3.10). First (Fig. 3.10a), since the diode D is always conducting, the breakpoint voltage is determined by

$$V_P = \frac{R_1}{R_1 + R_2} V_{BB} + V_{EBt} - V_D \approx \frac{R_1}{R_1 + R_2} V_{BB}, \quad (3.21)$$

under condition

$$R_D \gg \frac{R_1 R_2}{R_1 + R_2}.$$

Usually $100 \text{ k}\Omega < R < 1 \text{ M}\Omega$. Secondly, two diodes are used. Then:

$$V_P = \frac{R_1}{R_1 + R_2} V_{BB} + V_{EBt} - \frac{2R_1}{R_1 + R_2} V_D. \quad (3.22)$$

If one assumes that $V_D = V_{EBt}$, then temperature compensation is achieved for $R_1 = R_2$ and $V_P = 0.5 V_{BB}$. Therefore, for a given V_{BB} the breakpoint voltage is fixed. For the same purpose use is made of compensation by a transistor

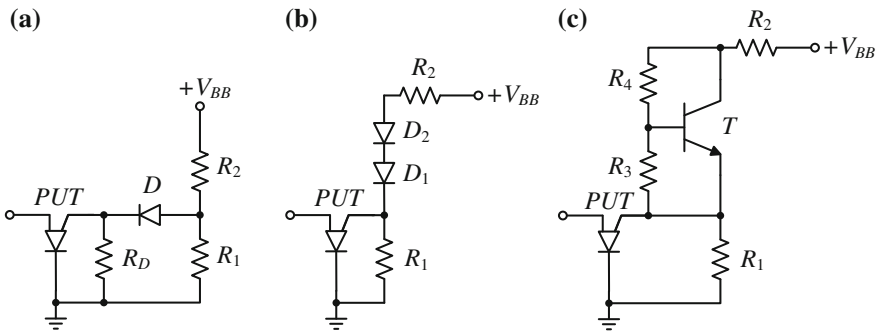


Fig. 3.10 Temperature compensation of the PUT breaking voltage by diodes (a, b) and compensation transistor (c)

(Fig. 3.10c) which together with the resistors R_1 and R_2 makes a voltage multiplier. If the base current is neglected, the current through R_3 and R_4 is $I = V_{BE}/R_4$, and the collector-emitter voltage is

$$V_{CE} = (1 + R_3/R_4)V_{BE}. \quad (3.23)$$

Now the breakpoint voltage is

$$V_P = \frac{R_1}{R_1 + R_2} V_{BB} + V_{EBt} - R_1 \frac{1 + R_3/R_4}{R_2 + R_2} V_{BE}. \quad (3.24)$$

By equating the second and the third member in (3.24) and for $V_{BE} = V_{BEt}$ one obtains that V_P is temperature independent if

$$R_2/R_1 = R_3/R_4. \quad (3.25)$$

Then

$$V_P = \frac{V_{BB}}{1 + R_3/R_4}. \quad (3.26)$$

In selecting the resistors care must be taken that the transistor is on, i.e.,

$$R_4 \frac{V_{BB}}{R_1 + R_2 + R_3 + R_4} > V_{BEt}. \quad (3.27)$$

Usually $R_1 + R_2 \gg R_3 + R_4$ and the condition (3.27) reduces to

$$\frac{R_4}{R_1 + R_2} V_{BB} > V_{BEt}. \quad (3.28)$$

In addition to the programmability of the voltage V_P and the current I_V there are other significant advantages of a PUT over a UJT. The voltage V_V of a PUT is lower, which extends the range of the supply voltages V_{BB} . The resistance R_{BB} is below 10 k Ω and the base-to-base current ranges from 1 to 10 mA. The base-to-base resistance of a PUT is $R_1 + R_2$ and it can be selected within the limits of one hundred Ω up to several hundreds M Ω . If a large minimum conduction current is not required, then R_1 and R_2 should be selected from the range of several tens k Ω up to several hundreds k Ω . This means that the base-to-base current of a PUT can be considerably lower than that of a UJT. Also, the reverse current of the emitter diode (anode) of a PUT is lower by at least one order of magnitude.

Example 3.1 For a circuit of Fig. 3.7b determine dV_P/dT if

- (a) $R = 0$ and
- (b) $R = R_{opt}$.

The circuit from Fig. 3.7b has: $V_{BB} = 10 \text{ V}$, $\eta = 0.6$, $R_{BB} = 8 \text{ k}\Omega$ and $dV_{Di}/dT = -2.7 \text{ mV}/^\circ\text{C}$.

- (a) Taking that η , V_{BB} , and R do not depend on temperature, by differentiation of Eq. (3.9) in a function of temperature and inclusion $R = 0$ in expression (3.11) one obtains

$$\frac{dV_P}{dT} = \frac{dV_{Di}}{dT} = -2.7 \text{ mV}/^\circ\text{C}.$$

- (b) The value of the resistance for which $dV_P/dT \approx 0$ is obtained by calculating the expression (3.12)

$$R_{\text{opt}} \approx 0.34 \frac{R_{BB}}{\eta V_{BB}} = 453 \Omega.$$

3.1.3 Complimentary UniJunction Transistor

The Complimentary UniJunction Transistor (CUJT) consists of a p -type substrate into which an n -type emitter is diffused (Fig. 3.11a). The principle of its operation is identical to that of a UJT. The polarization of the electrodes is different so the static characteristic is in the third quadrant (Fig. 3.11d). The main advantage of CUJT over UJT is that the majority carriers in the emitter are electrons so it can be used at higher frequencies. Furthermore, the minimum conduction voltage is somewhat lower, typically 1.5 V. This extends the range of supply voltages.

Today CUJTs are manufactured by planar technology, like monolithic integrated circuits. This is a four-layer structure comprising an n -type substrate (Fig. 3.12). The diffused resistors R_{B1} and R_{B2} are manufactured together with the active structure. The model containing two complimentary transistors is shown in

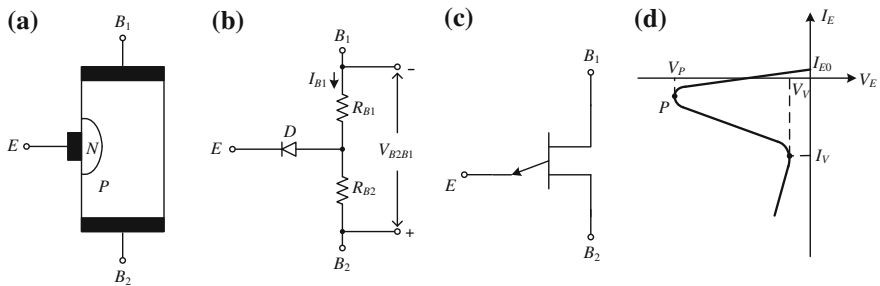


Fig. 3.11 Structure (a), model (b), symbol (c), and static characteristic of a CUJT (d)

Fig. 3.12 Basic structure (a) and transistor model of a planar CUJT (b)

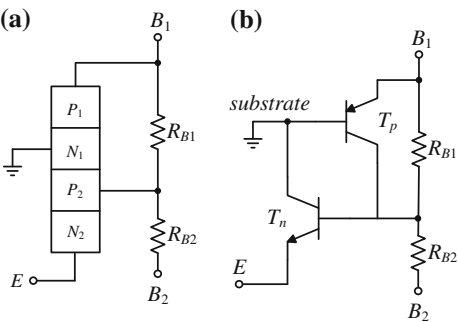


Fig. 3.12b. The shortcoming of this element compared to that of a UJT is that its emitter junction breakdown voltage is several times lower. Usually it is 8–9 V whereas for UJTs it is around 30 V. This limits the application of CUJTs to a supply voltage range of $V_{BB} = 15$ V.

Table 3.1 presents the parameters of conventional UJT 2N2647, CUJT D5K1, and PUT 2N6027.

Table 3.1 Comparative characteristics of various unijunction transistors

Parameter	UJT 2N2647		CUJT D5K1		PUT 2N6027			Unit
	Min	Max	Min	Max	Min	Max	At	
Break point current I_P	–	2	–	5	–	2	^a $R_G = 10$ k Ω , $U_G = 10$ V $R_G = 1$ M Ω	μ A
Constant η	0.68	0.82	0.58	0.62	x	x		–
Base-to-base resistance R_{BB}	4.7	9.1	5.5	8.2	x	x		–
Reverse emitter current I_{EO}	–	0.2	–	0.01	–	0.01		μ A
Breakdown voltage BV_{BE}	30	–	8	–		40		V
Minimum conduction current I_V	8		1		0.07		$R_G = 10$ k Ω $V_G = 10$ V	mA
Minimum conduction voltage V_V	–	2	–	1.5		1		V

^a $R_G = \frac{R_1 + R_2}{R_1 - R_2}$; $V_G = \frac{R_1}{R_1 + R_2} V_{BB}$; x—programmable

3.1.4 Pulse Generators

Unijunction transistors have found main application in simple and inexpensive RC pulse generators. The design of this type of generator requires the use of only one unijunction transistor (Fig. 3.13). This is possible because the static characteristic of a UJT has a region of negative differential resistance. The regenerative process, typical for relaxation generators, occurs within UJT or PUT.

An analysis of a UJT-based pulse generator (Fig. 3.13a) is further given. The scheme and the principle of operation of a PUT-based generator are exactly the same. The pulse waveforms of the voltages V_E and V_O are shown in Fig. 3.14a. During the time interval T_1 the UJT is off. If the reverse current I_E and the resistance R_1 are neglected ($R_1 \gg R_E$), then the capacitor C_E will be charged by V_{BB} via R_E and

$$V_E(t) = V_{BB} - (V_{BB} - V_{CO1})e^{-\frac{t}{C_E R_E}}, \quad (3.29)$$

where V_{CO1} is the voltage across C_E at the end of the conduction of UJT, T_2 . At

$$V_E(T_1) = V_P, \quad (3.30)$$

the UJT turns on and, on the basis of (3.29) and (3.30), one obtains

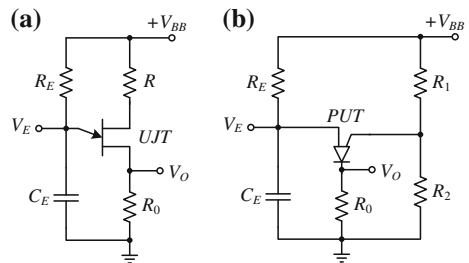
$$T_1 = C_E R_E \ln \frac{V_{BB} - V_{CO1}}{V_{BB} - V_P}, \quad (3.31)$$

where the breakpoint voltage, V_P , is determined by (3.14). At the end of the regenerative process the UJT is on. The resistance R_S between the emitter and the base B_1 is then only several Ω , and can be neglected.

At the start of this interval the operating point is in the position Q (Fig. 3.14b). Now, the capacitor C_E is discharging. The emitter current decreases and is determined by

$$i_E(t) = \frac{V_{BB} - V_{EB1}}{R_E + R_0} + \left(\frac{V_P - V_{EB1}}{R_0} - \frac{V_{BB} - V_{EB1}}{R_E + R_0} \right) e^{-t/\tau}, \quad (3.32)$$

Fig. 3.13 Pulse generators comprising UJT (a), or PUT (b)



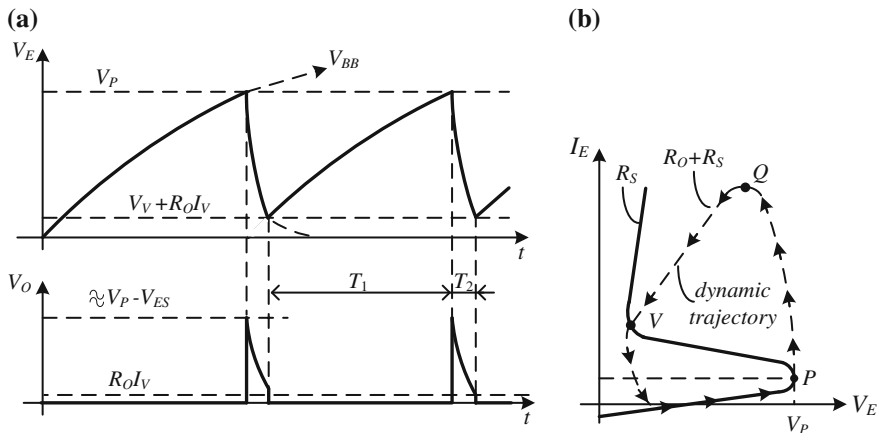


Fig. 3.14 Pulse waveforms (a) and dynamic trajectory of the operating point of the pulse generators from Fig. 3.13 (b)

where

$$\tau = C_E \frac{R_0 R_E}{R_E + R_0}.$$

As a rule, the resistance R_0 is between 10 and 100 Ω and $R_0 \ll R_E$. Now, the member in the brackets in (3.32) can be neglected and $\tau \approx C_E R_0$, so

$$i_E(t) \approx \frac{V_{BB} - V_{BB1}}{R_E} + \frac{V_P - V_{EB1}}{R_0} e^{-\frac{t}{C_E R_0}}. \quad (3.33)$$

Quasi-stable interval T_2 ends at

$$i_E(T_2) = I_V. \quad (3.34)$$

Now, $V_{EB1} = V_v$, and from (3.33) and (3.34)

$$T_2 = C_E R_0 \ln \frac{(V_P - V_v)/R_0}{I_V - (V_{BB} - V_v)/R_E}. \quad (3.35)$$

After T_2 UJT is off again and the capacitor C_E is discharging. The initial voltage across the capacitor is $V_{CO1} = V(T_2) = V_v + R_O I_v \approx V_v$, and finally

$$T_1 = C_E R_E \ln \frac{V_{BB} - V_v}{V_{BB} - V_P}. \quad (3.36)$$

The cycle of oscillation is $T = T_1 + T_2$. Since $R_E \gg R_0$, then $T_1 \gg T_2$ and $T \approx T_1$.

The condition of oscillation is determined by the position of the static load line with respect to the static characteristic of the UJT (Fig. 3.15a). The static conditions are determined for the circuit without the timing capacitor (Fig. 3.15b). The load line is

$$V_E = V_{BB} - R_E I_E. \quad (3.37)$$

because $R_E \gg R_0$. For the oscillating mode of the generator the load line must cross the static characteristic of UJT in the region of negative differential resistance. Thus, at $V_{EB1} = V_V$ it must be $I_E < I_V$, and from (3.37)

$$R_E > (V_{BB} - V_V)/I_V = R_{E\min}, \quad (3.38)$$

and at $V_E = V_P$, $I_E > I_P$, therefore it follows

$$R_E < (V_{BB} - V_P)/I_P = R_{E\max}. \quad (3.39)$$

Allowing for example $I_V = 1$ mA, $V_V = 2$ V, $I_P = 1$ μ A, $\eta = 0.6$, and $V_{BB} = 10$ V. Then, $V_P \approx \eta V_{BB} \approx 6.7$ V and on the basis of (3.38) and (3.39), 8 k $\Omega < R_E < 3.3$ M Ω . Therefore, the timing resistor R_E can be varied over a wide range. For the purpose of ensuring a soft transition from the saturation region to the negative differential resistance region it is recommendable that the lowest resistance of R_E is several times higher than the minimum value determined by (3.38).

The value of the timing capacitance C_E can also be varied over a very wide range (from several nF to several tens of μ F). The minimum capacitance is limited by the turn-on (t_u) and turn-off (t_i) times of the unijunction transistor. Usually, these times are between one hundred and several hundreds of ns. Since, the minimum quasi-stable interval must be $T_{\min} > t_u + t_i$, it follows that the minimum capacitance C_E is from several nF to several tens of nF.

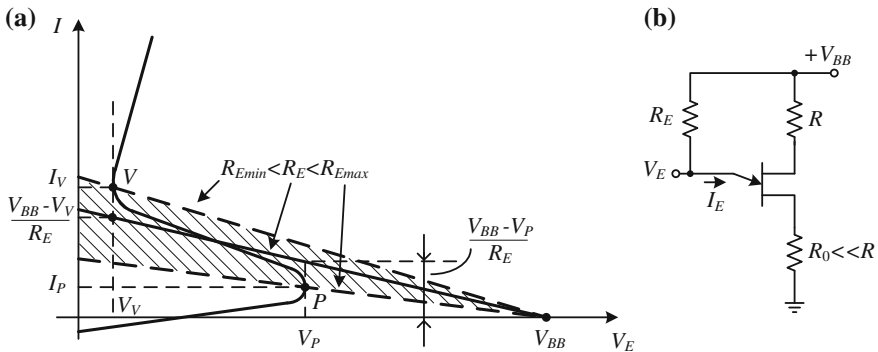


Fig. 3.15 Position of load line (a) of an oscillating generator and the equivalent circuit for determination of static conditions (b)

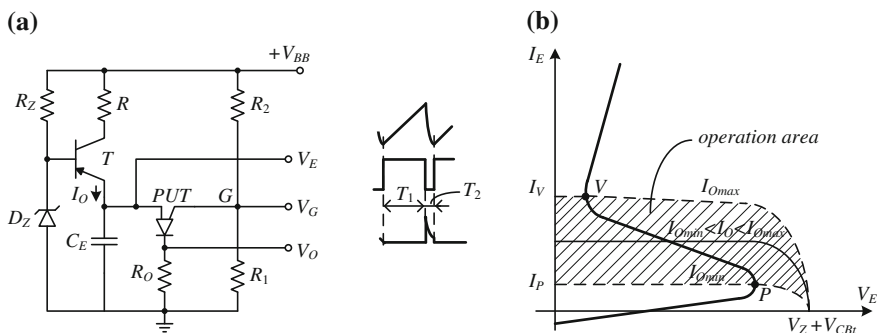


Fig. 3.16 PUT-based function generator (a) and its operation area (b)

Sometimes the UJT is used when designing generators that have simultaneously outputs of saw tooth and rectangular wave-shapes. A standard generator of this type using a PUT is shown in Fig. 3.16. The function of the timing resistor here is taken over by the current generator comprising elements T , D_z , R , and R_z producing the current

$$I_0 \approx (V_{BB} - V_{EB} - V_z)/R. \quad (3.40)$$

While the PUT is off, the variation of voltage V_E is linear

$$V_E(t) = V_V + I_V R_0 + \frac{I_0}{C} t. \quad (3.41)$$

From condition (3.30) and on the basis of (3.41) it follows that

$$T_1 = C \frac{V_P - (V_V + I_V R_0)}{I_0}. \quad (3.42)$$

The region of oscillation (Fig. 3.16b) is limited by

$$I_P < I_0 < I_V. \quad (3.43)$$

In addition, the collector junction of the transistor must not be forward biased, i. e., $V_P < V_z + V_{CBt}$, giving

$$V_z > \frac{R_1}{R_1 + R_2} V_{BB}. \quad (3.44)$$

The places of the resistance R_z and the Zener diode can be interchanged. Then, the condition $V_z < V_{BB} R_z / (R_1 + R_2)$ has to be satisfied.

Simple generators based on UJT are highly asymmetric ($T_1 \gg T_2$). By adding one transistor (Fig. 3.17) one obtains a generator where it is possible that $T_1 < T_2$. When

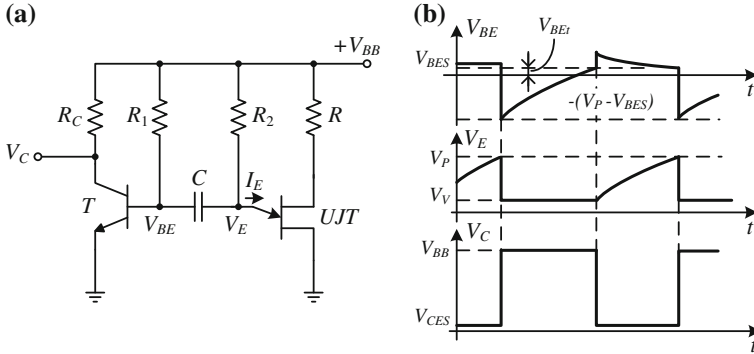


Fig. 3.17 Oscillator based on UJT and transistor T_r (a) and the voltage waveforms (b)

the UJT is cut off, T_r is on and vice versa. The pulse waveforms at characteristic points are shown in Fig. 3.17b. While the UJT is cut off, T_r is in saturation so

$$V_E = V_{BB} - (V_{BB} - V_V + V_{BEt})e^{-\frac{t}{R_2 C}}. \quad (3.45)$$

This quasi-stable period ends when $V_E(T_1) = V_P$ so that:

$$T_1 = R_2 C \ln \frac{V_{BB} - V_V + V_{BEt}}{V_{BB} - V_P}. \quad (3.46)$$

Now the UJT is in the saturation region and T_r is cut off. The capacitor C charges via resistor R_1 in the opposite direction and so

$$V_{BE}(t) = V_{BB} - (V_{BB} - V_P - V_V + V_{BES})e^{-\frac{t}{R_1 C}}. \quad (3.47)$$

The next change of state occurs at $V_{BE}(T_2) = V_{BEt}$ so on the basis of (3.47)

$$T_2 = R_1 C \ln \frac{V_{BB} - V_P - V_V + V_{BES}}{V_{BB} - V_{BEt}}. \quad (3.48)$$

Equation (3.48) applies if

$$I_E(T_2) = \frac{V_{BB} - V_V}{R_2} + \frac{V_{BB} - V_{BEt}}{R_1} > I_V, \quad (3.49)$$

therefore it follows

$$R_1 < \frac{V_{BB} - V_{BEt}}{I_V - (V_{BB} - V_V)/R_2}. \quad (3.50)$$

The restrictions on the resistance R_2 are defined by (3.38) and (3.39), i.e.,

$$\frac{V_{BB} - V_P}{I_P} < R_2 < \frac{V_{BB} - V_V}{I_V}. \quad (3.51)$$

In the static conditions the transistor T_r should be in the saturation region. For this reason

$$R_1 < \beta R_C \frac{V_{BB} - V_{BES}}{V_{BB} - V_{CES}} \approx \beta R_C. \quad (3.52)$$

3.1.5 Non-standard Applications

It is possible to use a UJT for designing monostable and bistable multivibrators. In the stable state of a monostable multivibrator, re-triggering enabled (Fig. 3.18), UJT is cut off and its static load line crosses its I-V characteristic in the saturation region (Fig. 3.18b). Therefore, it is required that $(V_{BB} - V_V)/R_E > I_V$, therefore, it is

$$R_E < (V_{BB} - V_V)/I_V. \quad (3.53)$$

T_r is turned on by a positive pulse. This will cause a reduction of the emitter current of the UJT by factor β , i.e., by the amount corresponding to the collector current of the transistor T_r . This should bring the operating point into the region of negative differential resistance, i.e.,

$$(V_{BB} - V_V)/R_E - \beta I_B < I_V, \quad (3.54)$$

and this turns off the UJT. Thus, the minimum resistance is bounded by

$$R_E > \frac{V_{BB} - V_V}{I_V + \beta I_B}. \quad (3.55)$$

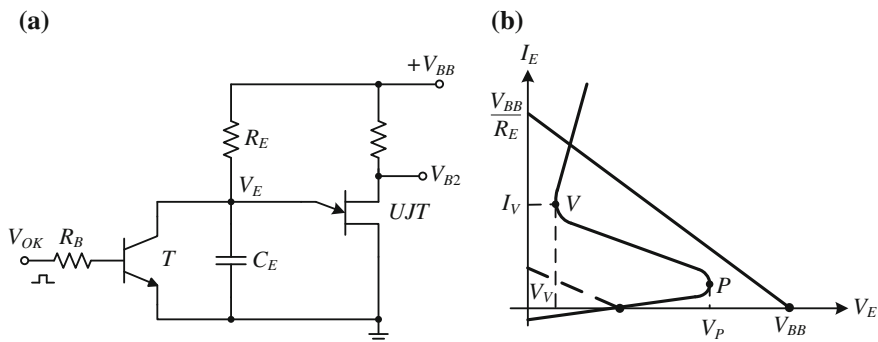


Fig. 3.18 Monostable multivibrator re-triggering enabled (a) and the position of its static load line (b)

During the positive triggering pulse the capacitor C will be discharged. T_r is then in saturation, i.e., $V_E = V_{CES}$. At the trailing edge of the triggering pulse T_r is turned off and the capacitor C_E starts charging. Then

$$V_E = V_{BB} - (V_{BB} - V_{CES})e^{-\frac{t}{C_E R_E}}. \quad (3.56)$$

The quasi-stable interval T_M ends when $V_E(T_M) = V_P$ so that, on the basis of (3.56) and bearing in mind that $V_{BB} \gg V_{CES}$,

$$T_M = C_E R_E \ln \frac{V_{BB}}{V_{BB} - V_P} + \Delta t, \quad (3.57)$$

where Δt is the width of the positive triggering pulse.

In the re-triggering mode a triggering pulse arrives before V_E reaches the value of the breakpoint voltage of the UJT. Thus, the condition for re-triggering is

$$V_E(T_0) < V_P. \quad (3.58)$$

Since T_r is turned on, during Δt C_E is discharged to the initial value $V_E = V_{CES}$. At the end of Δt , T_r is turned off and the capacitor C_E restarts charging (Fig. 3.19). Throughout this period the UJT is turned off. If one assumes that $V_P = \eta V_{B2} + V_{Dt} \approx \eta V_{BB}$, then, on the basis of (3.58) and (3.56), the re-triggering condition can be written in the form

$$C_E R_E < -\frac{T_0}{\ln(1 - \eta)}. \quad (3.59)$$

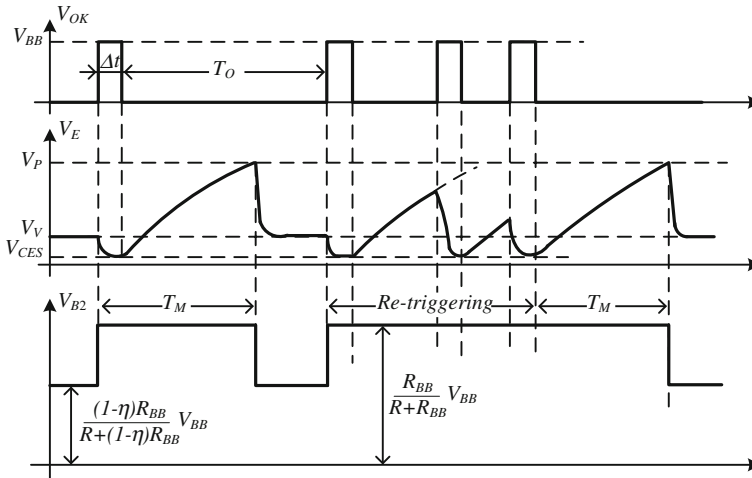


Fig. 3.19 Voltage pulse waveforms of a UJT based monostable multivibrator

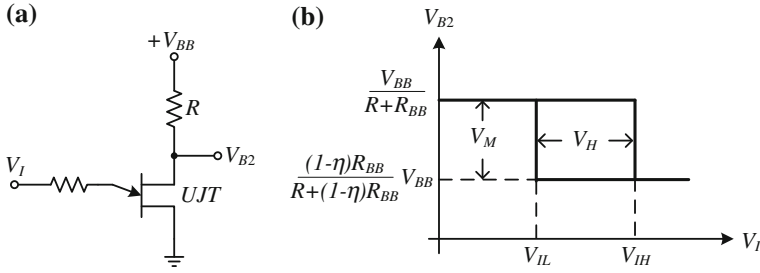


Fig. 3.20 Schmitt trigger based on UJT (a) and its transfer characteristic (b)

It is possible to design a monostable multivibrator having the UJT cut off during the stable state. In that case, the static load line crosses the I-V characteristic in the cut off region. This position of the load line is shown by dotted lines in Fig. 3.18b.

Among the nonstandard applications a very simple Schmitt trigger will be described (Fig. 3.20). This possibility is quite obvious since the input characteristic of UJT is in the form of a hysteresis loop. Here, the lower threshold of the Schmitt trigger is controlled by the resistor R_E . The upper threshold is determined by

$$V_{TH} = V_P + R_E I_P \approx V_P. \quad (3.60)$$

In the course of decreasing the input voltage, the UJT turns off when $I_E = I_V$. Then, $V_{EB1} = V_V$ and the lower threshold of the Schmitt trigger is

$$V_{TL} = R_E I_V + V_V. \quad (3.61)$$

The hysteresis voltage

$$V_H = V_P - V_V - R_E I_V. \quad (3.62)$$

can be controlled by changing the resistance R_E over the range from 10 V down to several hundreds mV. The maximum value of R_E is limited by the condition that upon turn-on the UJT is in the saturation region, i.e., $(V_P - V_V)/R_E > I_V$, or $V_H > 0$. Therefore, it follows

$$R_E < (V_P - V_V)/I_V. \quad (3.63)$$

The minimum resistance R_E is limited by the maximum permitted emitter current $I_{E\max}$. Namely

$$R_E > \frac{V_{I\max} - V_V}{I_{E\max}}, \quad (3.64)$$

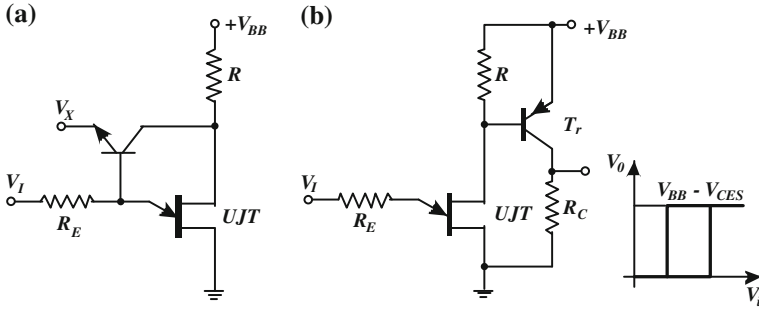


Fig. 3.21 Programmable Schmitt trigger (a) and Schmitt trigger having increased output voltage amplitude (b)

where $V_{I_{\max}}$ is the maximum value of the input voltage.

By adding one NPN transistor one obtains an interesting solution for the Schmitt trigger having a voltage controlled upper threshold level (Fig. 3.21). In essence UJT, the transistor T_r , and the resistor R make a sort of PUT having the breakpoint voltage

$$V_P = V_x + V_{BE} \quad (3.65)$$

which is a function of the control (programming) voltage V_x . At the same time the following condition has to be met

$$V_I - V_{BEt} < V_x < \eta \frac{V_{BB}}{1 + R/R_{BB}} \approx \eta V_{BB}. \quad (3.66)$$

As long as $V_I < V_x$, UJT and T_x are in the cut off region. At $V_I = V_x + V_{BEt}$, T_x begins turning on. Owing to this the reduction of V_{B2B1} of the UJT will follow. Now it is

$$V_{B2B1} = \frac{V_{BB} - \beta I_B R}{1 + R/R_{BB}}, \quad (3.67)$$

where β is the current gain of the transistor T_x . A small change of the current I_B , and consequently of the voltage V_{BE} , will cause a considerable reduction of V_{B1B2} . Since, the breakpoint voltage of UJT is $V_P = \eta V_{B2B1} + V_{Dt}$, it means that soon after turning on of T_r , turning on of the UJT will occur. For this reason the breakpoint voltage is determined by (3.65). If the breakpoint current I_P of the UJT is neglected, the upper threshold of the Schmitt trigger is

$$V_{TH} = V_x + V_{BE} + R_E I_{BP} \quad (3.68)$$

From the condition

$$V_x + V_{BE} = V_p = \eta \frac{V_{BB} - \beta R I_{BP}}{1 + R/R_{BB}} + V_{Dt}$$

it follows that the base current I_{BP} at which the UJT turns on is

$$I_{BP} = \frac{V_{BB}}{\beta R} \left[1 - \frac{V_x}{\eta V_{BB}} \left(1 + \frac{R}{R_{BB}} \right) \right]. \quad (3.69)$$

Since, this current is very low, the member $R_E I_{BP}$ in (3.68) can be neglected and

$$V_{TH} \approx V_x + V_{BE}. \quad (3.70)$$

Immediately upon the UJT being turned on, the transistor T_r is turned off. Thus its only task is to initiate the turning on of the UJT. Therefore, the lower threshold is determined by (3.61).

The output voltage amplitude V_M of the Schmitt triggers in Figs. 3.20 and 3.21 is relatively small ($V_M < 0.5$ V). By adding a PNP transistor (Fig. 3.21b), the amplitude is $V_M = V_{BB} - V_{ECS} \approx V_{BB}$. In order to keep T_r in the saturation region when the UJT is conducting, it has to be

$$\frac{V_{BB} - V_{EB}}{R_{B2}} - \frac{V_{EB}}{R} > \frac{V_{BB} - V_{ECS}}{\beta R_C} \quad (3.71)$$

Since, $V_{BB} \gg V_{EB}$ and $R_{B2} = (1 - \eta)R_{BB}$, and taking into account that the member V_{EB}/R can be neglected, from (3.71) it follows:

$$R_C > \frac{1 - \eta}{\beta} R_{BB}. \quad (3.72)$$

Therefore, if the UJT is off, T_r must also be off. Thus, $RV_{BB}/(R + R_{BB}) < V_{EBt}$, therefore, for $V_{BB} \gg V_{EBt}$

$$R < \frac{V_{EBt}}{V_{BB}} R_{BB}. \quad (3.73)$$

For example, for $V_{BB} = 10$ V, $R_{BB} = 8$ k Ω , $\eta = 0.6$, $\beta = 50$, and $V_{EBt} = 0.6$ V; on the basis of (3.72) and (3.73) one obtains $R_C > 640$ Ω and $R < 480$ Ω . The choice can be $R_C = 1.5$ k Ω and $R = 320$ Ω .

3.2 Thyristors

The thyristor is general name for a family of four-layer semiconductor switches comprising three p-n junctions. Often, however, this concept implies a complete group of regenerative switches. Within this concept the unijunction transistor belongs to the thyristor group. Broadly speaking, the thyristor (Greek *thyra*—*gate*) is a bistable switch having a regenerative transition from the high-resistance to the low-resistance region and vice versa. The ranges of controlled currents and voltages are very wide. The nominal values of currents of the present day thyristors range from several mA up to several thousands of A and the nominal values of voltages extend up to 10,000 V.

3.2.1 Triode Thyristor—SCR

The triode thyristor is representative of the four-layer elements and it is often referred to as thyristor. It comprises three electrodes (anode, cathode, and control electrode—gate). The load is connected in the anode–cathode circuit and the control is realized via the gate. Since, the triode thyristor is most frequently used in AC circuitry as a rectifier (conducts in one direction only, like a diode) having a controlled conduction angle, the abbreviated name *Silicon Controlled Rectifier (SCR)* is almost universally accepted.

The thyristor structure and a typical distribution of impurities are shown in Fig. 3.22. Technologically, the initial material is a highly resistive N_1 region having typical concentration of donor dopants from 10^{14} to 10^{15} cm^{-3} .

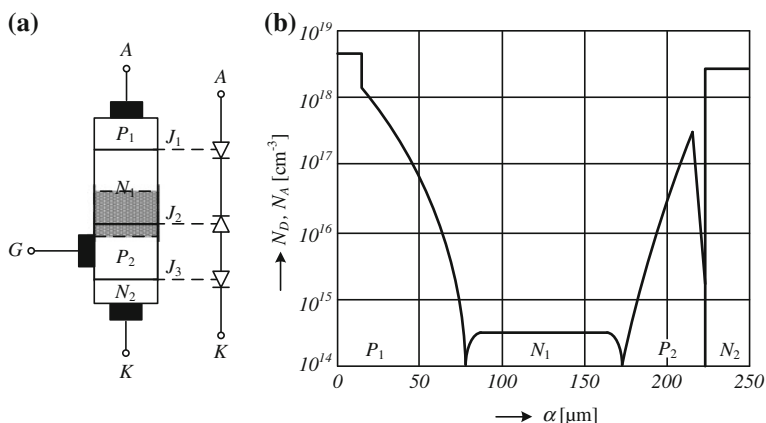


Fig. 3.22 Thyristor structure (a) and typical distribution of dopant concentrations (b)

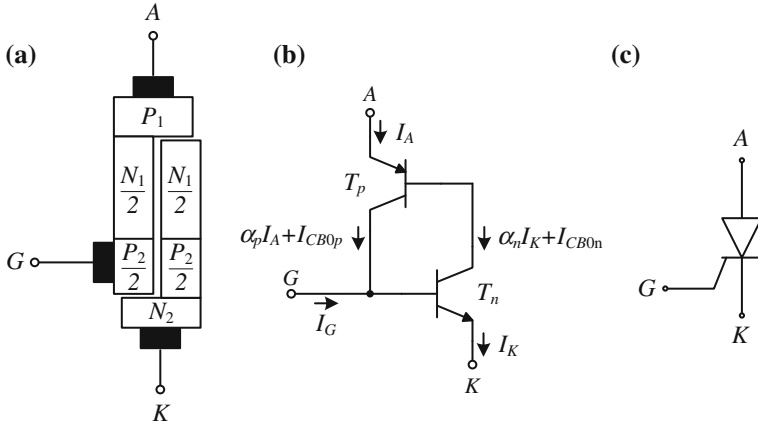


Fig. 3.23 Two-transistor model of the thyristor (SCR) (a and b) and its symbol (c)

On both sides are deeply diffused p -type regions. The first p -region P_1 is the anode emitter. The cathode emitter is made of the n^+ -type diffused region N_2 . Thus, a thyristor consists of three p-n junctions.

At forward bias, when $V_{AK} > 0$, the outside junctions J_1 and J_3 are forward biased and the central junction J_2 is reverse biased. The thyristor current is then determined by the current of the reverse biased p-n junction. Practically, the full applied voltage V_{AK} is across junction J_2 . Owing to the low dopant concentration, the space charge region is located in the N_1 region (shaded area in Fig. 3.22). The thyristor will crossover from the cut off to the conduction region when the voltage V_{AK} is equal to the breakdown voltage of the central p-n junction.

In order to simplify the explanation of the turn-on and turn-off mechanisms, it is customary to represent the thyristor using a two-transistor model (Fig. 3.23).

The regions N_1 and P_1 are common for the PNP and NPN transistors. Allowing the gate to be open, i.e., $I_G = 0$. At $V_{AK} > 0$, both emitter junctions are forward biased, whereas the common collector p-n junction is reverse biased. The transistors are, thus, in the active forward regions. Since at $I_G = 0$ the anode and cathode currents are equal, then

$$I_A = \alpha_p I_A + I_{CBOp} + \alpha_n I_A + I_{CBOn}, \quad (3.74)$$

Therefore, it follows

$$I_A = \frac{I_{CBOp} + I_{CBOn}}{1 - (\alpha_n + \alpha_p)} = \frac{2I_{CBO}}{1 - (\alpha_n + \alpha_p)}, \quad (3.75)$$

where α_n and α_p denote the common-base current gains of transistors T_n and T_p , respectively. If the individual currents of the collector junction are equal, then its total current is $I_{CBOp} + I_{CBOn} = 2I_{CBO}$.

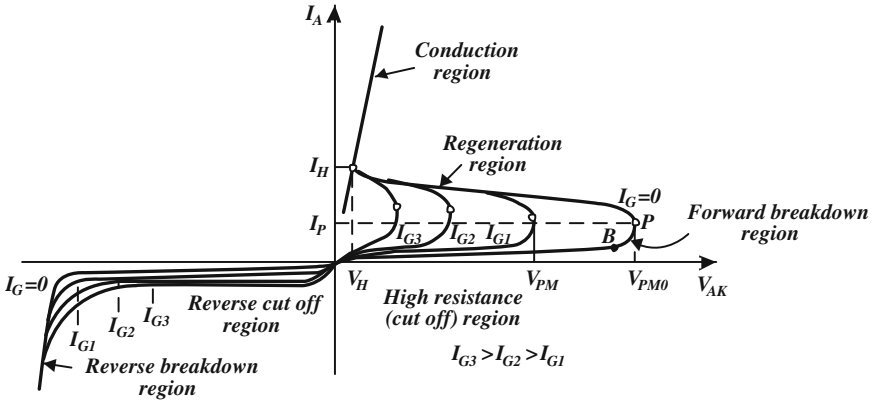


Fig. 3.24 Static I-V characteristic of SCR

At small currents I_A the gains α_n and α_p are very small (Fig. 3.25a), and $I_A = I_K \approx 2I_{CBO}$. An increase of the voltage $V_{AK} \approx V_{CBn} = V_{CBp}$ causes the current I_{CBO} to increase gradually, so α_n and α_p also increase. When V_{AK} becomes sufficiently large, in the reverse biased barrier of J_2 the process of avalanche multiplication starts. The thyristor is in the forward breakdown region (region between the points B and P in Fig. 3.24). In the breakpoint P the regenerative process starts by turning on of the thyristor with both transistors T_n and T_p in the saturation region. Namely, an increase of the base current of the transistor T_n will cause its collector current to increase β_n times the base current. Since, $i_{cn} = i_{bp}$, the collector current of the transistor T_p will increase $\beta_n \beta_p$ times. Thus, the closed loop current gain is $\beta_n \beta_p$. If the regenerative process is to start, it has to be

$$\beta_p \beta_n \geq 1, \quad (3.76)$$

therefore the thyristor turn-on condition follows in the form

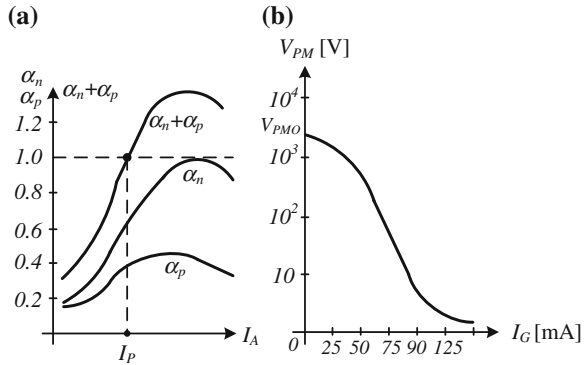
$$\alpha_n + \alpha_p = 1. \quad (3.77)$$

The same result is obtained on the basis of Eq. (3.75) and the condition that $I_A \rightarrow \infty$. The current I_A , to which (3.77) applies, is the breakpoint current I_P (Fig. 3.25a).

The anode current of the thyristor in the off state, at $I_G = 0$, is so small that the condition (3.77) is impossible to reach without a considerable increase of V_{AK} . If one assumes that the multiplication factors of electrons and holes are equal, then one can write that the anode current in the breakdown region is

$$I_A = \frac{2I_{CBO}M}{1 - M(\alpha_n + \alpha_p)}, \quad (3.78)$$

Fig. 3.25 Current gains α_n and α_p of transistors T_n and T_p as functions of the anode current (a) and the dependence of the break point voltage on the gate current (b)



where the multiplication factor is

$$M = \frac{1}{1 - (V_{AK}/BV_{J2})^n}, \quad (3.79)$$

where BV_{J2} is the breakdown voltage of the central p-n junction. By letting $I_A \rightarrow \infty$, at $V_{AK} = V_{PMO}$, from (3.78) and (3.79) one obtains the breakpoint voltage

$$V_{PMO} = BV_{J2} n \sqrt{1 - (\alpha_n + \alpha_p)} \quad (3.80)$$

In order to have a V_{PMO} as high as possible, the gain of one of the transistors has to be quite small. Usually, this is the transistor T_p (Fig. 3.23), since its base (region N_1) is very wide.

If, however, $I_G > 0$, the thyristor will turn-on sooner, i.e., $V_{PM} < V_{PMO}$ (Fig. 3.24). Namely, due to a positive I_G the thyristor current is higher, so α_n and α_p are higher which leads to the turn-on at lower voltages V_{AK} . Now

$$I_K = I_A + I_G, \quad (3.81)$$

and the anode current is

$$I_A = \frac{\alpha_n I_G + 2I_{CBO}}{1 - (\alpha_n + \alpha_p)}. \quad (3.82)$$

Therefore, the turn-on condition is again $\alpha_n + \alpha_p = 1$. The difference is that α_n and α_p increase primarily due to current I_G . This is exactly why the breakpoint voltage is inversely proportional to the gate current I_G (Fig. 3.24). Practically, if I_G is sufficiently high, the break point voltage could be only several V (Fig. 3.25b). Consequently, the breakpoint voltage of the SCR is programmable by the gate current within limits from several V up to the value of the breakpoint voltage at $I_G = 0$, V_{PMO} .

In the conduction region both transistors are saturated, the anode-to-cathode voltage is

$$V_{AKS} = |V_{CES}| + |V_{BES}| \quad (3.83)$$

and, depending on the anode current, it ranges from 0.7 V up to 2 V. It should be emphasized that no gate current is needed in the state of conduction. Therefore, the thyristor is a switch that requires a relatively small drive only during turn-on. This makes the essential difference between the thyristor and the bipolar transistor as a switch. Namely, a transistor requires a permanent and relatively high drive throughout the state of conduction. For instance, if a transistor, maintaining a collector current of about 20 A, is to be in saturation, the base current of at least 1 A is required.

The thyristor will remain in the on state (the region of low resistance) as long as the anode current is higher than the holding current, I_H . The holding current is the lowest anode current maintaining the thyristor in the state of conduction with the gate open ($I_G = 0$). Namely, at $I_A = I_H$ the regenerative process is restarted and owing to the reduction of I_A it leads to the turning off of the thyristor. Typical values of I_H are within the range from several hundreds μA up to 10 mA.

At reverse bias ($V_{AK} < 0$), the outside p-n junctions J_1 and J_3 of the thyristor are reverse biased. Because of that the regenerative process does not arise in the region of reverse breakdown. The current-voltage characteristic in this region is very similar to the I - V characteristic of a reverse biased diode. Since, the region N_1 is only weakly doped, i.e., its resistance is much higher compared to that of the region N_2 , most of the applied voltage appears across the junction J_1 and the influence of the junction J_3 can be neglected. The breakdown occurs either due to the avalanche process or due to the spreading of the transition region of the junction J_1 over the entire region N_1 up to the junction J_2 . However, since the region N_1 is quite wide, the breakdown is mainly caused by the avalanche process.

3.2.1.1 Characteristics of Control Electrode (Gate)

As already emphasized, a controlled turn-on of a thyristor occurs at the moment when the positive gate current I_G causes a positive anode-to-cathode bias, $V_{AK} > 0$. After the thyristor is turned on, no gate drive is required. Moreover, it is then of no use because it only heats up the thyristor. In addition, there is no use of a negative anode bias since it increases the reverse anode current (Fig. 3.24). Because of all this, the gate should be pulse driven. The driving pulse should have the required gate current I_G , the voltage V_G , and a sufficient length T_G .

The time T_G is several μs . Practically, however, T_G is between 10 and 20 μs and the gate $I_g - V_g$ characteristics are called the static thyristor characteristics (Fig. 3.26). Practically, these are the I - V characteristics of the P_2N_2 junction and

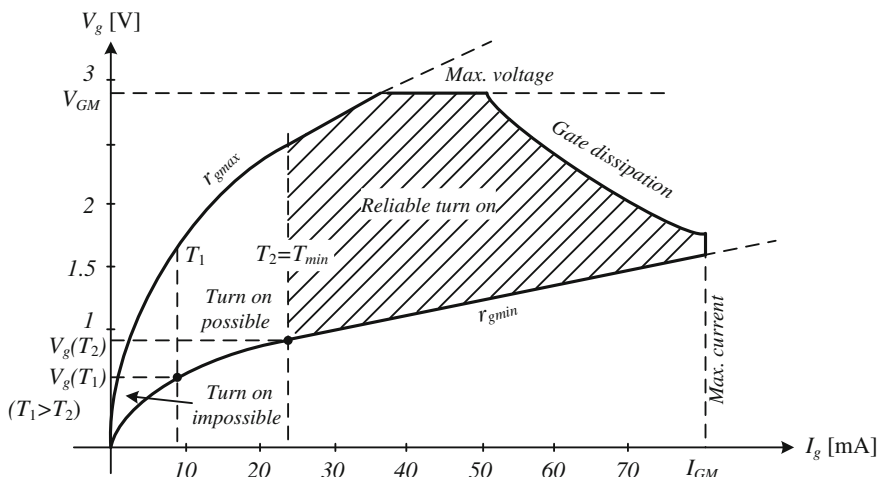


Fig. 3.26 Static start-up characteristics of a thyristor

they are determined by the minimum (r_{gmin}) and maximum (r_{gmax}) gate resistances. The gate voltage has to be higher than the threshold voltage of the p-n junction which is about 0.5 V. The region of safe turn-on of the thyristor is the cross-hatched region shown in Fig. 3.26. The maximum voltage V_{GM} is several V and the maximum gate current I_{GM} ranges from 100 mA for low power thyristors up to the order of one A for power thyristors. On the right-hand side the operating region is limited by the hyperbola of permitted dissipation. This is power which will not cause any damage to the p-n junction. Owing to the temperature dependence of the p-n junction voltage, triggering of a thyristor is not reliable in the region of the characteristics without cross-hatch. Therefore, at lower temperatures the region of safe triggering is narrower.

In order to accomplish the exactly defined instant of thyristor triggering, it has to be driven by current pulses of much higher level compared to those corresponding to the static conditions. In other words, an overdrive current pulse is applied. In this way the influence of temperature variations of the gate characteristics is reduced and very short triggering times are accomplished.

Example 3.2 The characteristics of a directly biased thyristor are shown in Fig. 3.27. Determine the power losses on the thyristor for excitations shown in Fig. 3.28a, b.

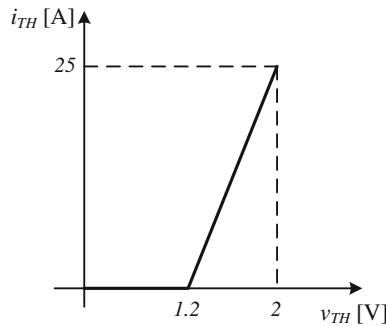


Fig. 3.27 Characteristics of thyristor in direct polarization

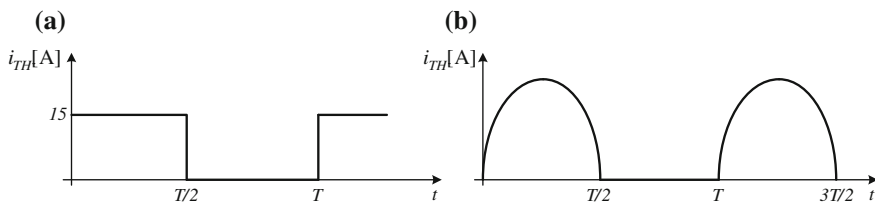


Fig. 3.28 Thyristor current—rectangular form (a), form of sine half-wave (b)

Voltage on the thyristor when it is directly biased (Fig. 3.27) is: $V_{TH} = V_{TH0} + r_{TH}i_{TH}$, where $V_{TH0} = 1.2$ V, and $r_{TH} = 0.8/25 = 32$ m Ω . In a general case power losses on the thyristor in the period T are equal to

$$p_{TH} = \frac{1}{T} \int_0^T i_{TH}(t) v_{TH}(t) dt \quad (3.84)$$

Substituting the expression for the voltage on the thyristor when it is directly biased into Eq. (3.55) one obtains

$$\begin{aligned} p_{TH} &= \frac{1}{T} \int_0^T i_{TH}(t) (V_{TH0} + r_{TH} i_{TH}(t)) dt \\ &= \left[V_{TH0} \frac{1}{T} \int_0^T i_{TH}(t) dt + r_{TH} \frac{1}{T} \int_0^T i_{TH}^2(t) dt \right] = V_{TH0} I_{TH,sr} + r_{TH} I_{TH,eff}^2. \end{aligned} \quad (3.85)$$

If the current through the thyristor is as shown in Fig. 3.28a, the average value of the current is $I_{\text{THsr}} = 15/2 = 7.5$ A, and the effective value of the current is $I_{\text{THeff}} = 15/\sqrt{2} = 10.6$ A. Substituting these values in Eq. (3.85) one obtains

$$p_{\text{TH}} = 7.5 \times 1.2 + 0.032 \times (10.6)^2 = 12.63 \text{ W}.$$

In a case, when the current has the form of a sine half-wave (Fig. 3.28b) the average value of the current through the thyristor is:

$$I_{\text{THsr}} = \frac{1}{T} \int_0^{T/2} 20 \sin(\omega t) dt = \frac{20}{\pi} = 6.36 \text{ A}.$$

The effective value of the current through the thyristor is $I_{\text{THeff}} = \frac{I_{\text{THmax}}}{2} = 10$ A. Substituting these values in Eq. (3.85) one obtains

$$p_{\text{TH}} = 6.36 \times 1.2 + 0.032 \times 10^2 = 10.83 \text{ W}.$$

3.2.1.2 Effect of the Rate of Anode Voltage Change (dv/dt Effect)

The previous analysis of the turn-on process is valid only under the assumption that the anode voltage changes are slow. At high rates of anode voltage variations turning on of a thyristor will be faster. Since, the collector p-n junctions of transistors T_n and T_p are reverse biased, they can be considered as a capacitor (Fig. 3.29a). If the voltage drop across the forward biased emitter junctions is neglected, the current through this capacitor is

$$i = C_{\text{CB}} \frac{dV_A}{dt} + V_A \frac{dC_{\text{CB}}}{dt} \approx \frac{1}{2} C_{\text{CB}} \frac{dV_A}{dt}, \quad (3.85)$$

since $C_{\text{CB}} \sim 1/\sqrt{U_A}$.

Thus, the anode current is proportional to the rate of change of the anode voltage. At high rates of dV_A/dt this current may become significant. As the current rises, the current gains α_n and α_p increase and the turn-on conditions are fulfilled at lower input voltages (3.77). In other words, the turn-on occurs at smaller voltages compared to the static breakpoint voltage V_{PMO} . Therefore, the capacitive current causes the thyristor to turn-on in accordance with the same mechanism as that of the gate current. Figure 3.29b shows the dependence of the breakpoint voltage of a thyristor on the rate of change of the anode voltage and temperature. As the temperature increases, this dependence becomes more pronounced because the constants α_n and α_p are higher. Moreover, this effect is more pronounced for power thyristors since the capacitance C_{CB} is proportional to the cross section S . This phenomenon is often called the dv/dt effect or dv/dt capability.

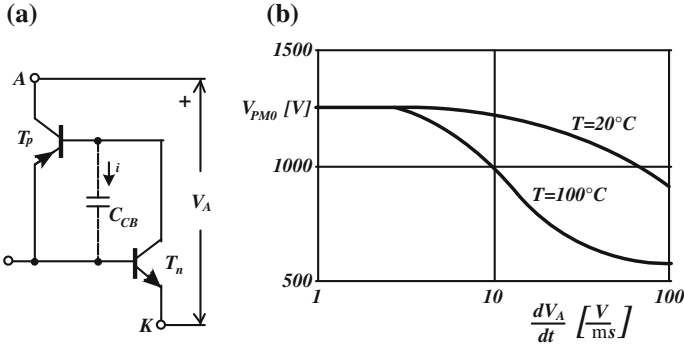


Fig. 3.29 High frequency thyristor model (a) and break point voltage versus the rate of anode voltage change and with temperature as parameter (b)

In device specifications it is defined as the maximum value of $(dV_A/dt)_M$ which will not cause the turn-on process of a thyristor. It ranges from 10 V/ μs up to about 100 V/ μs .

It is possible to increase the capability dv/dt in several different ways (Fig. 3.30). A capacitor C_S between the anode and cathode (Fig. 3.30a) reduces the rate of the anode voltage increase. The anode-to-cathode voltage now increases exponentially. In the limiting case when the voltage V_{AA} changes abruptly, the condition must be satisfied that

$$\frac{V_{AA}}{R_0 C_S} < \left(\frac{dV_A}{dt} \right)_M, \quad (3.86)$$

from which the value of capacitance C_S is calculated. For a given thyristor (dV_A/dt) is an item of the catalog specifications. In order to reduce the discharge current of C_M at the beginning of thyristor conduction, the resistor R_S is added (dotted lines in Fig. 3.30a).

The effect of the two protection methods of Fig. 3.30 is the same. The difference is in that R_g in Fig. 3.30b is external whereas in Fig. 3.30c this is the resistance of the P_2 region which is on one side short circuited by the cathode (denoted by K_S in Fig. 3.30c). In both cases a part of the capacitive current is shunted through this resistor to the cathode. This reduces the emitter current of T_n and therefore the gain α_n . A thyristor with the short circuited emitter (Fig. 3.30c) could have a very large breakpoint voltage V_{PMO} (over several thousands volts) at the open gate because the gain α_n is very small.

The effect of reducing α_n can be explained by the two-transistor model of a thyristor in terms of the resistor R_S between the gate and the cathode. Excluding the short circuited emitter the gain is

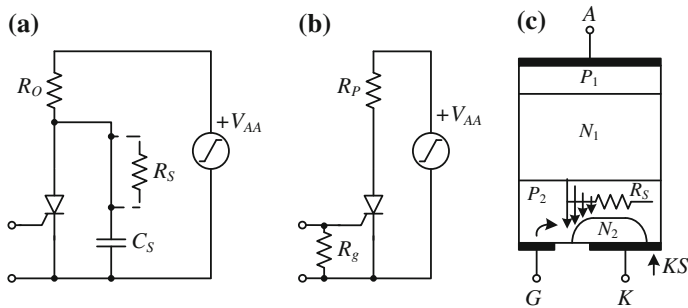


Fig. 3.30 Protection (snubber) circuits (a and b) and the thyristor having short circuited emitter for the purpose of reducing the dv/dt effect (c)

$$\alpha_n = \frac{I_{cn} - I_{con}}{I_{En}} = \frac{I_{cn} - I_{con}}{I_K}. \quad (3.87)$$

Including the short circuited emitter, the current I_{En} is, due to the longitudinal resistance R_S , smaller than I_g by the amount of the branching current I_S . Namely

$$I_K = I_{En} + I_S. \quad (3.88)$$

Now, the effective current gain of the transistor T_n can be defined as

$$\alpha_{nef} = \frac{I_{cn} - I_{con}}{I_{En} + I_S} = \frac{I_{cn} - I_{con}}{I_{En}(1 + I_S/I_{En})} = \frac{\alpha_n}{1 + I_S/I_{En}}. \quad (3.89)$$

For small values of R_S , or R_g it is possible that $I_S/I_{En} \gg 1$, thus $\alpha_{nef} \ll \alpha_n$.

Example 3.3

- (a) Determine the values of the elements in Fig. 3.31 in order to provide dv/dt protection of a thyristor if $f = 2$ kHz (switching frequency),

$$S = dv/dt_{(\max)} = 100 \text{ V}/\mu\text{s} \text{ and } L = 50 \mu\text{H}.$$

The input voltage has sharp change from 0 to V_s equal to 200 V.

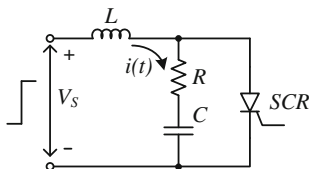


Fig. 3.31 Thyristor snubber circuit

- (b) Determine power losses in the protection circuit.
- (a) After the sharp change of the input voltage, the current through the snubber RC circuit can be described by the following differential equation

$$L \frac{di(t)}{dt} + Ri(t) + \frac{1}{C} \int i(t) dt = V_s.$$

By transformation from time (t) to complex (s) domain one obtains

$$(s^2 + 2\xi\omega_0 s + \omega_0^2)I(s) = V_s/L, \quad (3.90)$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$ and $\xi = \frac{R}{2} \sqrt{\frac{C}{L}}$.

Following the same approach for the voltage on the thyristor, the following expression can be derived

$$v_0(t) = V_s - L \frac{di(t)}{dt}, \text{ where } \tau = CR. \quad (3.91)$$

Solving Eqs. (3.90) and (3.91) and taking into account conditions $i(0) = 0$ and $v_0(0) = 0$ the following expression is obtained for the current i

$$i(t) = \frac{V_s}{R} \frac{2\xi}{\sqrt{1-\xi^2}} e^{-\xi\omega_0 t} \sin \omega t \text{ (A) and for the voltage on the thyristor}$$

$$v_0 = V_s \left\{ 1 - e^{-\xi\omega_0 t} \left[\cos(\omega t) - \frac{\xi}{\sqrt{1-\xi^2}} \sin(\omega t) \right] \right\} \text{ (V) where } \omega \text{ is the oscillation frequency equal to } \omega = \omega_0 \sqrt{1-\xi^2}.$$

If the damping factor is $\xi > 0.5$, for instance $\xi = 0.7$ the maximum rate of the thyristor voltage change is $S = 2V_s\omega_0\xi = V_s R/L$.

From the expression for S it follows $R = \frac{SL}{V_s} = 25 \Omega$.

The capacitance of the snubber circuit is equal to (Fig. 3.45)

$$C = \frac{4\xi^2 L}{R^2} = 158 \text{ nF}.$$

- (b) Losses on the resistor R in the snubber circuit are proportional to accumulated energy in the capacitor C and they are approximately equal to

$$P_R = CV_s^2 f = 12.64 \text{ W}.$$

3.2.1.3 Effect of the Rate of Anode Current Change (di/dt Effect)

Conventionally designed thyristors have a side positioned control electrode (Fig. 3.32c). Immediately upon the action of a positive pulse at the control electrode, the full voltage V_g will appear only at the part of junction J_2 nearest to the

gate terminal. Owing to the voltage drop across the transversal resistance R_S of the region P_2 , the remote parts will be at a lower potential, thus at a lower forward bias. Therefore, at the beginning of conduction, the electron injection from the N_2 region will be marked only in the vicinity of the gate (denoted by an arrow in Fig. 3.32c). This means that at the beginning only a narrow part of the thyristor is conducting whereas the major part is in the off state. Owing to a high current density at this narrow part the dissipation in this part is the highest, which may lead to overheating of the junction and to destruction of the element. This is particularly true for very fast increase of the anode current. Namely, the anode current does not attain a uniform distribution but is concentrated to a narrow conduction region. If the rate of increase di_A/dt is smaller than the maximum permitted $(di_A/dt)_M$, the current due to the regenerative process will be distributed homogeneously across the cross section and therefore no damage to the thyristor will occur.

The power thyristors have a larger surface and consequently larger a cross-section resistance R_S , thus they are more sensitive to the di/dt effect than the low power thyristors. At higher temperatures this effect is more pronounced. Since, $(di_A/dt)_M$ varies from sample to sample, the (di/dt) capability is defined as the worst case. Typical values of di/dt capability are several tens of A/ μ s.

Figure 3.32 shows two designs of thyristors with increased di/dt capabilities. In the first case (Fig. 3.32a) the gate is in the middle, surrounded by the cathode.

In this way, the initial conduction surface of the junction is considerably larger, consequently the initial anode current distribution is more uniform. For power thyristors, however, this improvement is not sufficient. For this reason thyristors having an amplifying gate are designed (Fig. 3.32b). At the gates surrounding the central gate a field is induced making these gates active. Practically, there is one pilot thyristor which controls the operation of the two main thyristors (Fig. 3.32c). In addition to the more homogenous distribution of the anode current, this system allows operation with very small control signals. In fact, the pilot thyristor amplifies the gate signal.

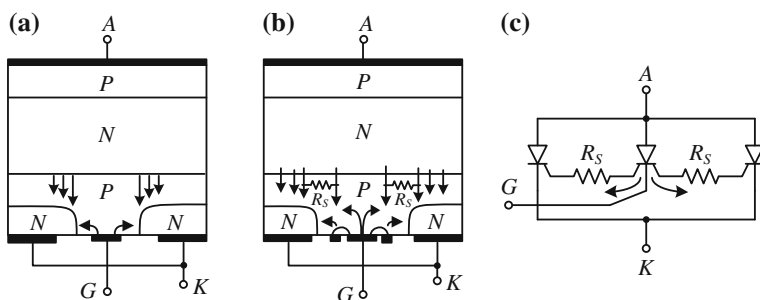


Fig. 3.32 Thyristor with central gate (a) and with amplifying gates (b and c)

3.2.1.4 Turn-On Time

Usually a thyristor is turned on by the gate current. During the turn-on process the anode voltage could be considered constant and $V_{AA} < V_{PMO}$. A test circuit having a resistive load is shown in Fig. 3.33a. If one allows instant increase of the gate current, the turn-on condition by an abrupt current drive is fulfilled. After a certain period, referred to as the turn-on time, the anode voltage and current will attain their stationary values. The turn-on time consists of two parts, the delay time t_d and the rise time t_r .

The delay time t_d is defined as the time required by the anode current to reach 10 % of its stationary value in the state of conduction. This time is a consequence of the finite period required by minority carriers to cross the base-collector regions N_1 and P_2 . Because of this, the regenerative process resulting in increasing of the anode current does not arise immediately. In other words, a certain time is required to allow the carriers to cross certain thyristor regions. The wider the base regions N_1 and P_2 , the longer is the delay time. For high-voltage thyristors, having a wide P_2 base, the time t_d is quite long. In this situation, the thyristor should be turned on by a higher gate current because t_d reduces with an increasing I_G (Fig. 3.33c). During the rise time t_r , the anode current increases from 0.1 to 0.9 I_A . The most part of this period corresponds to the propagation time. It was already mentioned that at the beginning of thyristor conduction only the part of the cathode close to the gate is conducting. The time required for the whole cathode to become conductive is the propagation time. For very powerful thyristors this time may be several hundreds of μ s long. The rise time of the anode current is not only dependent on the thyristor design, but is also load-dependent. For instance, if the load is inductive, the rise time will depend much more on the load inductance than on the thyristor parameters.

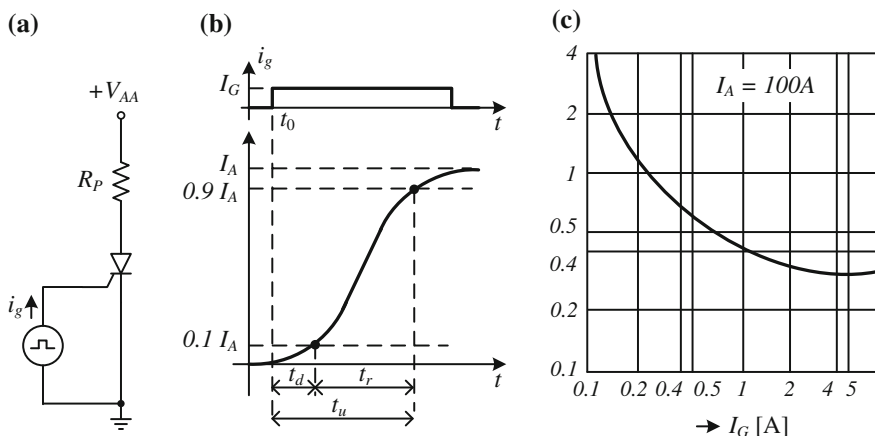


Fig. 3.33 Turn-on test circuit (a), anode current response to abrupt gate drive (b), and delay time as function of gate current at $I_A = 100$ A (c)

3.2.1.5 Turn-Off Time

While a thyristor is on, all p-n junctions are forward biased and both transistors are in saturation. Owing to this, particularly for power thyristors, there are considerable piled-up charges in all four parts of the thyristor. Figure 3.34a shows the corresponding minority carrier distributions. The most part of the charge is stored in the region N_1 because this region is the widest and the least conductive. The concentrations of the minority carriers in the anode and cathode emitters (regions P_1 and N_2) are negligible because the conductivities of these regions are very high. If a thyristor is to be turned off, the piled-up charge has to be cleared away. This is accomplished mainly by cutting off or reversing the bias of the anode circuit. In the case of cutting off the anode circuit, the anode current drops below the holding current. The piled-up charge is cleared away by recombination. Consequently, the turn-off time is quite long. The reversal of the polarity of the anode voltage is the most frequent and the most reliable method of turning off the thyristor. Then, similarly to the processes in diodes and bipolar transistors, the piled-up charge is cleared away by the negative anode current. The larger this current, the faster clearing away. Figure 3.34b shows the response of the anode current to an abrupt change of the anode supply voltage from $+V_{AA}$ to $-V_{AA}$. In the interval from t_0 to t_1 the anode current is negative, determined by the external elements of the circuit. Within this time the minority carrier concentration at the junction J_3 drops to zero. In the interval from t_1 to t_2 the anode current reduces because the voltage at junction J_3 increases. This interval is very short because the breakdown of these junctions of only several volts occurs very quickly. After this, in the interval from t_2 to t_3 clearing away of the carriers from the junction J_1 is continued. The anode current during this interval is constant. At the instant t_3 the minority carrier concentration at the junction J_1 is zero. After that the anode current decreases until the capacitance of the reverse biased junction J_1 is charged, when $i_A = 0$.

The time from t_0 to t_4 is the thyristor recovery time t_c . However, the thyristor is still not off. Namely, although the external junctions are reverse biased, the concentrations of the charge carriers in the N_1 and P_2 regions are above their static

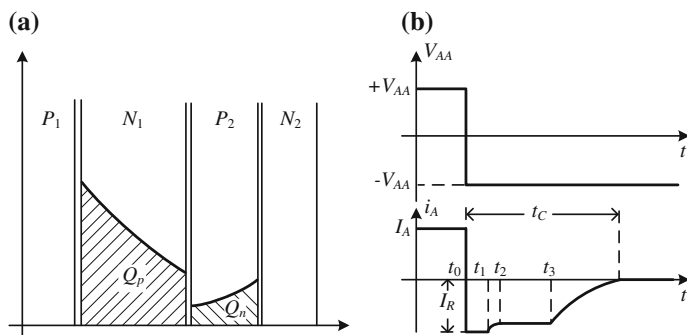


Fig. 3.34 Distribution of minority carriers in a conducting thyristor (a) and the response of the anode current to the reversal of the anode voltage (b)

levels because the junction J_2 is forward biased. Owing to this, in case of a forward bias of the anode circuit, the thyristor would be switched on at anode voltages below V_{PMO} . In other words, the thyristor is still not capable of blocking a positive anode voltage. It is able to do that only if the excess minority carriers around the junction J_2 are cleared away. This clearing away is accomplished by recombination because the anode current is negligible. Consequently, the turn-off time t_i of a thyristor is the elapsed time from the reverse bias of the anode circuit until the thyristor is again capable of blocking a positive anode voltage at the maximum permitted value and at the maximum permitted rate of its change. Typically, it is several tens of μs , and for fast thyristors it is of the order of $1 \mu s$. It should be emphasized that the gate voltage will influence the turn-off time: it will increase it if positive or decrease it if negative. This is understandable because a positive voltage supports the regeneration within a thyristor and negative, by extracting the positive charge from the P_1 region, suppresses the regeneration.

Figure 3.35 shows the responses of the anode current and voltage to a real current drive of the gate during the turn-on and the anode supply voltage during the turn-off processes. Upon the polarity of the anode voltage being reversed, the anode current is also reversed.

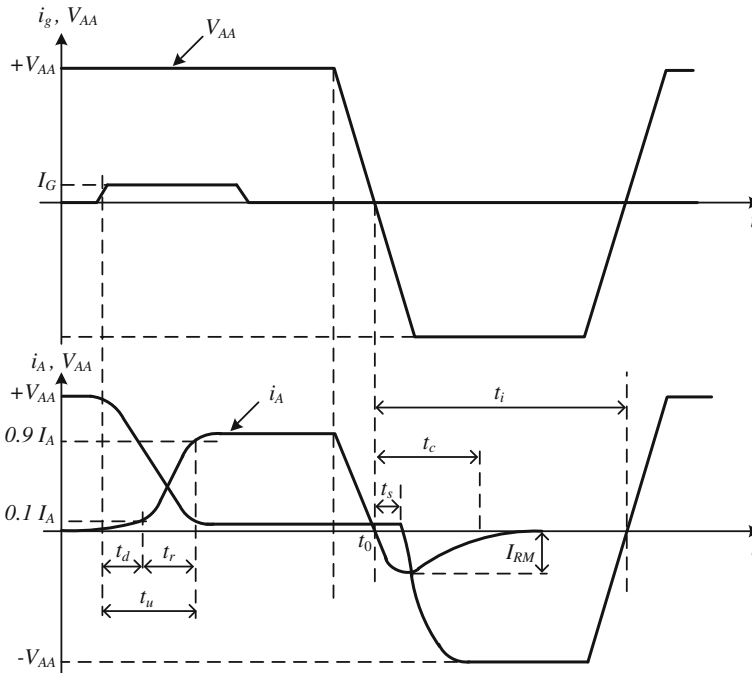


Fig. 3.35 Responses of anode current and voltage to real driving currents of the gate and anode supply voltage

The anode voltage remains unchanged during the time interval t_s . This interval corresponds to the interval t_0 to t_1 (Fig. 3.34b). During t_s the anode current reaches its maximum negative value I_{RM} .

3.2.1.6 Turning On (Triggering) and Off

In principle, switching circuits can be divided into two groups: the circuits fed by the anode circuit of the thyristor and the circuits having a completely separate source of triggering signals. A triggering signal could be DC, low frequency, or pulsed. A power supply having thyristor-controlled load current could be DC or AC. As it has already been mentioned, turning off of the thyristor is not carried out by the gate but by the anode circuit, except for a special type of thyristors (GTO). The most reliable way of turning off is by applying a reverse bias to the anode-to-cathode circuit. In an AC power supply this is carried out automatically, at the beginning of the negative half-cycle. For a DC power supply, however, turning off is more complicated. It is usually done by one of the three methods (Fig. 3.36).

The least used method is turning off by breaking the anode current (Fig. 3.36a) because the switch Pr , either mechanical or semiconductor, has to be very powerful. In addition, during the switch-on of Pr , as a consequence of a sudden anode voltage change, the undesired triggering of the thyristor may occur.

Turning off by short circuiting the thyristor (Fig. 3.36b) is the simplest, but not the most reliable. The transistor is on only for a short while, so it can be low power. When on, it should take upon itself the major part of the anode current so that it drops below the holding current value ($I_A < I_H$)

$$\frac{V_{AA} - V_H}{R_0} - \beta I_B < I_H. \quad (3.92)$$

A reverse biased anode is the most reliable method of turning off. This is accomplished by adding a low power thyristor SCR_2 and a commutating capacitor

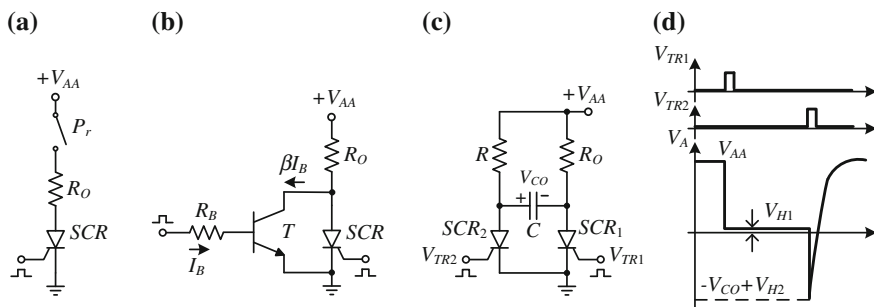


Fig. 3.36 Methods of turning off the thyristor in a DC power supply by breaking the anode current (a), short circuiting the thyristor (b), reverse biased anode (c) and the voltage waveforms in characteristic points (d)

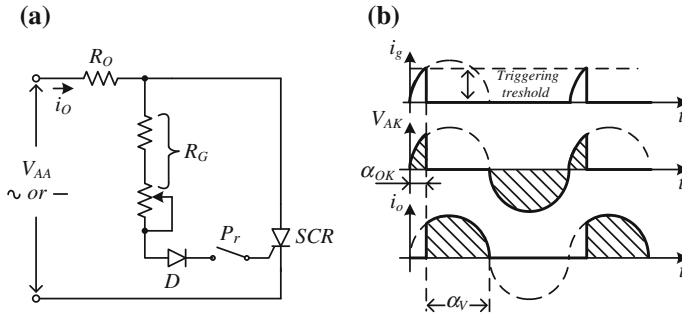


Fig. 3.37 Triggering circuit fed from a common supply (a) and the waveforms of the gate and load currents and the anode-to-cathode voltage for an AC supply (b)

C (Fig. 3.36c). The main thyristor SCR_1 is turned off by turning on the auxiliary thyristor SCR_2 . Namely, while SCR_1 is on, SCR_2 is off and the capacitor is charged through R in the direction indicated in Fig. 3.36c. By triggering SCR_2 the anode voltage of SCR_1 becomes negative (Fig. 3.36d) leading to turning off of SCR_1 . Instead of SCR_2 it is possible to use a transistor (bipolar or MOS).

In the design of triggering circuits there is no significant difference whether the supply is AC or DC. Figure 3.37a shows a simple triggering circuit involving a front-resistor fed from a common power supply. The diode D is used only with an AC supply in order to block the negative half-cycle. With a DC supply the thyristor is triggered by turning on the switch P_r . In case of an AC voltage V_A , triggering can be accomplished without the switch P_r . The instant of triggering, by adjusting the gate current required for triggering (Fig. 3.37), is programmed by the resistance R_G . By R_G it is possible to achieve that the SCR is completely nonconductive or that it conducts at least during a half-cycle up to a full cycle. Thus, the angle of conduction can be varied within limits. Figure 3.38b shows the waveforms of the characteristic currents and voltages of an AC supply.

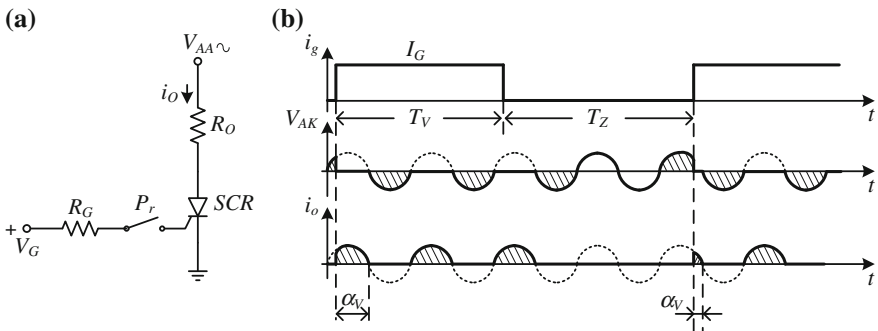


Fig. 3.38 Triggering circuit having separated supplies (a) and the anode voltage and current for an AC supply when the thyristor is a static switch (b)

If the supply of the triggering circuit is separate (Fig. 3.38), the angle of conduction can practically be controlled within limits $0^\circ \leq \alpha_v \leq 180^\circ$. Moreover, it is often required that the thyristor is conducting for a certain number of half-cycles and then blocked for another number of half-cycles (Fig. 3.38). The switch Pr serves for controlling the intervals of conduction T_v and blocking T_z . The resistance R_G should be chosen so that the thyristor is triggered at the minimum voltage V_{AA} . In these applications the thyristor is often called the static switch.

3.2.1.7 Triggering Circuits Based on UJT

The basic pulse generator circuit using an unijunction transistor belongs to the group of the most popular thyristor triggering circuits. In this application the output from the base $B1$ of the UJT is connected to the gate of the thyristor, directly (Fig. 3.39a) or by a pulse transformer (Fig. 3.39b) or an optocoupler. The instant of triggering is adjusted by the timing elements R_E and C_E . After the UJT is switched on, each pulse can trigger the thyristor at a positive anode voltage. The voltage across R_1 , when the UJT is off, has to be below the minimum triggering voltage of the thyristor, i.e.,

$$R_1 I_{BB} < V_{GKmin}, \quad (3.93)$$

where

$$I_{BB} = \frac{V_{BB}}{R_{BB} + R_2 + R_1}. \quad (3.94)$$

Since $R_{BB} \gg R_1 + R_2$, from (3.92) and (3.93) it follows

$$R_1 < \frac{V_{GKmin}}{V_{BB}} R_{BB} = R_{1max}. \quad (3.95)$$

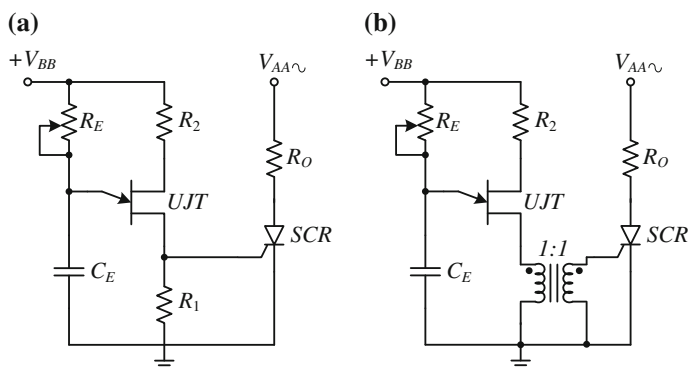


Fig. 3.39 UJT-based oscillators for thyristor triggering

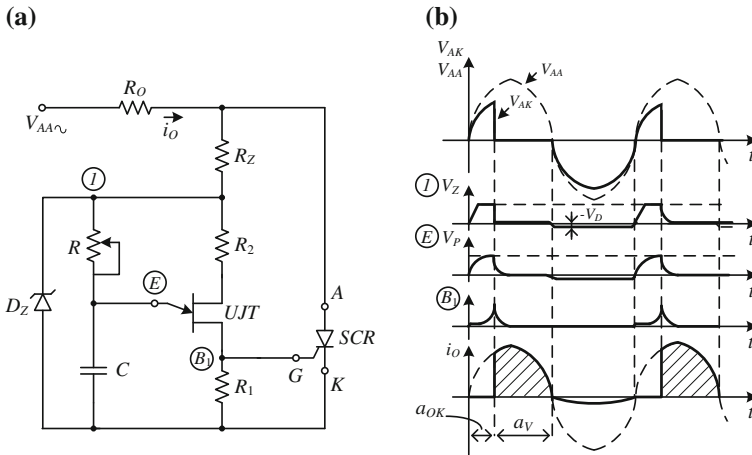


Fig. 3.40 UJT based oscillator in a phase controlled circuit (a) and the characteristic waveforms (b)

For instance, if $V_{BB} = 24$ V, $R_{BB} = 6$ k Ω , and $V_{GKmin} = 0.4$ V, then $R_{1max} = 100$ Ω .

The triggering circuits from Fig. 3.39 require a separate power supply V_{BB} . In the phase controlled circuits the triggering circuit is fed from a common AC supply (Fig. 3.40). Here the oscillator is fed by a Zener diode and a common resistor R_Z . The first oscillator pulse turns the thyristor on. The voltage across it reduces to approximately 1 V so that the oscillator is cut from the supply and stops generating pulses. Thus, the gate current exists only until the thyristor is switched on. During the negative half-cycle the Zener diode operates as a forward biased diode. Owing to this a negative current will flow through the load. However, since $R_Z \gg R_O$, this current is very low. The operation of the circuit from Fig. 3.40 is illustrated in Fig. 3.40b. The phase control (variation of the angle of conduction) is accomplished by the variations of the timing elements R_E and C_E .

It is often required that the triggering circuit is galvanically separated from the primary source. This is accomplished by a mains transformer (Fig. 3.41). Here the oscillator is fed throughout the positive half-cycle. Then it generates triggering pulses. However, only the first triggering pulse is active. All others are passive and have no influence since the thyristor is on. Thus, the angle of conduction is controlled by the timing elements R_E and C_E . During the negative half-cycle D_z is forward biased and it cuts the oscillator supply. Meanwhile, the capacitor C_E is discharged so that the synchronism is automatically established (triggering at the same instant during each half-cycle) since C_E charges from the beginning during each positive half-cycle. The resistance R_g reduces the influence of noise in the gate

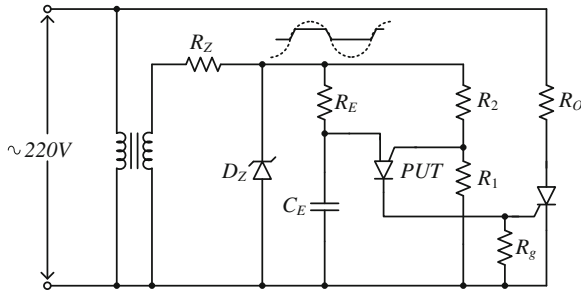


Fig. 3.41 Galvanically separated triggering circuit based on PUT in a phase controlled circuit of a half-wave rectified voltage

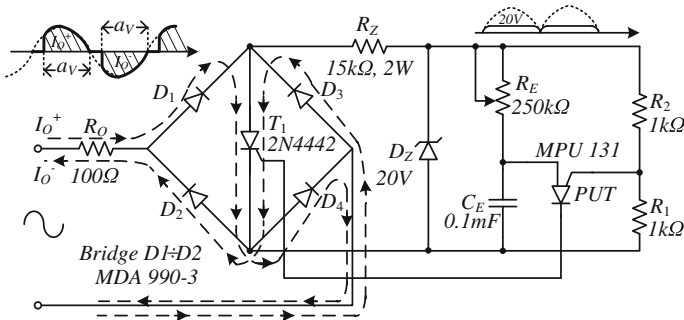


Fig. 3.42 Phase control in a full-wave rectifier

circuit and it ranges from one hundred Ω up to several k Ω . Here it is not necessary since the resistance R_1 is in a UJT-based oscillator, thus the current of a PUT in the off state is considerably lower and cannot turn-on the thyristor.

In the circuits analyzed so far the thyristor was connected in a half-wave rectifier circuit. The circuit from Fig. 3.42 controls the phase in both half-cycles of the load current. The diode bridge D_1-D_4 rectifies the negative half-cycle and feeds the PUT based oscillator during both half-cycles. The first triggering pulse from the oscillator, either in the positive or in the negative half-cycle, turns on the thyristor and it conducts until the mains voltage changes the polarity. By varying the cycle of the oscillator from 1 to 7.8 ms, the angle of conduction is controlled within limits from 21.6° up to 168.5° .

Example 3.4 For the circuit from Fig. 3.43 determine:

- the value of the resistance R_x so the average value of the current through the load R_p , L_p is 5 A, and
- the average value of the current through the diodes in the diode bridge.
- Sketch the voltage waveforms in the marked points.

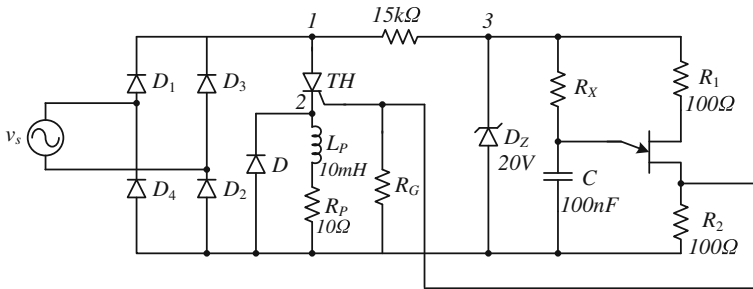


Fig. 3.43 An example of phase control of full-wave rectifier

Remark, $v_s(\omega t) = \sqrt{2} \times 220 \sin(2\pi 50t)$, $\eta = 0.6$.

- The angle γ at which the Zener diode is turned on is determined from the condition $V_{SM} \sin \gamma = V_Z \Rightarrow \gamma = \arcsin \frac{V_Z}{V_{SM}} = 0.064$ rad.

The thyristor angle of triggering is determined from the condition that the desired average current through the load is

$$I_0 = \frac{1}{\pi} \int_{\alpha}^{\pi} \frac{V_{SM} \sin(\omega t)}{R} d(\omega t) = \frac{V_{SM}}{R\pi} (1 + \cos \alpha),$$

where α is the angle of triggering.

From the expression for the average value of the load current, the value of the angle α is calculated as

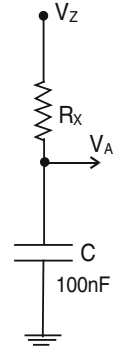
$$\alpha = \arccos \left(\frac{I_0 R \pi}{V_{SM}} - 1 \right) = 2.08 \text{ rad.}$$

Based on the calculated angle α , the RC time constant is determined as

$$t_a = \frac{\alpha}{\omega} = \frac{\alpha}{2\pi 50} = 6.62 \text{ ms.}$$

The capacitor charging circuit which generates the required time constant is shown in Fig. 3.44.

Fig. 3.44 RC circuit for generation of the required time constant



Since, the angle γ is very small it can be considered that the Zener diode leads at the beginning of each period of the diode rectifier output voltage. The anode voltage V_A of a unijunction transistor is equal to

$$V_A(t) = V_Z - V_Z e^{-\frac{t}{R_X C}}.$$

The resistance R_X is determined from the condition for the desired angle of the thyristor triggering.

$$\begin{aligned} V_A(t_a) &= V_{Dk} + \eta V_{B_2 B_1} \\ &\approx \eta V_{B_2 B_1} = \eta V_Z. \end{aligned}$$

From the expression for the voltage on the anode of the unijunction transistor and the conditions for the unijunction transistor turn-off, next expressions are obtained

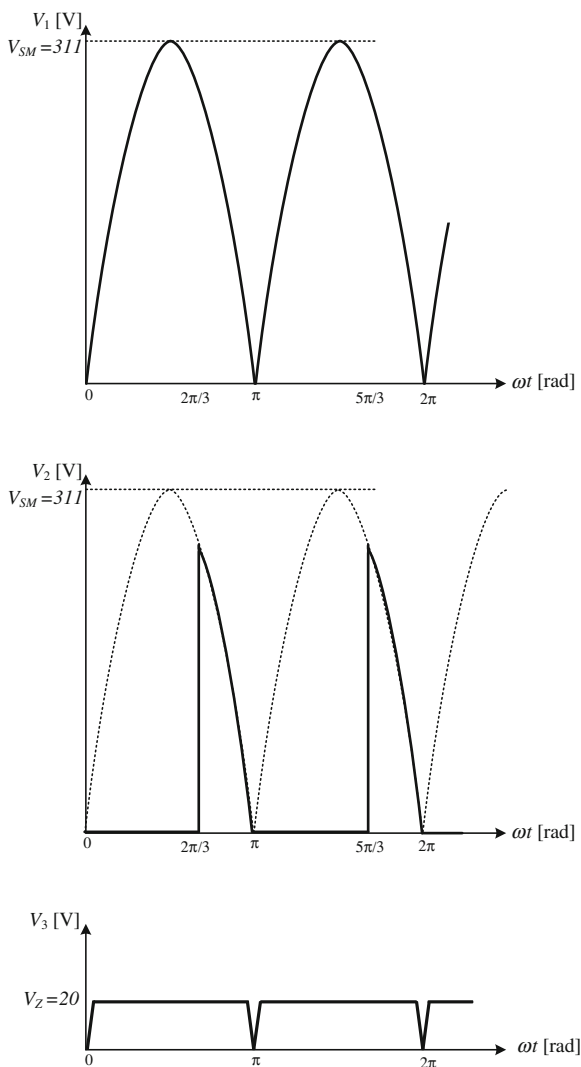
$$\begin{aligned} t_a &= R_X C \ln \frac{1}{1 - \eta}, \text{ and} \\ R_X &= \frac{t_a}{C \ln \frac{1}{1 - \eta}} = 72.25 \text{ k}\Omega. \end{aligned}$$

(b)

$$I_{Dsr} = \frac{I_0}{2} = 2.5 \text{ A}.$$

(c) Voltage waveforms of marked points 1,2 and 3 of circuit from Fig. 3.43 are shown in Fig. 3.45.

Fig. 3.45 Voltage waveforms of marked points 1, 2 and 3 of circuit from Fig. 3.43



3.2.2 Gate Assisted Turn-Off Thyristor

A Gate Assisted Turn-off Thyristor (GATT) is a thyristor where the turn-off process is gate assisted. It is mainly used at high frequencies. Namely, the turn-off time of conventional thyristors could be as high as several tens of μs , which reduces considerably the useful frequency range. This is particularly true of the high-voltage (over 1,000 V) thyristors. A GATT operating at voltages in excess of 1,000 V could have a turn-off time of only several μs . The acceleration of the turn-off process is accomplished by applying a negative bias to the gate. This helps clearing away the

piled-up charge in P_2 base and eliminates the possibility of a forward bias at the junction J_3 .

Like a thyristor having an increased dv/dt capability, GATT makes use of the cathode-emitter short circuits and for more powerful components distributed or inter-digital gates are applied. Since turning on of thyristors having inter-digital gates requires high gate currents, GATTs are usually designed with amplifying gates. Their structure is similar to that shown in Fig. 3.32 except that they have two turn-off electrodes. The auxiliary electrode is connected to the main (central) electrode via a (bypass) diode. During turn-on this diode is reverse biased and during turn-off it is conducting and bypasses the “pilot” thyristor. The bypass diode can be external or integrated.

3.2.3 Asymmetric Thyristor

Asymmetric Semiconductor Controlled Rectifier (ASCR) is an asymmetric thyristor. It has a very narrow n-base. Owing to this its reverse breakdown voltage is only 20–30 V. However, narrowing the base reduces the on voltage and the turn-on time. Thanks to this the power losses in ASCR are smaller than those of conventional thyristors.

3.2.4 Reverse Conducting Thyristor

Owing to the small reverse breakdown voltage of ASCR, an anti-parallel diode is usually connected. An Reverse Conducting Thyristor (RCT) is a reverse conducting thyristor having an integrated anti-parallel diode. Its cross section and symbol are shown in Fig. 3.46. Practically a fast thyristor and a fast diode are integrated into a single component. The reverse voltage of the thyristor is equal to the forward

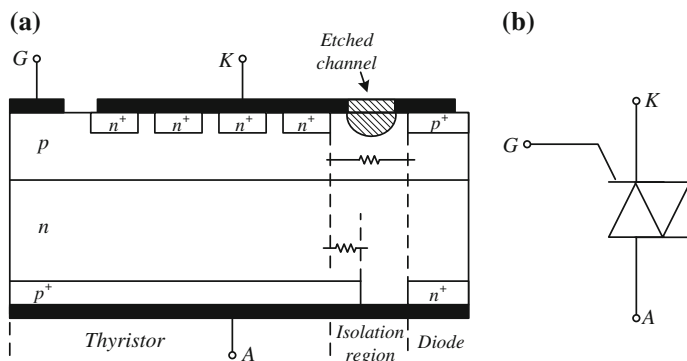


Fig. 3.46 Cross section (a) and symbol of a reverse conducting thyristor (RCT) (b)

voltage of the diode. The basic problem in designing a reverse conducting thyristor is that between the diode and the thyristor region good isolation is required. This isolation blocks the penetration of the excess charge carriers from the conducting diode to the thyristor which could cause a considerable slowing down of the thyristor turn-off process. The isolation is accomplished by introducing a high-resistance region between the components in the p and n bases.

3.2.5 Gate Turn-Off Thyristor

A gate turn-off thyristor (GTO) is a thyristor which is turned on or off by the gate. Its cross section, two-transistor model, and symbol are shown in Fig. 3.47. Turning off is achieved by a negative gate current. In order to initiate the regenerative process, both transistors during turn-off have to be in the active region. Thus, the base current of T_n has to be lower than the saturation base current, i.e.,

$$I_{Bn} = \alpha_p I_A - I_G \leq I_{Bns} = \frac{(1 - \alpha_0) I_A}{\beta_n}. \quad (3.96)$$

From (3.96) it follows that the minimum gate current, required for turning off the thyristor, is determined by

$$I_G \geq \frac{\alpha_p + \alpha_n - 1}{\alpha_n} I_A. \quad (3.97)$$

Consequently, it is possible in principle to turn-off any thyristor by the gate. However, for this a very high gate current, even higher than the anode current, would be required. For instance, if $\alpha_n = \alpha_p = 0.95$, then, according to (3.97),

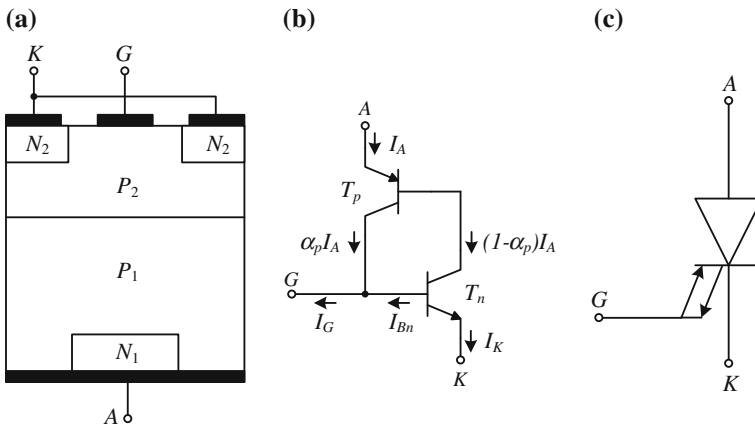
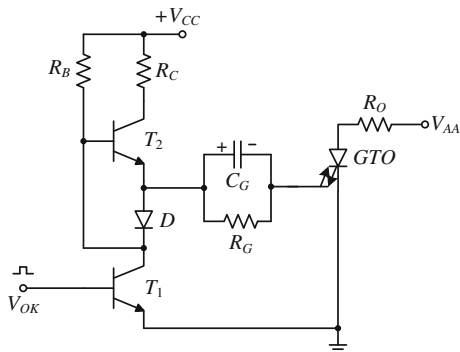


Fig. 3.47 Cross section (a), two-transistor model (b), and symbol of GTO thyristor (c)

Fig. 3.48 Triggering circuit of a GTO thyristor



$I_G > 0.95 I_A$. The ratio of the anode and the gate current required for turn-off is often called the turn-off current gain and is determined by

$$A_I = \frac{I_A}{I_G} = \frac{\alpha_n}{\alpha_n + \alpha_p - 1}. \quad (3.98)$$

For conventional thyristors $A_I \approx 1$. In order to make the gate turn-off process practically possible, the condition $A_I \gg 1$ has to be met. This, according to (3.98), means that the sum of current gains α_n should be approximately 1, but $\alpha_n + \alpha_p > 1$ and α_p should be as small as possible. If, e.g., $\alpha_n = 0.8$ and $\alpha_p = 0.21$, then $A_I = 80$.

High α_n and low α_p in GTO thyristors are technologically accomplished in several ways. The cross section of the structure of a GTO thyristor is shown in Fig. 3.47. The p-emitter surface is small, so α_p is small. On the other hand, the n-emitter surrounds the gate, so its effective surface is large and consequently α_n is large.

If the standard circuit for triggering GTO thyristor (Fig. 3.48) is used, turn-on is accomplished by the trailing edge and turn-off by the leading edge of the triggering pulse fed to the base of the transistor T_{r1} . The capacitor C_g plays the same role as a speed-up capacitor in the base of a bipolar transistor. It allows a large initial gate current in both turn-on and turn-off phases of a GTO thyristor. While $V_{ok} = 0$, T_{r1} is off, whereas T_r and the thyristor are on. The capacitor C_g is charged in the direction denoted in Fig. 3.48. The gate-cathode of the thyristor is reverse biased exactly by this voltage and provides a negative gate current which turns off the thyristor when T_{r2} is off and T_{r1} is on ($V_{ok} = V_{BB}$).

3.2.6 MOS Thyristor

An MOS-Controlled Thyristor (MCT) is a thyristor controlled by an MOS transistor. It is often denoted as an MOS SCR. Its fabrication belongs among the new thyristor technologies. The transistor model of an MCT is shown in Fig. 3.49. By

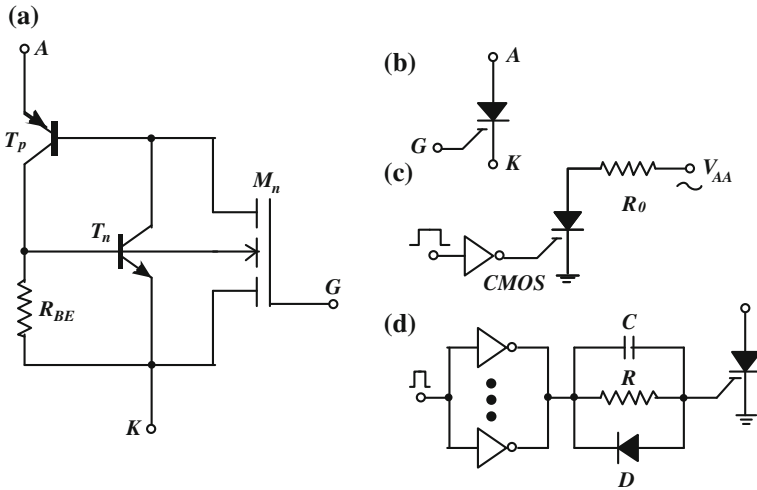


Fig. 3.49 Transistor model (a), symbol (b), and CMOS drive of MCT: simple (c) and optimum (d)

feeding a positive pulse to the gate of the NMOS transistor, M_n , the regenerative switch made up of a complimentary pair of transistors T_n and T_p is turned on. As soon as M_n is on, T_p is also on. Its collector current makes a voltage drop across the resistance R_{BE} which turns on T_n . Then, the regenerative process is started and the triggering pulse does not have any effective influence. A significant feature of MCT is that the input resistance of the gate is very high (of the order $10^9 \Omega$), so it can be driven by very low power signals. Thanks to this it can be driven directly by the output of a CMOS buffer (Fig. 3.49c). The input of an MOS transistor is of a capacitive nature. Due to this the gate voltage change is exponential which slows down the turn-on process. In order to accelerate the process of charging of this capacitor, a circuit with several buffers connected in parallel is usually applied. If an abrupt drive of the gate is required, and this is the case when the triggering pulse is very narrow, a speed-up capacitor is used (Fig. 3.49d).

In parallel with this capacitor a resistor R and a diode D are connected in order to allow discharging of the capacitor C and provide a low impedance between the gate and the cathode of the thyristor in the on state. The resistance ranges from 1 k Ω up to several tens of k Ω , and the capacitance from 1 to 10 nF.

3.2.7 Insulated Gate Control Thyristor

The Insulated Gate Control Thyristor (IGCT) is a powerful semiconductor device. Its characteristics are similar to those of the GTO thyristors, whose turning on and off is controlled by the gate current. Unlike the GTO thyristor, IGCT have much

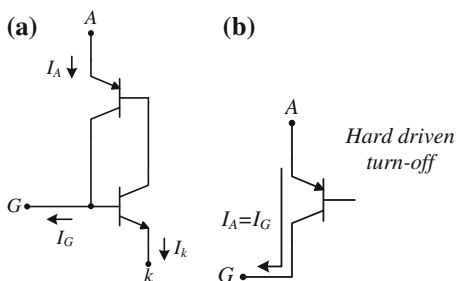
greater turning off gate current than the GTO, which results in complete elimination of minority carriers from the lower p-n junction and a shorter turn-off time. The idea was to get a switching component with a low voltage drop and low losses in the on state, and the ability to rapidly turn-off with minimal switching losses. This means that such a switch in the on state should behave as a rectifier, a low resistance of conductive structure, should have a low value of the anode-cathode voltage, and during the turning off process it should behave as a transistor in order to achieve good dynamic characteristics.

It is known that the turning off of the GTO transistor can be realized by the gate current. The goal is to have a turn-off time as short as possible. While a GTO is turning off, the gate current is sharply increasing (close to the anode current) before the anode voltage begins to rise. In this case, known as the “unity gain turn-off”, or “hard-driven” [1] NPN transistor turns off the first (Fig. 3.50a), and then a PNP transistor with open base assumes the basic function of turning off the GTO thyristor (Fig. 3.50b). If the storage time of the GTO thyristor (the time from the moment when negative voltage between the gate and the cathode appears to the moment when the thyristor anode voltage start to rise) is t_s , the negative voltage between the gate and the cathode. When the thyristor is turned off gate voltage is V_{Goff} , and the total inductance of gate is L_{Gt} . Then the maximum turning off current is

$$I_{\text{GMoff}} = \frac{V_{\text{Goff}} t_s}{L_{\text{Gt}}}. \quad (3.99)$$

Based on (3.99), it can be concluded that the maximum turn-off current can be increased by increasing the voltage V_{Goff} and the time t_s , and reducing the inductance L_{Gt} . Using the state-of-the-art technology it is difficult to increase V_{Goff} and t_s , so the only solution is to reduce the L_{Gt} . The reduction of the gate inductance is achieved by the special technology of IGCT, so the maximum turn-off current can be 1,000 A and more. IGCT is made of two basic components. One is a GCT thyristor placed in a disk case (similar to the GTO thyristor) and the other is a gate unit, placed as close as possible to the GTO on the same printed circuit board (Fig. 3.51).

Fig. 3.50 Two transistors model (a) and hard driven turn off of GTO thyristor (b)



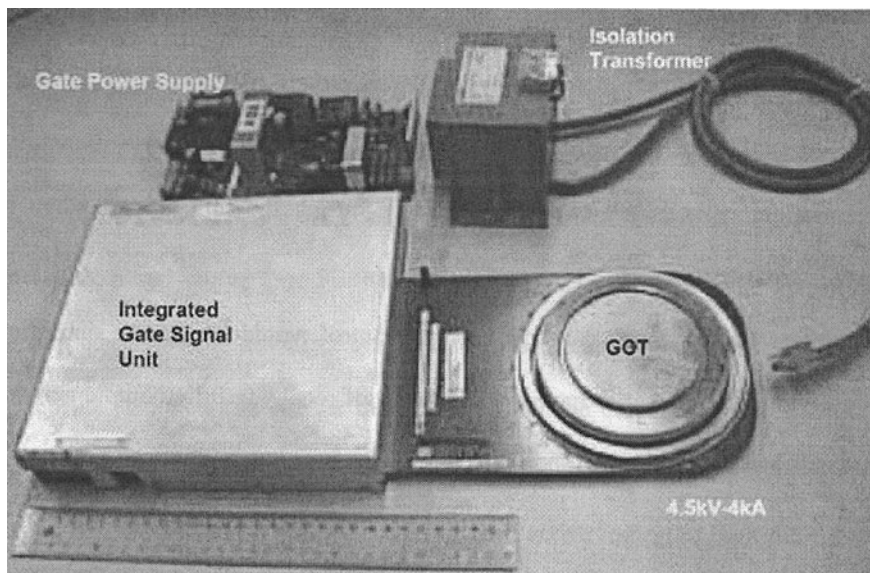


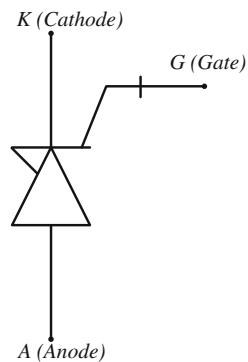
Fig. 3.51 IGCT [1]

This design reduces the total inductance of the gate by up to 100 times (order of a few nH) compared to the GTO thyristor and according to (3.99) increases the turn-off gate current so this current approaches close to the anode current, the “unity gain turn-off.”

The symbol of IGCT and the waveforms of the current and the voltage for a typical IGCT 600A/700 V during its turning off are shown in Figs. 3.52 and 3.53, respectively.

Typical waveforms of the IGCT current and the voltage during transition from the thyristor mode operation (condition state) to the transistor mode (transient process during turning off) are shown in Fig. 3.53. Upon receiving the control

Fig. 3.52 Symbol of IGCT



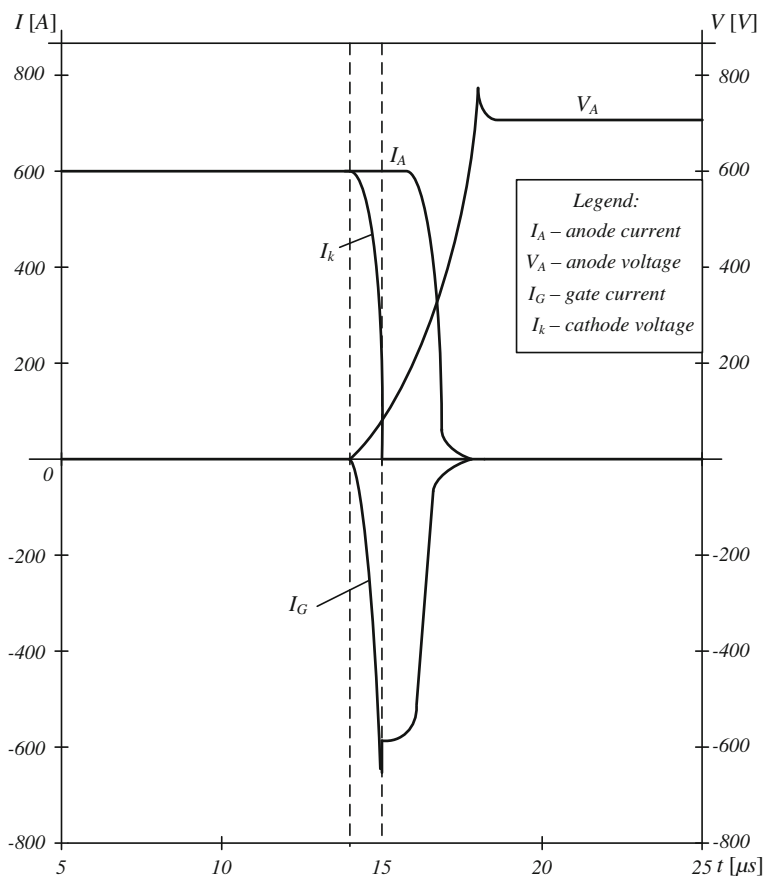


Fig. 3.53 Waveforms of current and voltage for a typical IGCT 600 A/700 V during its turning off

pulse, the cathode current and the gate current rapidly decrease (absolutely increasing). When the cathode current drops to 0, the anode voltage begins to increase. At the same time the anode current is sharply decreasing, and the gate current increases (IGCT is turning off). In the steady state when the IGCT is turned off $I_A = 0$, $I_G = 0$, $I_K = 0$, and V_A has a value of the anode voltage in the off state.

The gate has a specially designed power supply unit. This is a low voltage source connected via an isolation transformer to the gate unit that is usually at a different voltage relative to the source (Figs. 3.51 and 3.54).

This can be a problem if the IGCT is used in high-voltage converters, because the necessary isolation transformers are larger, and it is often difficult to apply a reliable method of isolation. Also, an external power source increases the price and decreases the efficiency and reliability of the system.

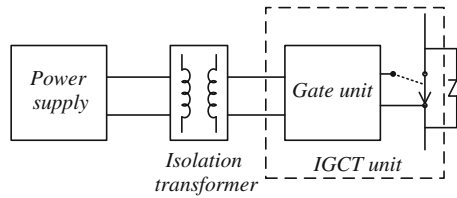


Fig. 3.54 Gate powered by low voltage through isolation transformer

In relation to the GTO thyristor the IGCT has the following advantages:

- higher dv/dt capability,
- no need for a turn-off snubber circuit,
- lower switching losses and
- significant reduction of the turn-on and the turn-off time (the ability to work at a higher frequency than the GTO).

Some of the areas where IGCT is applied are:

- frequency converters,
- current or voltage inverters,
- high power electric motor drives,
- resonant serial or parallel inverters and
- power system protection.

3.2.8 Emitter Turn-Off Thyristor

The emitter turn-off thyristor (ETO) is a hybrid high power MOS-GTO component (device). Compared to the GTO thyristor it has a higher nominal current, voltage, and the ability of gate control via MOS transistors. In this way, it provides low power consumption of the control circuit. In addition to this, it is characterized by an operating frequency greater than the GTO and IGCT, a wider working area for inverse polarization, lower conduction losses, significant turn-off capability, built-in current sensitivity and low cost.

The symbol and the equivalent circuit of ETO are shown in Figs. 3.55 and 3.56, respectively. The emitter switch Q_e is connected in series with the GTO thyristor and the switch Q_g is connected with the gate.

Each of these switches comprises a number of MOS parallel connected transistors in order to increase the current capability.

The ETO thyristor is turned on by turning on the switch Q_e , turning off the switch Q_g and injection gate current into GTO thyristor through G_2 . The applied voltage V_{Q_e} directs the cathode current toward the gate. The voltage V_{Q_e} can be close to the breakdown voltage of the MOS transistor which is significantly larger

Fig. 3.55 ETO thyristor symbol

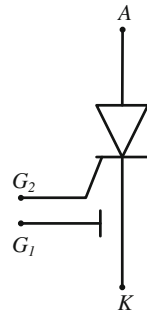
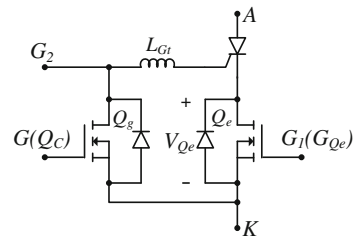


Fig. 3.56 ETO thyristor equivalent circuit



than the maximum voltage gate-cathode (V_{Goff}). In this way, it is possible to realize an equally high gate current of the ETO thyristor as that of an IGCT with a higher inductance in the contour of the gate. This means that in the ETO thyristor design is not necessary to implement special procedures to obtain a low L_{Gt} , as is the case with IGCT's.

Waveforms of currents and voltages during turning off of a 1.4 kA/2.5 kV ETO device are shown in Fig. 3.57. The mechanical and the electrical design of ETO thyristors are continuously improving in order to achieve better characteristics, especially the reduction of the gate inductance, the increase of the operating frequency and the improvement of the device reliability. The new generation of ETO thyristors is shown in Fig. 3.58.

All components except the GTO's are located on the circuit board. The GTO with the printed circuit board is connected to the copper substrate placed on the insulating material. The MOS transistors are placed in a ring around the GTO in order to reduce the inductance of the gate contours and to better remove the heat generated in transistors. Also, the heat generated by a GTO thyristor is effectively removed by the cooling technique from both sides (double side cooling).

The ETO is a powerful switching device designed for applications with currents 1,000 A and more, and voltages up to several 1,000 V, such as powerful drives, systems of protection in power systems, distributed power sources, renewable energy sources, etc.

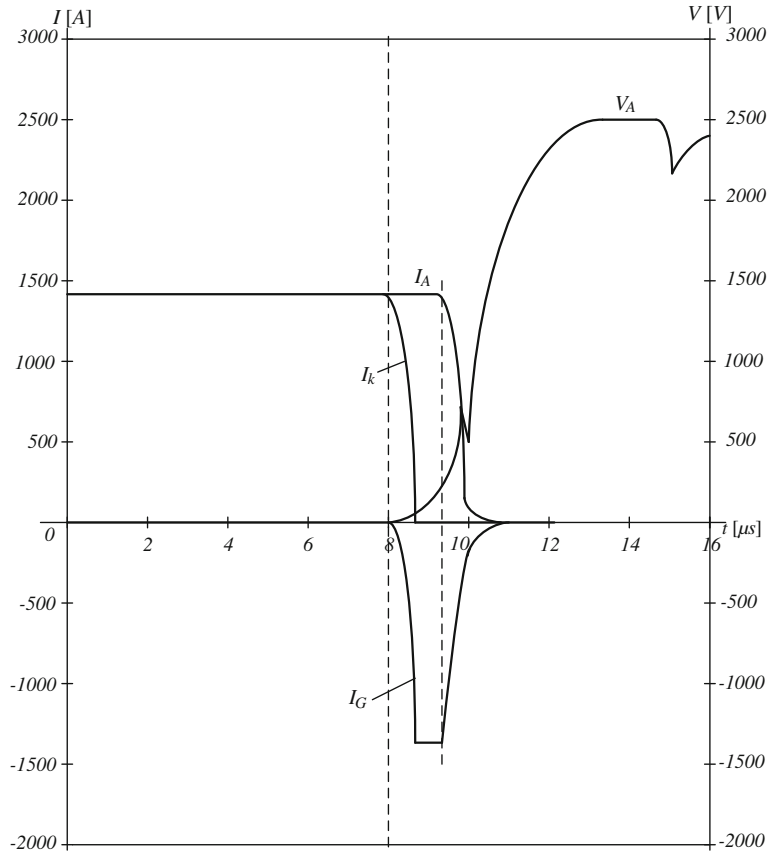


Fig. 3.57 Waveforms of 1.4 kA/2.5 kV ETO thyristor during its turning off

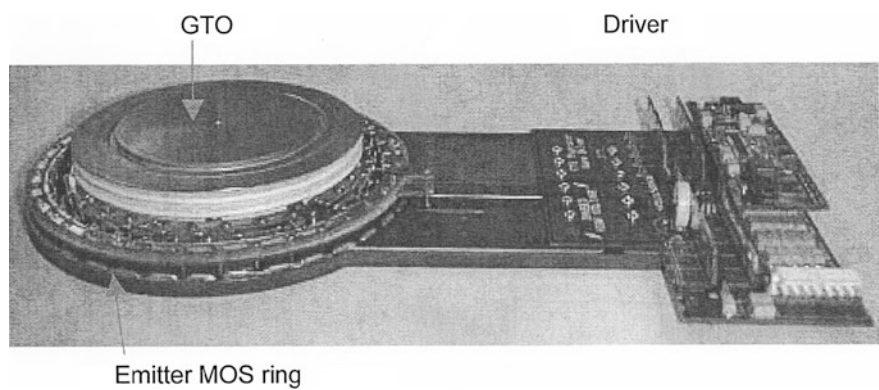


Fig. 3.58 New generation ETO [2]

3.2.9 Photo-thyristor

Photo-thyristors are light-controlled devices. In terms of the electrical and physical characteristics they are identical to the standard thyristors driven by electric signals. Consequently, their applications are exactly the same. The difference is only in the type of drive used. Most of the photo-thyristors also have a gate terminal. It is used for the additional control of the sensitivity by the level of the light signal.

Practically, the only structural difference between a photo-thyristor and a standard thyristor is that in one part of the case, usually on the top cover, the photo-thyristor has a built-in optical lens serving to optically control the thyristor.

3.2.10 Unilateral Switch

A Silicon Unilateral Switch (SUS) is a low power thyristor having the control electrode (gate) on the anode side. Between the gate and the cathode a low voltage Zener diode is built-in. The equivalent model, symbol, and static characteristic are shown in Fig. 3.59.

The structure of a SUS and its characteristic are almost the same as those of a PUT. The difference is only that a SUS has a built-in Zener diode, so its breakpoint voltage is fixed and amounts to

$$V_p = V_Z + V_{EBt} \quad (3.100)$$

where V_Z is the breakdown voltage of the Zener diode and V_{EBt} is the threshold voltage of the PNP transistor. The voltage V_Z ranges from several volts up to several tens of volts.

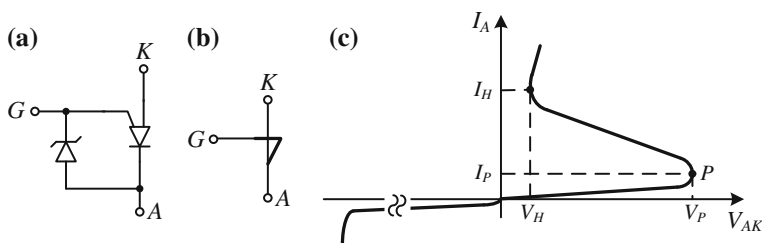


Fig. 3.59 Equivalent model (a), symbol (b), and static characteristic of a unilateral switch (c)

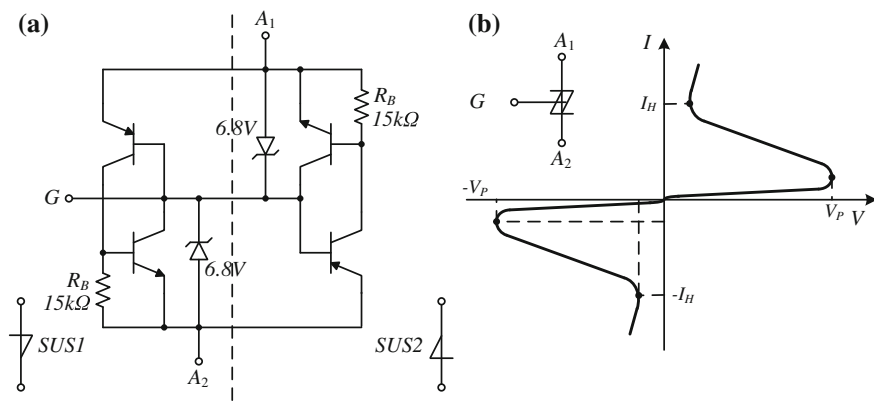


Fig. 3.60 Transistor model (a), static characteristic and symbol of the bilateral regenerative switch (b)

3.2.11 Double Switch—SBS

Compared to the SUS which is capable of only one-directional conduction, an Silicon Bilateral Switch (SBS) is a bilateral (two-directional) switch. Its transistor model and static characteristic are shown in Fig. 3.60. Therefore, an SBS consists of two anti-parallel SUSs. The Zener voltages are equal so the characteristic in the I and III quadrants is symmetric. The breakpoint voltage of the SBS in Fig. 3.60 is $V_P \approx 7.5$ V. The SUS and SBS are low voltage regenerative switches. Although they are manufactured as individual components, they are usually manufactured as an integral part of an integrated circuit. As separate components they are mainly used in the triggering circuits of thyristors and triacs.

3.2.12 Diode Thyristors

The diode thyristors are regenerative switches with two terminals. The breakpoint voltage of a given component is fixed and, like for an open gate thyristor, determined by the breakdown voltage of the central p-n junction. The diode thyristors can be divided into two groups: unilateral and bilateral.

The four-layer diode is a unilateral component (Fig. 3.61). It is often called the Break Over Diode (BOD). Practically this is a thyristor without a gate. It turns on when the anode-to-cathode voltages reaches the break point voltage V_P or when a sudden change of the anode voltage occurs (dV/dt effect). Turning off of the four-layer diode occurs when the anode current decreases to the value of the minimum conduction current I_V , i.e., I_H . Namely, in that case $\beta_n\beta_p > 1$, or $\alpha_n + \alpha_p > 1$ (Fig. 3.61b) like during the turn-on process, so a regenerative process is established. The current I_V is usually within the limits from several mA up to several tens of mA.

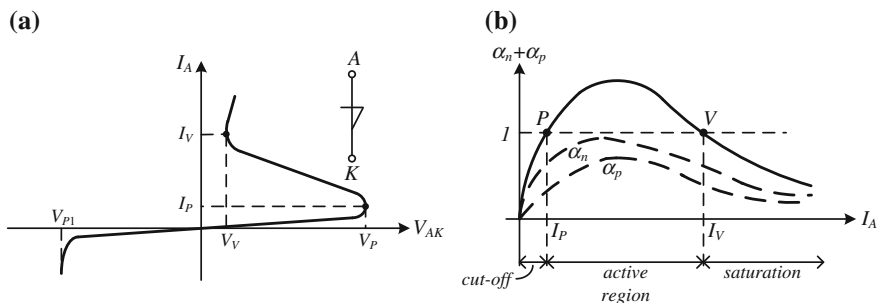


Fig. 3.61 Symbol and static characteristic (a) of a four-layer diode and the operating regions of the current gains of the equivalent complementary transistor pair versus anode current (b)

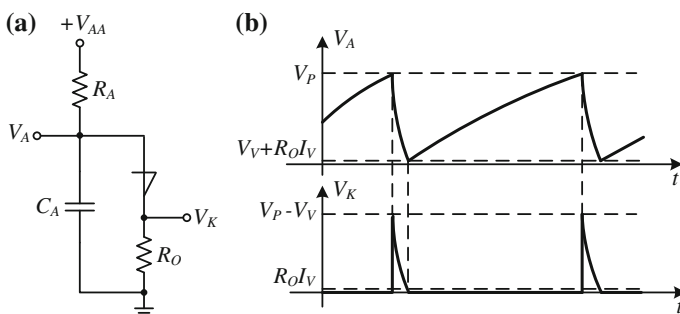


Fig. 3.62 Four-layer diode in an oscillator circuit (a) and characteristic voltage waveforms (b)

As a rule, the four-layer diodes are less powerful devices than the thyristors. They are mainly used as switching elements in pulse circuits, oscillator circuits, as replacements for unijunction transistors, as protection elements, etc.

Figure 3.62 shows the basic circuit of a pulse generator based on a four-layer diode. The principle of operation, static conditions, and limitations are identical to those of the corresponding generators based on unijunction transistors. Here an additional condition is valid that $V_{AA} > V_P$.

Diode AC switch (DIAC) is a bilateral (symmetric) diode thyristor. Its cross section and static characteristic are shown in Fig. 3.63. Practically, it consists of two four-layer diodes in anti-parallel connection. Namely, the regions P_1 and N_3 and P_2 and N_2 are short circuited. When $V_{AK} > 0$, the p-n junction J_3 is reverse biased, so the left-hand side of the component behaves like a four-layer diode having the short circuited p-n junction J_3 . At the breakdown of the junction J_2 the current through it initially bends, in parallel to junction J_3 , toward the cathode. Owing to this, at the junction P_2 a voltage drop arises which makes a forward bias for the junction J_3 . In this way, the region N_2 becomes active, leading to the initiation of the regenerative process and switching of the component to the state of conduction. The junction J_3 is reverse biased and has no influence.

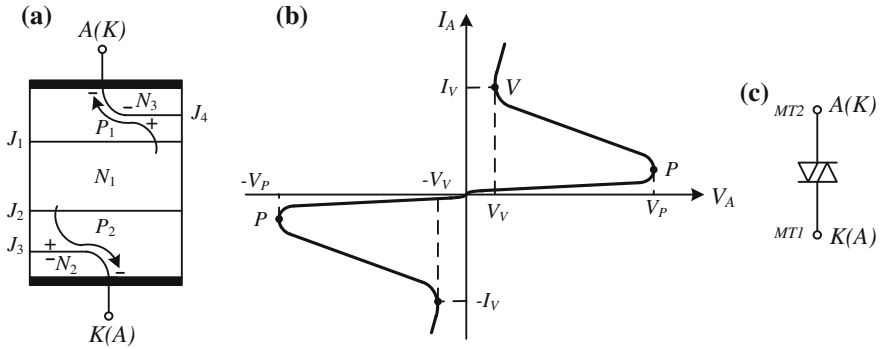


Fig. 3.63 Cross section (a) I-V characteristic (b), and symbol of DIAC (c)

If, however, $V_{AK} < 0$, the junction J_3 is reverse biased and J_4 is short circuited. Now the left hand side behaves like a four-layer diode. When the breakdown of the junction J_1 occurs, the current through this junction runs in parallel with the junction J_4 because it is not biased. This current makes a positive voltage drop across the region P_1 and provides a forward bias for the junction J_4 . Owing to this the region N_3 also becomes active.

If the breakdown voltages of the junctions J_1 and J_2 are equal, then the static characteristics in the I and III quadrants are completely symmetric (Fig. 3.63b).

Therefore, a DIAC can conduct in both directions, from anode to cathode and vice versa, depending upon polarity of the applied voltage. For this reason the external terminals are usually not called anode and cathode because this makes sense only with DC components. Their common name is the “main terminals” and they are denoted as MT1 and MT2. Sometimes they are simply denoted as A_1 and A_2 .

Like a four-layer diode, DIAC is a component of relatively low power. The breakpoint voltages are usually several tens of V. DIAC is used as a switching element in various pulse circuits, most frequently in the circuits based on TRIACs. It is off whenever the load current drops to the SIDAC holding current (Fig. 3.64b).

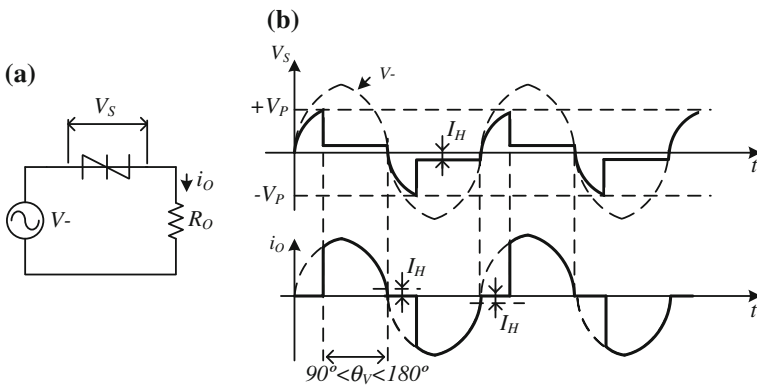


Fig. 3.64 SIDAC as a switch in an AC circuit (a) and voltage and current waveforms (b)

3.2.13 TRIAC

The TRIode AC switch (TRIAC) is a bilateral regenerative AC current switch with three terminals. Practically, this is a component consisting of two anti-parallel SCRs having a common gate. The difference from the triode SCR is that the TRIAC can conduct in both directions, from anode to cathode and vice versa. For this reason, similarly to DIAC, the terminals are called the main terminals and are denoted as MT1 and MT2 taking MT1 for the reference electrode.

The cross section of a TRIAC is shown in Fig. 3.65a. When MT2 is positive compared to MT1, the thyristor structure $P_1N_1P_2N_2$ is active. The region P_2 plays the role of gate. The junction P_1N_3 is reverse biased and the region N_3 is passive. If MT2 is negative compared to MT1, the four-layer structure $P_2N_1P_1N_3$ is active. The region N_2 , owing to the reverse bias, is now passive. The gate covers the regions P_2 and N so the four modes of TRIAC operation are possible, as shown in Table 3.2.

I quadrant—positive gate. The gate (region P_2) is forward biased and behaves like the gate of a standard thyristor. The region P_2 injects holes, the region N_2 injects electrons and this leads to turning on of the thyristor structure $P_1N_1P_2N_2$.

I quadrant—negative gate. The gate is negative compared to the electrode MT1. Because of that the region N of the gate is forward biased and injects electrons to the region P_2 . The gate current flows from P_2 towards N and makes a voltage drop in the region P_2 which acts as a forward bias for P_2N_2 part. This, also, leads to

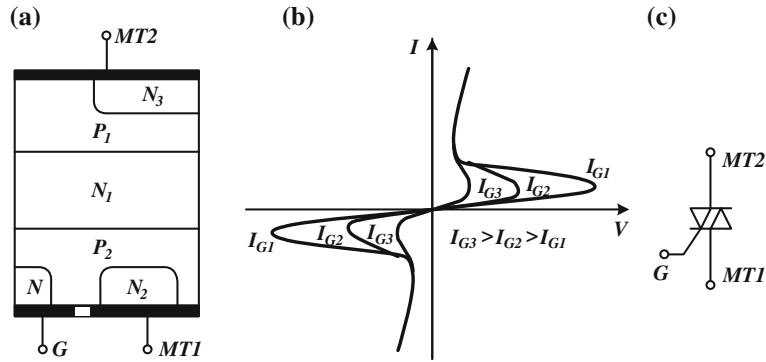


Fig. 3.65 Cross section (a), I-V characteristic (b), and symbol of TRIAC (c)

Table 3.2 Four modes of TRIAC operations

I quadrant MT1– MT2+	
II quadrant MT1+ MT2–	

turning on of the structure $P_1N_1P_2N_2$. Of course, this requires a higher gate current compared to the situation when the gate is positive.

III quadrant—negative gate. In this case terminal MT1 is positive compared to MT2 and the direction of the current of a conducting TRIAC is from MT1 toward MT2. The gate is negative compared to MT1, as a consequence the region $N-P_2$ is forward biased and the electrons from N are injected into the P_2 region. These electrons are “collected” by the P_2-N_1 junction that leads to triggering of the thyristor structure $P_2N_1P_1N_3$.

III quadrant—positive gate. Now the gate is positive compared to MT1. The active part of the gate is the region P_2 between N and N_2 . The junction P_2-N_2 is forward biased and it emits electrons “collected” by the P_2-N_1 junction. This, like in the previous case, leads to the turning on of the TRIAC. Upon turn-on, the region N does not participate in conduction since the current flows in the direction of the metallization. In both cases of the operation in the III quadrant the gate acts as a “remote” control electrode. Under these conditions turning on of the TRIAC requires the largest gate current (critical current) owing to the relatively poor collecting efficiency of the forward biased junction P_2N_1 . The lowest critical current is in the I quadrant at a positive bias of the gate. In general, the limits of the critical current and the triggering voltage of the TRIAC are similar to those of SCRs, except that a TRIAC can also be triggered by negative pulses.

It has already been emphasized that in SCRs, owing to the pile-up of minority carriers, problems may arise at turning off. This is more pronounced for TRIACs not only because they consist of thyristors but also because a considerably shorter time is available for the turn-off process. For AC voltage operation SCRs have available a sufficiently longer time. Indeed, after the current drops below I_H , the positive half-cycle ends and the negative half-cycle starts so SCRs have sufficient time to turn-off. A TRIAC, however, is able to conduct during the negative half-cycle so a very short time is available for it to turn-off. Practically this is the time during which the voltage changes its polarity, i.e., during zero crossing, when the current is below the minimum conduction current. If the change of voltage polarity is fast, the TRIAC may continue conducting in the opposite direction.

It is exactly because of this that the operating frequencies of TRIACs are limited to couple of hundreds Hz and at present are usually below 500 Hz.

Triggering of TRIACs. The triggering circuits are similar to those of SCRs with the exception that a TRIAC could also be triggered by negative pulses during positive or negative half-cycles of AC voltage. Consequently, for TRIAC triggering the bilateral switching elements are required.

The triggering circuit consisting of a resistance R_1 and a switch Pr (Fig. 3.66) uses a common power supply. R_1 serves for adjusting the level of the mains voltage at which the TRIAC is turned on if the switch is on.

The triggering circuit using a separate power supply (Fig. 3.67) is realized by using a CMOS buffer. The transistor Tr provides the necessary triggering current. If the total output current from the CMOS buffer is I_{DP} , then the gate current of the TRIAC is $I_g = (\beta + 1)I_{DP}$, where β is the current gain of the transistor Tr. This current has to be greater than the critical gate current, i.e., $I_{GT} < (\beta + 1)I_{DP}$. The

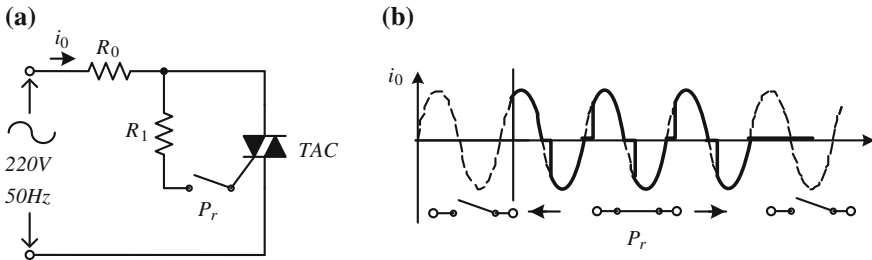


Fig. 3.66 Common supply TRIAC triggering circuit (a) and the waveform of the load current (b)

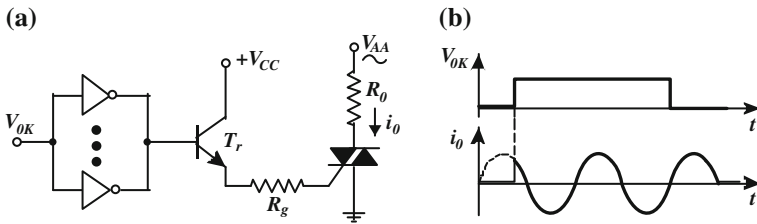


Fig. 3.67 CMOS triggering circuit (a), and waveforms of the excitation voltage and the output current (b)

resistance R_g ranges from several tens of Ω up to several hundreds of Ω . In any case, the condition $(\beta + 1)R_g > R_{DP}$ has to be fulfilled, where R_{DP} is the total output resistance of the CMOS buffer when the output is high (PMOS transistor is on). In the absence of a triggering pulse the TRIAC is off and the load current is $i_0 = 0$ (Fig. 3.67b). If the TRIAC stays on after the triggering pulse ends, it remains on until the anode voltage changed its polarity. Throughout the action of the triggering pulse the TRIAC is on. This method of control is often called the TPC-control (Time Proportional Control). It is therefore based on the principle of the ratio of the time the TRIAC is on to the time the TRIAC is off. It is customary to synchronize the turn-on instant with the zero crossing of the AC voltage. The shortcomings of the phase method (the control of the conduction angle of each half-cycle) compared to the TPC method are the low power factor owing to the nonsinusoidal waveform of the load current and the presence of noise in the mains network due to abrupt current changes when the TRIAC or the thyristor is turned on.

A typical TRIAC triggering circuit for the phase control of the load current (Fig. 3.68) uses a two-directional regenerative switch (DIAC, SBS, SIDAC) in the gate circuit. In this way the angle of conduction control is accomplished in both the positive and the negative half-cycles.

The TRIAC is, namely, triggered by each turn-on of the bilateral switch. Time constant R_C , and consequently the angle of TRIAC conduction, is varied by potentiometer R_1 . When the voltage across the capacitor C reaches the value of the break point voltage V_P during the positive half-cycle, or $-V_P$ during the negative

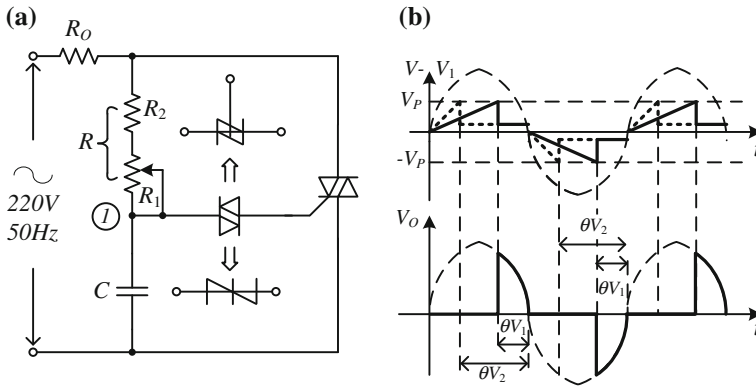


Fig. 3.68 Triggering circuit of a bilateral regenerative switch (a) and voltage waveforms at the input V_P , load V_O , and capacitor V_1 (b)

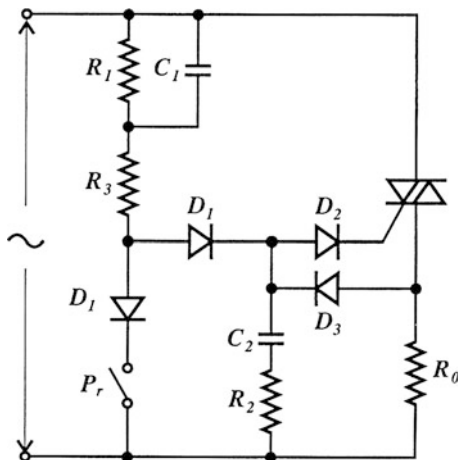
one, the two-directional switch will be turned on. This causes triggering of the TRIAC and discharge of the capacitor C . Then, $V_1 = V_H + V_{GK} = 1.5\text{--}2\text{ V}$ until the current of the two-directional switch drops below the holding current I_H . This occurs immediately before the zero crossing of the mains voltage. The corresponding voltage waveforms are shown in Fig. 3.68b, with the linearized voltage V_1 across C . The dotted lines show the variations of the voltages V_1 and V_O across the load R_O for a smaller value of R . In such a situation the TRIAC is turned on earlier so its angle of conduction is greater ($\theta_{v2} > \theta_{v1}$).

The typical values of the timing elements are several μF to several hundreds of μF for the capacitance C and several $\text{k}\Omega$ to several hundreds of $\text{k}\Omega$ for the resistance R . The breakpoint voltages of the two-directional switches are from 10 V to several hundreds of V, depending upon the type of the switch. The choice of the TRIAC depends upon the load current, i.e., the load resistance R_O and the maximum AC voltage. The break point voltage of the TRIAC at the open gate ($I_G = 0$) should be greater than the maximum operating voltage. The load resistances usually range from several Ω to hundred Ω .

Triggering by zero crossing. It has already been emphasized that triggering of a TRIAC during a half-cycle would cause abrupt current changes and the appearance of noise. The noise can be removed by filtering. However, at high powers these filters can become very bulky and expensive. Because of that, noise is removed by elimination of its causes. This is done by designing a triggering circuit to turn-on the TRIAC during zero crossing of the AC voltage.

One of the possibilities to implement the zero-crossing triggering of the TRIAC is shown in Fig. 3.69. Owing to the RC network the gate voltage precedes the voltage between the main electrodes, creating in this way the conditions for triggering at very small voltages and allowing the switch Pr to open. The triggering of the TRIAC will

Fig. 3.69 Zero crossing triggering of the TRIAC



occur at a very small positive voltage through the capacitor C_1 , the resistor R_3 , and the diodes D_1 and D_2 . Owing to this charging of the capacitor C_2 through the diode D_3 will proceed as long as the input voltage is increasing. After that, while the input voltage decreases, the diode D_3 will be off and the capacitor C_2 will discharge through the diode D_2 which is turned on. In this way C_2 provides the gate current which will keep TRIAC in the state of conduction during the negative half-cycle even if meanwhile the switch P_r is turned on. Thus, in the circuit from Fig. 3.69 the TRIAC is always conducting an integer number of cycles. Also, it should be emphasized that during the negative input voltage the turn-on cannot occur. In other words, both turning on and turning off occur at the positive zero crossing.

The integrated circuits used as the triggering circuits at zero crossing are available today. Their application simplifies considerably the control circuits of the thyristor circuits (SCRs and TRIACs).

Problems

- 3.1 Determine the resistance R_B in the circuit from Fig. 3.36b to ensure turning off of the thyristor. The voltage on the thyristor in the on state can be neglected. The circuit in Fig. 3.36b has $V_{AA} = 100$ V, $R_0 = 50$ Ω , $V_{BB} = 15$ V (high level of control voltage on the base of the transistor T_r) and $\beta = 50$.
- 3.2 If the latching time (minimal duration of trigger pulse) is $t_L = 8$ μ s, determine the anode current I_L (thyristor current at the moment T_L) in the circuit shown in Fig. 3.70.
- 3.3 For the circuit in Fig. 3.71 determine the angle when the thyristor starts to conduct, so that the average value of a current through the load is 1 A. The voltage drop on the diodes in the on state is 0.7 V, and the diode resistance can be neglected.

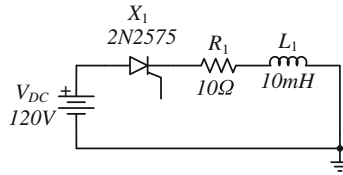


Fig. 3.70 Simple circuit with the thyristor as a switch

Fig. 3.71 Bridge rectifier with the thyristor in a load branch

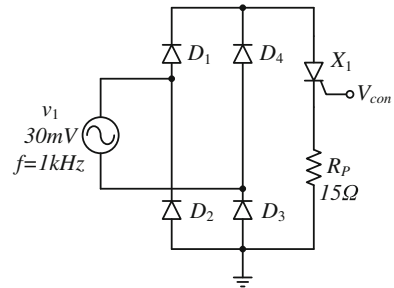
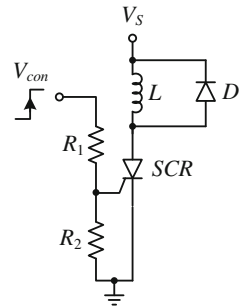


Fig. 3.72 Turning on the thyristor in circuit with the inductive load



- 3.4 Determine the resistance of the resistors in the circuit shown in Fig. 3.72 to provide a reliable turn-on of the thyristor. For the circuit from Fig. 3.72 it is known that $V_{con} = 5 \text{ V}$, $V_{Gmin} = 3 \text{ V}$ and $I_{Gmin} = 20 \text{ mA}$.
- 3.5 The characteristics of a forward biased thyristor are shown in Fig. 3.27. Determine power losses on the thyristor for the thyristor current shown in Fig. 3.73.
- 3.6 For the circuit shown in Fig. 3.74 determine the interval of time t_1 after which the current will fall to 0. The thyristor is turned on in the moment $t = 0$. The diode and the thyristor can be considered ideal. It is known that $i_C(0) = 0$,

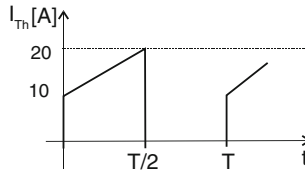
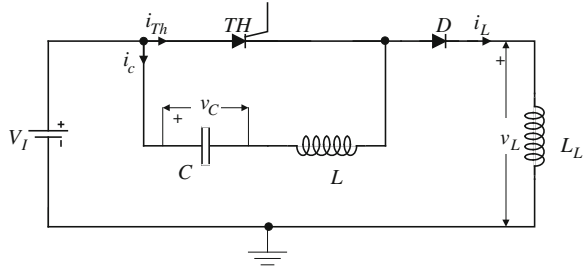


Fig. 3.73 The waveform of the thyristor current

Fig. 3.74 One part of resonant circuit with the thyristor as a switch



$v_C(0) = V_I$ and $i_L = 5$ A (current through L_L can be taken as constant). The circuit in Fig. 3.74 has: $V_I = 100$ V, $I_L = 5$ A, $C = 1$ μ F and $\omega_0 = \frac{1}{\sqrt{LC}} = 10^5$ rad/s.

- 3.7 To control the power on a load with a resistance of $100\ \Omega$ the circuit shown in Fig. 3.68 is used. The breakdown voltages of the diac are ± 25 V, while the voltages on the diac and the triac in the on state can be neglected. The circuit is connected to the power network 220 V, 50 Hz. The circuit in Fig. 3.68 has $R = 50$ k Ω and $C = 0.1$ μ F.

- Determine the angle when the triac starts to lead.
- Draw the waveform of the load voltage.

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Chapter 4

PWM DC/DC Converters

In principle, the pulse DC/DC converters consist of two parts, a basic circuit and a regulating assembly. The basic circuit comprises of switches (usually a transistor and a diode), a choke and/or a transformer, and a capacitor. By turning on and off the switches in a controlled manner, the required amount of energy is transferred through the switches and the low frequency filter (the choke and the capacitor) from the input to the load. In this way, the output voltage is proportional to the ratio of the on and off time intervals of the switch. This ratio, thus the output voltage, is controlled by the control block (CB).

Depending on the configuration of the elements in the basic circuit, there are several different DC/DC converters. Globally, however, they could be classified as converters without galvanic isolation and those with galvanic isolation (the input and the output are separated by a transformer or an optocoupler). The classification of these two groups could be made as shown in Fig. 4.1. On the other hand, all these devices can be split into four groups: forward (direct), flyback (indirect), push–pull (symmetric), and Ćuk converters. The peculiarity of Ćuk converters is that in addition to the electromagnetic energy transfer (similar to other converters) they also use electrostatic energy transfer. This type of converter also comprises coupled input–output coils which serve to eliminate the variations of the input and output currents, the property significant from the point of view of elimination of pulse disturbances.

The classification according to the mode of control, or regulation, of the output voltage is shown in Fig. 4.2. The self-oscillating converters are simple from the design point of view, but their efficiency factor η is the lowest. They are mainly used for supplying small loads (up to several tens of watts). The widest application today finds DC/DC converters using pulse width modulation (PWM). The output voltage is controlled by varying the ratio of the on and off times of the switch with a constant frequency of switching.

Over the past 10 years an ever increasing attention has been paid to the resonant converters. It is considered that the future in the design of efficient power supplies belongs to this type of converter. The essential difference of resonant power converters compared to other converter types is that the state of the switch is changed at the zero crossing of the current or voltage. Owing to this the dissipation of the switching elements is very low and the efficiency factor of the resonant converters

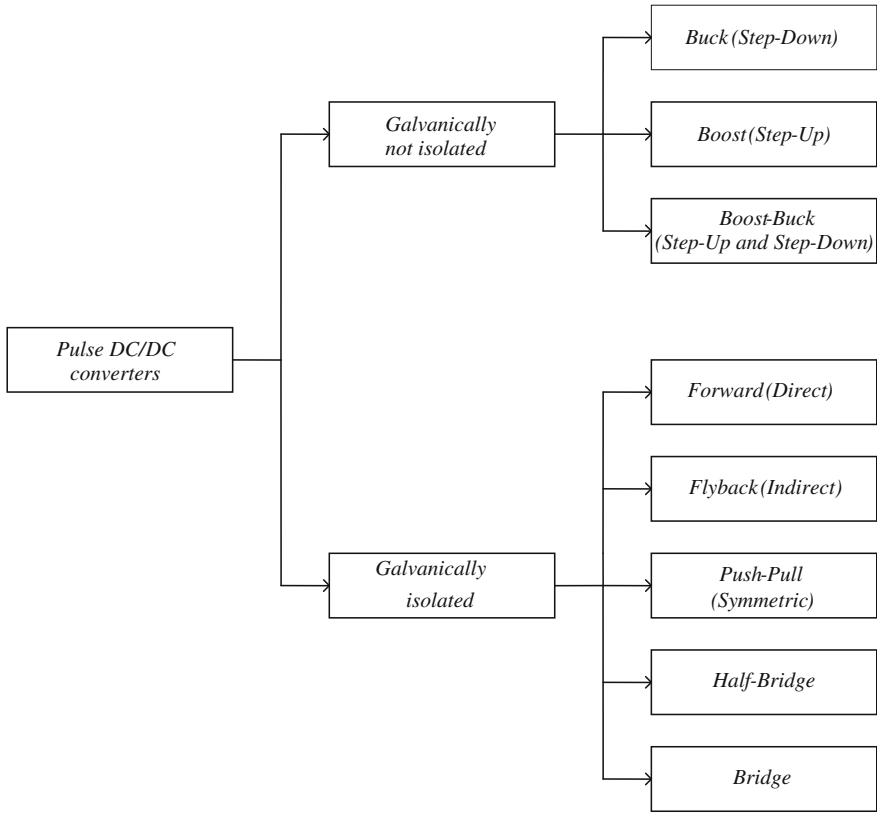


Fig. 4.1 Classification of pulse DC/DC converters according to the topology of the basic circuit

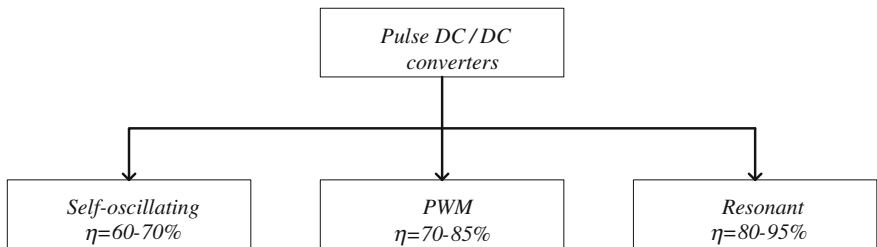


Fig. 4.2 Classification according to the mode of control

may be in excess of 90 %. This allows the switching elements to operate up to the frequencies of several MHz, whereas the maximum switching frequency of PWM converters is within the limits of 100–200 kHz. For this reason, the specific power density is more than one order of magnitude higher compared to that of the PWM converters and amounts to several thousands W/dm³. This opens new possibilities

in designing compact power supplies which can, together with the standard ICs, constitute a part of the layout of a printed circuit board. If the period from 1970 up to the late 1980s can be qualified as the period of PWM converters, it is certain that 1990s were the period of resonant converters.

In the resonant converter, energy is redistributed within a resonant circuit consisting of a coil and a capacitor. In this process, the energy is proportional to the square of the current through the coil and to the square of the voltage across the capacitor. The output voltage depends on the operating frequency. It is at the highest when the operating and the resonant frequency are equal.

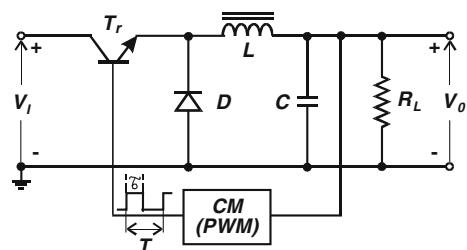
A separate group of pulse DC/DC converters consists of coil-less converters. As the name indicates, they do not make use either of coils or of transformers. The only accumulating element is the capacitor. The basic circuit is made of a switched-capacitor network. These networks are suitable for the hybrid form of design, and sometimes for monolithic integrated circuit. Until recently these converters, as a rule, have been auxiliary power supplies with low output currents (several tens of milliamperes). Over the past several years, they have been given increased attention and are envisaged to be in the mainstream for designing supplies of portable and pocket equipment of low consumption and containing one battery as the primary power source [1]. This is the reason that they have been classified as a separate group even though their basic application does not belong to power electronics but to supplying electronic equipment of low consumption (pocket calculators, mobile phones, etc.).

4.1 Forward Converters

The simplest version of a DC/DC converter is the forward converter without galvanic input–output separation (Fig. 4.3). Owing to the type of connection between the transistor T_r , the choke L , and the load, this circuit is often called the series converter. The term “forward” indicates that the energy from the source is directly forwarded to the load. With the transistor conducting, the energy of the source is simultaneously transferred to the load and accumulated by the choke.

The diode D is then off. When the transistor is off, the circuit is closed through the turned-on diode and the energy accumulated by the choke is transferred to the load. The output voltage depends on the ratio of the intervals when the transistor is on or off

Fig. 4.3 Basic circuit of forward converter



and is lower than the input voltage. Because of such ratio of the input and the output voltages ($V_o < V_I$), this type of converter is often called the step-down converter.

Depending on the value of the control signal the transistor and the diode are alternately on and off. At the input of the LC filter, if the turn-on and turn-off times of the transistor and diode are neglected, a rectangular voltage with pulses of variable duration is established. The amplitude of these pulses is approximately equal to the input voltage. The diode D ensures the current flow when the transistor T_r is off. The role of the choke L is to pass to the output only the DC component which is equal to the mean value of the voltage at the input of the filter during one cycle of the control signal

$$V_{av} = \frac{1}{T} \int_0^{\tau} V_I dt \approx V_I \frac{\tau}{T} = DV_I, \quad (4.1)$$

where τ is the duration and T is the cycle, while $D = \tau/T$ is the duty cycle of the control signal. The capacitor C corrects the AC components across the load, R_L .

According to (4.1), it would appear that the variation of the output voltage is proportional to the variation of the nonstabilized input voltage. However, the output voltage, or a fraction of it, is fed to the control module. This module generates square signals for turning on and off of the controlling transistor. The variation of the output voltage of the converter modulates the duration of the pulses τ at the output of the control module. This closed system of automatic control, through the action of the control module, maintains the output voltage constant irrespective of the variations of the input voltage or of the load current.

4.1.1 Analysis of the Basic Circuit

In this section, some basic relations between the parameters characterizing the operation of the converter are derived. For the purpose of this analysis several justifiable assumptions have been made.

In the first part, it will be assumed that the transistor and the diode are ideal switches (instantaneous switch-on and switch-off, the on-resistance negligible, the off resistance infinite), and that the output voltage V_o and the current I_o are constant. When the transistor T_r is on, the diode is off (Fig. 4.4). The current through the choke increases from the minimum value I_{Lm} (at the switch-on) to the maximum value I_{LM} (at the switch-off of the transistor). If V_I and V_o are constant, the variation of the choke current is governed by the following differential equation

$$V_I = L \frac{di_L}{dt} + r_L i_L + V_o, \quad (4.2)$$

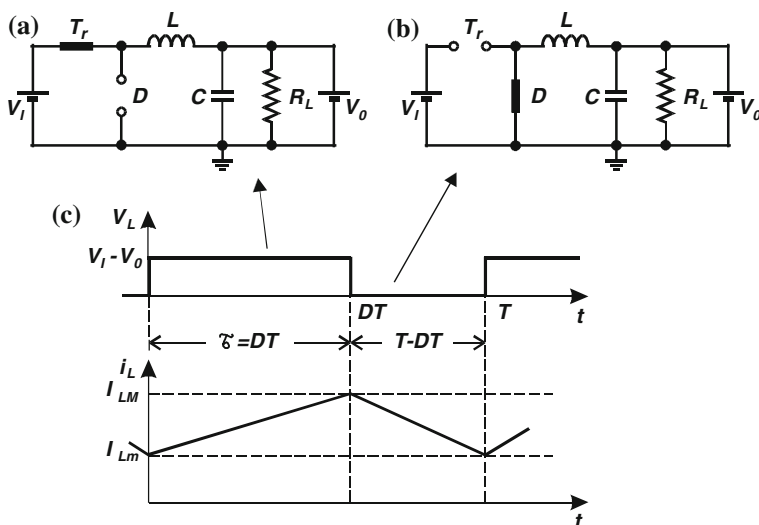


Fig. 4.4 Equivalent circuits of forward converter during intervals $0 < t < DT$ (a) and $DT < t < T - DT$ (b), and the corresponding variations of the voltage and current of the choke (c)

where r_L is the active resistance of the choke. The solution of (4.2) can be expressed as:

$$i_L(t) = \frac{V_I - V_o}{r_L} \left(1 - e^{-t/\tau_L} \right) + I_{Lm} e^{-t/\tau_L}, \quad (4.3)$$

where $\tau_L = L/r_L$. It has been shown that the coefficient of efficiency would be maximal if $T/\tau_L < 0.05$, because the active resistance of the choke can then be neglected. In the design of the choke, therefore, care should be taken to ensure r_L as small as possible. In such a case, by expanding the exponential terms in (4.3) in Maclaurin series and after justifiable approximations, it turns out that

$$i_L(t) = I_{Lm} + \frac{V_I - V_o}{L} t. \quad (4.4)$$

The maximum value of the choke current is at $t = \tau$, so

$$I_{LM} = I_{Lm} + \frac{V_I - V_o}{L} \tau. \quad (4.5)$$

During $\tau < t < T - \tau$, the voltage of the control pulse is zero, so the transistor T_r is off and the diode D is on (Fig. 4.4). Then the current through the choke is

$$i_L(t) = I_{LM} - \frac{V_o}{L}t, \quad (4.6)$$

and its minimum value is

$$I_{Lm} = I_{LM} - \frac{V_o}{L}(T - \tau). \quad (4.7)$$

From (4.4) and (4.6), it can be seen that the current $i_L(t)$ is a linear function of time. The load current is equal to the average value of the current through the choke, i.e.,

$$I_O = \frac{I_{Lm} + I_{LM}}{2}. \quad (4.8)$$

The variation of the current through the choke is equal to the difference between the maximum and the minimum values, i.e.,

$$\Delta i_L = \frac{V_I}{L}TD(1 - D) \quad (4.9)$$

where $D = \tau/T$ is the duty cycle of the control pulse. Obviously, the variation of i_L when the transistor is on is equal to the variations of i_L when the transistor is off, i.e.,

$$\frac{V_I - V_o}{L}\tau = \frac{V_o}{L}(T - \tau), \quad (4.10)$$

therefore, it follows that

$$V_o = \frac{\tau V_I}{T} = DV_I. \quad (4.11)$$

4.1.1.1 Output Voltage Variation

The variation of the output voltage can be determined, if the variation of the current through the filter capacitor is known

$$i_C = i_L - I_O. \quad (4.12)$$

Fig. 4.5 Voltage and current waveforms, control signal (a), current i_L (b), current i_C (c), capacitive component of voltage v_C (d), resistive component of voltage v_C (e) and output voltage (f)

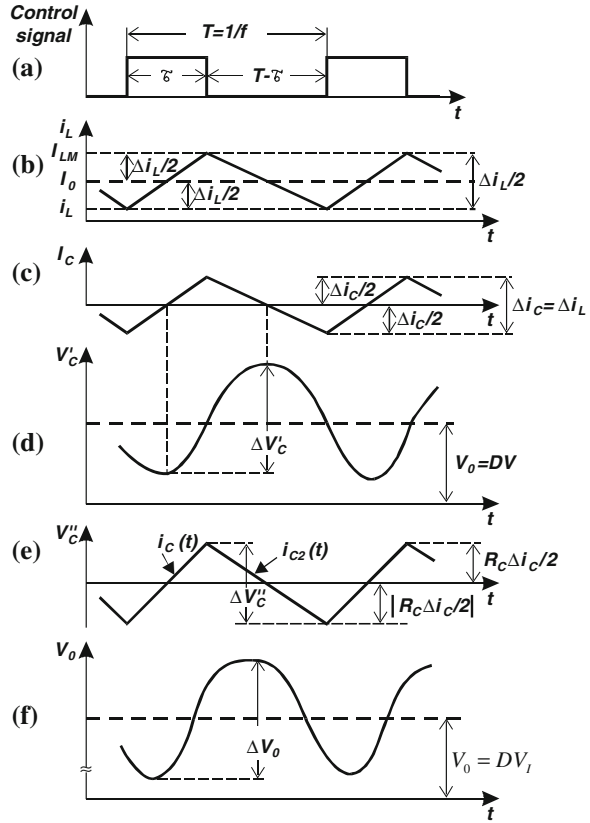


Figure 4.5 shows the variations of the currents i_L and i_C and the variations of the output voltage (voltage across the capacitance). The average value of the current through the capacitor is zero, whereas its variation is equal to the variation of the current through the choke, i.e., $\Delta i_C = \Delta i_L$. While $i_L > I_o$, the capacitor is being charged and the output voltage increases, whereas for $i_L < I_o$, the capacitor is being discharged and the output voltage decreases. The variation of the output voltage has two components, the capacitive $\Delta v_C'$ (Fig. 4.5d) and the resistive $\Delta v_C''$ (Fig. 4.5e), caused by the equivalent series resistance of the capacitor. The AC components are, for clarity, drawn out of proportion. The resistive component, which is in phase with the current i_C , can become dominant at high frequencies if the choice of the capacitor is wrong.

This may have particularly undesirable consequences in the relay converters where due to this voltage component a considerable shift in the nominal frequency of the controlling transistor may occur. For this reason in the design process, in addition to the selection of a capacitor having a low series resistance, it is often required that its capacitance is considerably higher than the optimum value

according to other criteria (small weight or small volume). The variation of the output voltage is equal to the sum of the capacitive and the resistive component of the voltage across the capacitor, i.e.,

$$v_o(t) = \frac{1}{C} \int_0^t i_C dt + R_C i_C. \quad (4.13)$$

When the transistor is on, taking into account (4.12), it follows that

$$i_C(t) = \frac{V_1 - V_o}{L} t - \frac{\Delta I}{2}, \quad (4.14)$$

where $\Delta I = \Delta i_L$, so

$$v_o(t) = \frac{V_1 - V_o}{2LC} t^2 + \left(R_C \frac{V_1 - V_o}{L} - \frac{\Delta I}{2C} \right) t - \frac{\Delta I}{2} R_C. \quad (4.15)$$

When the transistor is off, the currents through the choke L and the capacitor C decrease

$$i_C(t) = \frac{\Delta I}{2} - \frac{V_o}{L} t,$$

and the variation of the output voltage is

$$v_o(t) = -\frac{V_o}{2LC} t^2 + \left(\frac{\Delta I}{2C} - R_C \frac{V_o}{L} \right) t + \frac{\Delta I}{2} R_C. \quad (4.16)$$

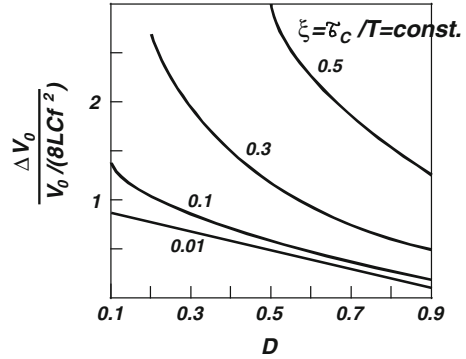
By differentiating (4.15) and (4.16) over time and equating them to zero, one obtains that the output voltage is maximum and minimum at the following respective instants

$$t_1 = \frac{\tau}{2} - \tau_C \quad \text{and} \quad t_2 = \frac{T - \tau}{2} - \tau_C,$$

where $\tau_C = CR_C$. The maximum and the minimum are shifted to the left by τ_C compared to the case when the value of R_L can be neglected. The maximum variation of the output voltage (peak-to-peak) is equal to the difference between its maximum and minimum values

$$\Delta v_o = \frac{V_o(1 - D)}{8LCf^2} + \frac{V_o}{2LCf^2 D} \left(\frac{\tau_C}{T} \right), \quad (4.17)$$

Fig. 4.6 Normalized variation of output voltage as function of D and ξ



where the first member is the capacitive component $\Delta v_c'$ and the second is the resistive component $\Delta v_c''$. If the notation $\xi = \tau_c/T$ is introduced, then

$$\Delta v_o = \frac{V_o(1-D)}{8LCf^2} \left[1 + \frac{4\xi^2}{D(1-D)} \right]. \quad (4.18)$$

From Fig. 4.6, it is obvious that for $\tau_c > 0.3T$, the dominant influence on the variation of the output voltage is due to the resistive component. In the course of selecting the value of the capacitor and the frequency of operation of the controlling transistor, the care should be taken that

$$\tau_c < 0.1T. \quad (4.19)$$

From (4.18) it is possible to determine the value of the product LC , which would result in the variation of the output voltage smaller than the permitted maximum

$$LC > \frac{V_o(1-D)}{\Delta V_o f^2} \left(1 + \frac{4\xi^2}{1-D} \right). \quad (4.20)$$

The right-hand side of (4.20) is at the maximum when $D = D_{\min}$. Therefore, it is required that

$$LC > \frac{V_o(1-D)}{\Delta V_o f^2} \left(1 + \frac{4\xi^2}{D_{\min}(1-D_{\min})} \right). \quad (4.21)$$

4.1.1.2 Quasi-static Mode of Transistor

The maximum collector-emitter voltage of the transistor in the quasi-stable state is equal to the input voltage, i.e., $V_{CE\max} = V_I$. While T_r is off the collector current is zero and when it is on, its current is equal to the current through the choke

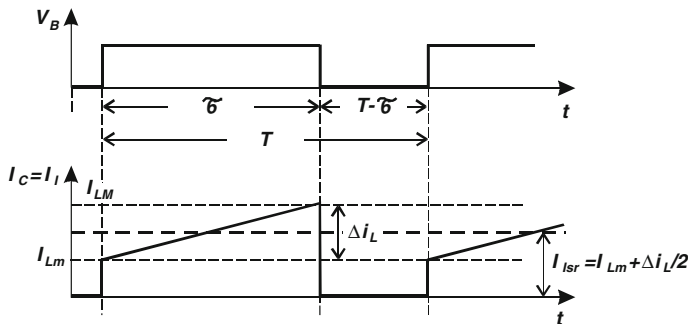


Fig. 4.7 Control voltage and collector current of transistor

(Fig. 4.7). Therefore, the maximum collector current is equal to the maximum current through the choke and is determined by (4.5), whereas its average value is

$$I_{Cs} = I_{Isr} = I_{Lm} + \Delta i_L/2, \quad (4.22)$$

where I_{Lm} and Δi_L are determined by (4.7) and (4.9), respectively.

From (4.23) it follows that,

The input converter current and the collector current are equal. Since the circuit is assumed ideal, there are no losses in the converter, so the average value of the input power is equal to the output power, i.e.,

$$V_I I_{Isr} = V_O I_O. \quad (4.23)$$

$$I_{Iav}/I_O = V_O/V_I = 1/D. \quad (4.24)$$

This indicates that an ideal converter behaves like a transformer whose transformation ratio is equal to the reciprocal value of the duty cycle of the control pulses.

From Fig. 4.7, it can be seen that the forward DC/DC converter behaves like a typical pulse load of the primary source involving high rates of current changes, di/dt . This generates noise which is transferred through the primary source to other parts of the equipment. It is for this reason that the corresponding filters are often inserted between the primary source and the input of the DC/DC converter.

Condition of Continuity of the Current Through the Choke

The above analysis applies under the condition that the current through the choke is continuous. This condition will be met if

$$I_O > \frac{\Delta i_L}{2}, \quad (4.25)$$

or

$$I_O > \frac{V_o}{2L} T(1 - D). \quad (4.26)$$

From (4.26) it follows that the minimum inductance of the first choke of the output filter which still results in a linear current through the choke is

$$L_{\min} = \frac{V_o T(1 - D)}{I_O 2}. \quad (4.27)$$

In order that the current through the choke be continuous for any value of the supply voltage (4.27) should be calculated taking into account the minimum duty cycle (the maximum value of the input voltage and the minimum value of the output voltage).

Example 4.1 Design a forward converter (Fig. 4.3) if $V_I = 48 \text{ V}$, $V_o = 18 \text{ V}$, $R_L = 10 \Omega$, and the variation of the output voltage is less than 0.5 %. The converter should operate in the continuous mode.

On the basis of (4.11), the duty cycle of the control pulses is

$$D = V_o/V_I = 18 \text{ V}/48 \text{ V} = 0.375.$$

The minimum inductance for the continuous operating mode is determined by (4.27). If it is assumed that the frequency of the control pulses is 40 kHz, it follows

$$L_{\min} = \frac{V_o}{2I_o f} (1 - D) = \frac{R_L(1 - D)}{2f} = \frac{10 \times (1 - 0.375)}{2 \times 40 \times 10^6 \text{ Hz}} = 78 \mu\text{H}.$$

Allowing the inductance to be 25 % higher than the minimum inductance, i.e.,

$$L = 1.25L_{\min} = 97.5 \mu\text{H}.$$

The current variation through the choke is

$$\Delta i_L = \frac{V_I}{L f} (1 - D) D = \frac{48 \times (1 - 0.375) \times 0.375}{(97.5 \times 10^{-6})(40 \times 10^3)} = 2.88 \text{ A}.$$

The average value of the current through the choke is equal to the load current, i.e.,

$$I_L = I_O = V_o/R_L = 18 \text{ V}/10 \Omega = 1.8 \text{ A}.$$

The maximum and minimum choke currents are, respectively,

$$\begin{aligned} I_{Lm,M} &= I_O + \Delta i_L/2 = 1.8 \text{ A} + 2.88 \text{ A}/2 = 1.8 \text{ A} + 1.44 = 3.2 \text{ A}, \\ I_{Lm,m} &= I_O - \Delta i_L/2 = 1.8 \text{ A} - 2.88 \text{ A}/2 = 1.8 \text{ A} - 1.44 = 0.36 \text{ A}. \end{aligned}$$

By neglecting the ESR of the capacitor in (4.17), it follows

$$C > \frac{1-D}{8Lf^2(\Delta V_0/V_0)} = \frac{1-0.375}{8(97.5 \times 10^{-6})(40 \times 10^3) \times 0.005} = 100 \mu\text{F}.$$

4.1.1.3 Discontinuous Mode

Depending on the fact whether the current through the choke is continuous or discontinuous within a single cycle, one can distinguish two modes of operation of the converter:

- continuous when the current of the choke is continuous, and
- discontinuous when the current of the choke is zero over a part of the cycle T .

The boundary between these two modes is reached when the minimum current of the choke $I_{Lm} = 0$. Whether a converter having specified parameters of the circuit elements will operate in the continuous or the discontinuous mode will be dependent on the load resistance. The limiting value of the load current I_{ol} is obtained when the inequality sign $>$ in (4.25) and (4.26) is replaced by the equality sign, so that

$$I_{ol} = \frac{V_o}{2L} T(1-D) = \frac{V_1 T}{2L} D(1-D). \quad (4.28)$$

Since $I_{ol} = V_o/R_{Ll}$, having in mind (4.28), the load resistance for which the converter is at the boundary between the continuous and the discontinuous mode is determined by

$$R_{Lg} = \frac{2L}{T(1-D)}. \quad (4.29)$$

The limiting load current I_{ol} is a quadratic function of the duty cycle (Fig. 4.8). Its maximum, taking into account (4.28), is at $D = 0.5$

$$I_{ol \max} = \frac{V_1 T}{8L}. \quad (4.30)$$

If the load resistance is increased above the value specified by (4.29), the converter crosses to the discontinuous operating mode (Fig. 4.8b). During the cycle $D_2 T$ the choke current is equal to zero, thus the voltage across the choke is also zero.

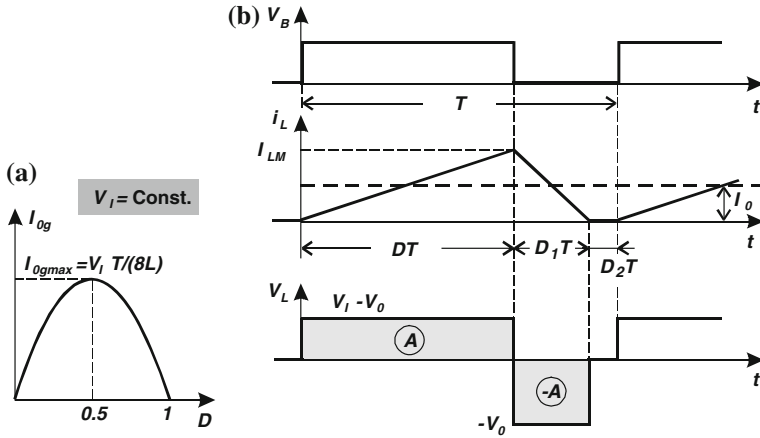


Fig. 4.8 Load current at the boundary between the continuous and discontinuous operating modes (a) and the current and voltage of the choke in the discontinuous mode (b)

The load current during this interval is provided by the capacitor only. Since the average value of the voltage across the choke is zero, the surfaces above and under the time axis are equal, i.e.,

$$(V_I - V_o)DT = V_o D_1 T, \quad (4.31)$$

therefore, it follows that

$$\frac{V_o}{V_I} = \frac{D}{D + D_1}, \quad (4.32)$$

where $D + D_1 < 1$. The maximum current of the choke is equal to its variation Δi_L , so that

$$I_{LM} = \frac{V_o}{L} (D_1 T). \quad (4.33)$$

The output current is equal to the average current through the choke, i.e.,

$$I_o = \frac{I_{LM} + 0}{2} \frac{(D + D_1)T}{T} = \frac{I_{LM}}{2} (D + D_1) \quad (4.34)$$

By combining (4.34) with (4.33), (4.32), and (4.30) it follows that

$$I_o = \frac{V_I T}{2L} D D_1 = 4I_{olmax} D D_1, \quad (4.35)$$

or

$$D_1 = \frac{I_o}{4I_{olmax}D}. \quad (4.36)$$

By introducing (4.36) into (4.32) it turns out that in the discontinuous mode

$$\frac{V_o}{V_I} = \frac{D^2}{D^2 + I_o/(4I_{olmax})} \quad (4.37)$$

If the input voltage is constant, then V_o will decrease with the increase of the load current I_o (Fig. 4.9) up to the boundary between the continuous and the discontinuous mode. Above this boundary ($I_o > I_{ol}$), the output voltage does not depend on the load current. The boundary between the continuous and the discontinuous mode as a function of the duty cycle D is a parabola (dotted lines in Fig. 4.9) having its maximum at $D = 0.5$ (Eq. 4.28). Therefore, if the load is variable, the converter may cross from one operating mode to the other. If the transition to the discontinuous mode is not permissible, a fixed load R_p should be connected in parallel with the load which will ensure at $R_L = R_{OLmax}$ that $I_o > I_{ol}$.

For the worst case when $D = 0.5$, it should be ensured that

$$V_o/(R_p || R_{Lmax}) > I_{olmax} = V_I T / (8L). \quad (4.38)$$

In the limiting case, when it is required that the converter operates in the continuous mode, if the load is not connected ($R_{Lmax} \rightarrow \infty$), the fixed load is

$$R_p \leq V_o / I_{olmax}. \quad (4.39)$$

The presence of R_p lowers the factor of efficiency because the power $V_o(V_o/R_p)$ is a net loss.

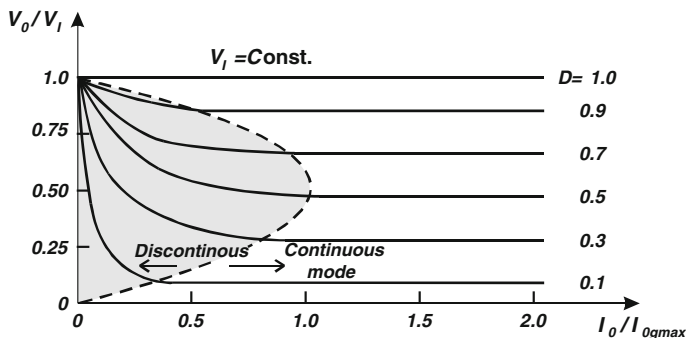


Fig. 4.9 Normalized output characteristics of a forward converter versus duty cycle of control pulses

Example 4.2 For a forward converter specified by $V_I = 24$ V, $L = 200$ μ H, $C = 1,000$ μ F, $f = 1/T = 10$ kHz, $D = 0.4$, and $R_L = 20$ Ω :

- check the operating mode and determine the output voltage,
 - determine the duty cycle of the control pulses for which the converter operates at the boundary between the continuous and the discontinuous mode,
 - determine the value of the fixed resistance (“idle resistance”) so that the loaded converter operates in the continuous mode.
- (a) The operating mode is checked on the basis of the variations of the current through the choke. At first it will be assumed that the current through the choke is continuous. Then, the average value of this current is equal to the load current, i.e.,

$$I_L = I_O = V_O/R_L = DV_I/R_L = 0.4 \times 24/20 = 0.48 \text{ A}.$$

On the basis of (4.9) it follows that

$$\Delta i_L = \frac{V_I}{L_f} D(1 - D) = \frac{24 \times 0.4(1 - 0.4)}{(200 \times 10^{-6})(10 \times 10^3)} = 2.88 \text{ A}$$

Since $\Delta i_L/2 = 2.88/2 = 1.44 > I_O = 0.48$ A, the continuity condition (4.25) is not met. Therefore, the current through the choke is discontinuous and the converter operates in the discontinuous mode when the transfer characteristic is determined by (4.37), so that

$$\frac{V_o}{V_I} = \frac{D^2}{D^2 + (V_o/R_L)/(4I_{\text{ogmax}})},$$

where, on the basis of (4.30), $I_{\text{olmax}} = (V_I T)/(8L) = 24/(8 \times 200 \times 10^{-6} \times 10 \times 10^3) = 1.5$ A. Therefore,

$$\frac{V_o}{24} = \frac{0.4^2}{0.4^2 + (V_o/20)/(4 \times 1.5)} = \frac{0.16}{0.16 + V_o/20},$$

thus it follows that

$$V_o^2 + 19.2V_o - 460.8 = 0,$$

or $V_o = 13.9$ V.

The waveforms of the voltage and current of the choke are shown in Fig. 4.10a.

- (b) At the boundary between the continuous and the discontinuous mode $\Delta i_L / 2 = I_O = V_O / R_L$, so according to condition (4.9), the limiting duty cycle is

$$D_g = 1 - \frac{2Lf}{R_L} = 1 - \frac{2 \times (200 \times 10^{-6}) \times (10 \times 10^3)}{20} = 0.8.$$

The output voltage is $V_O = D_1 V_1 = 0.8 \times 24 = 19.2$ V. The waveforms of the voltage and the current of the choke are shown in Fig. 4.10b.

- (c) On the basis of (4.28) it follows that the output current at the boundary between the continuous and the discontinuous mode is

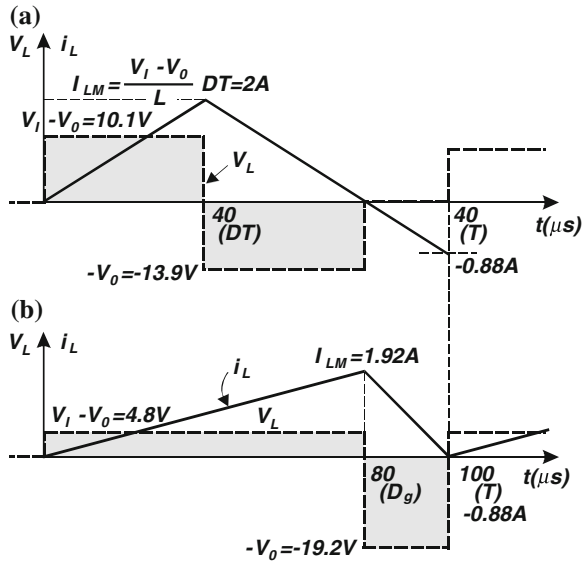
$$I_{og} = \frac{V_1 T}{2L} D(1-D) \frac{24 \times 0.4 \times (1-0.4)}{2 \times (200 \times 10^{-6}) \times (10 \times 10^3)} = 1.44 \text{ A}$$

Taking into account (4.9), the limiting value of the load is

$$R_{Lg} = \frac{2L}{T(1-D)} = \frac{2 \times (200 \times 10^{-6}) \times (10 \times 10^3)}{1-0.4} = \frac{2}{3} = \frac{R_P \cdot R_L}{R_P + R_L},$$

and the “idle resistance” is $R_P = 10 \Omega$.

Fig. 4.10 The waveforms of the voltage and the current of the choke in discontinuous (a) and continuous (b) operating mode



4.1.1.4 Energy Relations in Quasi-stable States

The following considerations are related to power losses in quasi-stable states when the transistor, or the diode, is on or off, under the assumption that the condition of continuity of the current through the choke is met.

Power Losses in Transistor

The average power loss in a transistor, during one cycle, when it is on and saturated, is determined by the expression

$$P_{ts} = \frac{1}{T} \int_0^{t_s} v_{ce}(t) i_c(t) dt. \quad (4.40)$$

The variations of the collector–emitter voltage and collector current are approximately linear,

$$\begin{aligned} v_{ce}(t) &= V_{ce}(I_{Lm}) + \frac{\Delta V_{ce}}{t_s} t \quad \text{and} \\ i_c(t) &= I_{Lm} + \frac{\Delta I_c}{t_s} t, \end{aligned} \quad (4.41)$$

where t_s is the time interval when the transistor is in saturation, I_{Lm} is the minimum current through the choke, $\Delta I_c = \Delta i_L = I_{Lm} - I_{Lm}$ is the variation of the collector current, and $v_{ce}(t)$ is the collector–emitter voltage of the transistor upon the turn-on, determined by

$$V_{ce}(I_{Lm}) = \varphi_t \ln \left[N(I_{Lm}) + \left(N(I_{Lm}) + \frac{\beta_N}{\beta_I} \right) \frac{I_{Lm}}{C} \right]. \quad (4.42)$$

ΔV_{ce} is the variation of the collector–emitter voltage when the transistor is on.

$$\Delta V_{ce} = V_{ce}(I_{LM}) - V_{ce}(I_{Lm}) = \varphi_t \ln \frac{N(I_{LM}) + \left(N(I_{LM}) + \frac{\beta_N}{\beta_I} \right) \frac{I_{LM}}{\Delta I_c}}{N(I_{Lm}) + \left(N(I_{Lm}) + \frac{\beta_N}{\beta_I} \right) \frac{I_{Lm}}{\Delta I_c}} \quad (4.43)$$

where β_N and β_I are the coefficients of the current gain in the normal and the reverse mode of operation. Introduction of (4.41) into (4.40), upon rearrangement, gives

$$P_{ts} = \frac{t_s}{T} \left[V_{ce}(I_{Lm}) I_{Lm} + \frac{1}{2} (\Delta V_{ce} I_{Lm} + V_{ce}(I_{Lm}) \Delta I) + \frac{\Delta V_{ce} I_{Lm}}{3} \right]. \quad (4.44)$$

Taking into account (4.9), the final expression is

$$P_{ts} = \frac{t_s}{T} \Delta V_{ce} I_O \left[\left(\frac{1}{2} + \frac{V_{ce}(I_{Lm})}{\Delta V_{ce}} + \frac{1}{12} \left(\frac{TV_o}{LI_o} \right) (1-D) \right) \right]. \quad (4.45)$$

The ratio P_{ts}/P_{tsmax} versus duty cycle is shown in Fig. 4.11a for different values of the parameter $a_1 = TV_o/(LI_o)$. P_{tsmax} is the maximum average power loss in the transistor that occurs at $D = 1$, which is understandable, since the transistor is permanently on. For $a_1 > 0.6$, P_{ts} exhibits maximum (dotted lines in Fig. 4.11a). Under realistic conditions, however, this maximum will not occur, because the condition for this maximum is in contradiction to the condition for the continuity of the current through the choke.

It straightforwardly shown that the average power loss of the turned-off transistor within one cycle is expressed by

$$P_{tz} = (1-D)V_1 I_{CO}, \quad (4.46)$$

where I_{CO} is the collector current with the open emitter circuit.

Power Losses in Diode

The average power loss in the diode during one cycle when it is on is determined by

$$P_d = \frac{1}{T} \int_{\tau}^T i_d^2(t) R_d dt + \frac{1}{T} \int_{\tau}^T i_d(t) V_{Dt} dt, \quad (4.47)$$

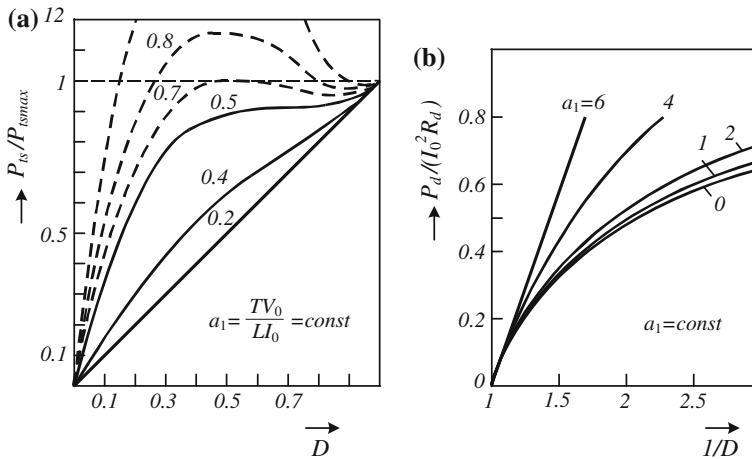


Fig. 4.11 Relative average power loss as function of D in the conducting transistor (a) and in the conducting diode (b)

where $i_d(t)$ is the diode current as function of time, R_d is the differential resistance of the diode, and V_{Dt} is the turn-on voltage of the diode (for silicon diodes, it is about 0.6 V). The current through the diode is approximately linear,

$$i_d(t) = I_{Lm} - \Delta I \frac{t}{T - \tau}. \quad (4.48)$$

If the power dissipated by the differential resistance of the diode is denoted by P_{d1} , then from (4.47) and (4.48) it follows

$$P_{d1} = R_d(1 - D)I_O^2 \left[1 + \frac{1}{12} \left(\frac{\Delta I}{I_O} \right)^2 \right]. \quad (4.49)$$

It is straightforward to show that the second member in (4.47) is

$$P_{d2} = V_{Dt}I_O(1 - D). \quad (4.50)$$

With (4.9) in mind, the total average power loss in a turned-on diode is expressed by

$$P_d = I_O^2 R_d(1 - D) \left[1 + \frac{1}{12} \left(\frac{TV_o}{LI_O} \right)^2 (1 - D)^2 \right] + I_O V_{Dt}(1 - D). \quad (4.51)$$

The differential diode resistance is approximately determined by

$$\begin{aligned} R_d &= \Delta V_d / \Delta I_d, \\ R_d &= \Delta V_d / \Delta I_d, \end{aligned}$$

where $\Delta I_d = I_{LM} - I_{Lm}$ and $\Delta V_d = v_d(I_{LM}) - v_d(I_{Lm}) = m \varphi_t \ln \frac{I_{LM} + I_{DS}}{I_{Lm} + I_{DS}}$, or taking into account that the reverse saturation current of the diode $I_{DS} \ll I_{Lm,m}$

$$\Delta V_d \approx m \varphi_t \ln \left(\frac{I_{LM}}{I_{Lm}} \right). \quad (4.52)$$

The maximum power P_d occurs at $D = D_{\min}$. By increasing D (decreasing V_1), the power losses in an open diode decreases monotonically (Fig. 4.11b). The average power losses during one cycle in a turned-off diode is

$$P_{dz} = DV_1 I_{DS}, \quad (4.53)$$

where I_{DS} is the reverse saturation current of the diode.

Power Losses in Choke

If the Ohmic resistance of the choke is denoted by R_L , then the average power losses in the choke while the transistor is conducting is determined by

$$P'_L = \frac{1}{T} \int_0^{\tau} R_L i_L^2(t) dt, \quad (4.54)$$

where

$$i_L(t) = I_{Lm} + \frac{\Delta I}{\tau} t. \quad (4.55)$$

By rearranging (4.54) and (4.55), one obtains

$$P'_L = DI_O^2 R_L \left[1 + \frac{1}{12} \left(\frac{TV_o}{LI_O} \right)^2 (1-D)^2 \right]. \quad (4.56)$$

The power losses in the choke while the diode is on are determined by (4.49), but with R_d replaced by R_L , i.e.,

$$P''_L = I_O R_L (1-D) \left[1 + \frac{1}{12} \left(\frac{TV_o}{LI_O} \right)^2 (1-D)^2 \right]. \quad (4.57)$$

The total power losses in the choke are $P_L = P'_L + P''_L$, i.e.,

$$P_L = I_O R_L \left[1 + \frac{1}{12} \left(\frac{TV_o}{LI_O} \right)^2 (1-D)^2 \right]. \quad (4.58)$$

Power Losses in Capacitor

The average power losses during one cycle in the series resistance of the capacitor of the output filter are determined by

$$P_C = \frac{1}{T} \int_0^{\tau} i_{C1}^2(t) R_C dt + \frac{1}{T} \int_{\tau}^T i_{C2}^2(t) R_C dt, \quad (4.59)$$

where $i_{C1}(t)$ and $i_{C2}(t)$ are the respective variations of the capacitor current (Fig. 4.3) when the control pulse is present and when the control pulse is not present. Since

$$i_{C1}(t) = \frac{\Delta I}{2} \left(\frac{2t}{\tau} - 1 \right),$$

the first member in (4.59) is

$$P'_C = DR_C \frac{\Delta I^2}{12}. \quad (4.60)$$

When the control pulse is not present

$$i_{C2}(t) = \frac{\Delta I}{2} \left(1 - \frac{t}{t - \tau}\right), \quad (4.61)$$

so the second member in (4.59) is determined by

$$P''_C = R_C(1 - D) \frac{\Delta I^2}{12}. \quad (4.62)$$

The total power losses in R_L is the sum of P'_C and P''_C , i.e.,

$$P_C = \frac{R_C}{12} \left[\frac{T}{L} V_o(1 - D) \right]^2. \quad (4.63)$$

4.1.1.5 Dynamic Losses of the Transistor and Diode

The previous section dealt with the analysis of power losses in quasi-stable states. It has been assumed that the transistor and the diode were the ideal switching elements (instantaneous turn-on and turn-off). In practice, however, the situation is different. The turn-on and turn-off times of the transistor and the diode cannot be neglected, particularly at higher frequencies. During the transition cycle the transistor is in the active region and the dissipation is highest. The question may be asked, what is the contribution of the dynamic losses compared to the total losses in the semiconductor (active) elements? It is clear that the dynamic losses compared to the total losses decrease proportionally to the decrease of the frequency. However, the minimum frequency is limited by other requirements (ripple in the output voltage, weight, volume of the converter, etc.).

Particular attention should be paid to the problem that may arise if the speeds of the transistor and diode are of the same order. These problems manifest themselves during the turn-on process of the transistor, because it is then that the transistor could be overloaded. As long as the diode is not on, the collector load of the transistor is very high (small impedance), so the amplitude of the current pulses increases (current shifts). These current pulses are transferred to the converter output and they increase the ripple of the output voltage. For this reason, the diode should be much faster than the transistor, or the turn-on process of the transistor should be slowed down.

In general, the driving stage of the switching transistor introduces its own delay because the base current is not an abrupt but an exponential function. Therefore, in

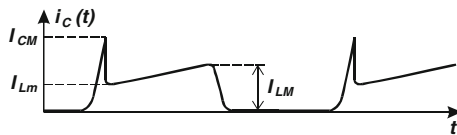


Fig. 4.12 Waveform of collector current

the considerations which follow it will be taken into account that the base current rises exponentially, determined by the time constant τ_b .

The transition phenomena in semiconductor devices will be analyzed by applying the charge control method which allows unique determination of turn-on/turn-off and delay times of the transistor and the diode and the variations of the currents during these intervals.

Transistor Turn On and Diode Turn Off

The variation of the current through the choke during the transient process is negligibly small. The amplitude of the overshoots of the collector current (Fig. 4.12) depends on the selected transistor and diode.

The variation of the base current of the controlling transistor during the turn-on process is

$$i_b(t) = I_b \left(1 - e^{-t/\tau_b} \right), \quad (4.64)$$

where τ_b —time constant of the base circuit, and I_b —constant base current. The collector current can be determined by applying the equation of charge continuity within the base region (Chap. 2). Since the initial condition is $Q(0) = 0$, then

$$i_c(t) = \beta I_b \left[1 - \frac{1}{1 - \frac{\tau_b}{\tau_c}} e^{-\frac{t}{\tau_c}} + \frac{\frac{\tau_b}{\tau_c}}{1 - \frac{\tau_b}{\tau_c}} e^{-\frac{t}{\tau_b}} \right], \quad (4.65)$$

where β is the common emitter current gain of the transistor and $\tau_c = \tau_\beta = 1/(2\pi f_\beta)$, and f_β is the cutoff frequency of the common emitter current gain. Upon application of the reverse bias, the diode is still conducting for some time. Namely, until the excess minority carriers surrounding the p-n junction are completely swept away, the diode will be in the state of conduction. The current through it is

$$i_d(t) = I_{Lm} - i_c(t), \quad (4.66)$$

where I_{Lm} is the minimum current through the choke.

It is of interest to determine the storage time of the diode (the time of discharge), because during that time the diode has a very small resistance and makes a high

load for the transistor. The fall time of the diode current in this case can be neglected. By applying the charge control method the delay time can be uniquely determined. Namely, the solution of the continuity equation gives the variation of the charge in the vicinity of the p–n junction of the diode

$$Q(t) = e^{-t/\tau_d} \left\{ \int_0^t i_d(t) e^{-t/\tau_d} dt + Q(0) \right\}, \quad (4.67)$$

where $i_d(t)$ —is the variation of the current through the diode, $Q(0)$ —is the initial charge in the diode and τ_d —is the time constant of the diode. Since $Q(0) = \tau_d I_{Lm}$, taking into account (4.66) and (4.65), the solution of (4.67) is obtained in the form

$$Q(t) = I_1 \tau_d - \beta I_b \tau_d \left[1 - e^{-t/\tau_b} + \frac{\tau_c^2}{(\tau_c - \tau_b) \cdot (\tau_c - \tau_d)} \left(e^{-t/\tau_c} - e^{-t/\tau_d} \right) + \frac{\tau_b^2}{(\tau_b - \tau_c) \cdot (\tau_b - \tau_d)} \left(e^{-t/\tau_b} - e^{-t/\tau_d} \right) \right]. \quad (4.68)$$

At the end of the storage time, the excess charge in the vicinity of the p–n junction is zero, i.e.,

$$Q(t_r) = 0. \quad (4.69)$$

From (4.69) and (4.68), after rearrangement, it follows

$$\frac{1}{N} = 1 - K_1 e^{-t_r/\tau_c} - K_2 e^{-t_r/\tau_c} + K_3 e^{-t_r/\tau_b}, \quad (4.70)$$

where $N = \frac{\beta I_b}{I_1}$,—the coefficient of saturation of the transistor after turn-on,

$$\begin{aligned} K_1 &= \frac{\tau_d^2}{(\tau_c - \tau_d)(\tau_b - \tau_d)}, \\ K_2 &= \frac{\tau_c^2}{(\tau_c - \tau_b)(\tau_c - \tau_d)}, \text{ and} \\ K_3 &= \frac{\tau_b^2}{(\tau_c - \tau_b)(\tau_b - \tau_d)}. \end{aligned} \quad (4.71)$$

Owing to a mathematical inconsistency in certain relations between time constants while solving (4.67), there are restrictions to the validity of Eq. (4.70). Two extreme cases are of practical interest.

1. When $\tau_b \approx 0$, then

$$i_c(t) = \beta I_b \left(1 - e^{-t/\tau_c}\right). \quad (4.72)$$

2. If $\tau_c \approx 0$ ($\tau_c \ll \tau_b$), it follows that

$$i_c(t) = \beta I_b \left(1 - e^{-t/\tau_b}\right). \quad (4.73)$$

In the first case ($\tau_b \approx 0$) it follows

$$\frac{1}{N} = 1 + \frac{\tau_d}{\tau_c - \tau_d} e^{-t_r/\tau_d} - \frac{\tau_c}{\tau_c - \tau_d} e^{-t_r/\tau_c}, \quad (4.74)$$

and in the second ($\tau_c \ll \tau_b$)

$$\frac{1}{N} = 1 + \frac{\tau_d}{\tau_b - \tau_d} e^{-t_r/\tau_d} - \frac{\tau_b}{\tau_b - \tau_d} e^{-t_r/\tau_d}. \quad (4.75)$$

The graphical solution of Eqs. (4.70), (4.74), and (4.75) for different ratios of the time constants, τ_d/τ_c and τ_b/τ_c , is shown in Fig. 4.13a, b. It is obvious that the storage time decreases with an increase of the coefficient of transistor saturation and with a decrease of the time constant of the base current. Figure 4.14 shows the dependence of the storage time on the ratio of the time constants of the diode and the transistor (τ_d/τ_c) with the coefficient of saturation of the transistor taken as a parameter.

Of particular interest is to establish how the amplitude of the current pulses depends on the ratio of the time constants of the diode and the transistor. In the case when $\tau_d > \tau_c$ and $\tau_b \approx 0$ the overshoots of the transistor current could be very high. Namely, it could then be assumed that the transistor is turned on instantaneously, so the current through the transistor, while the diode is still conducting, is equal to βI_b (Fig. 4.15).

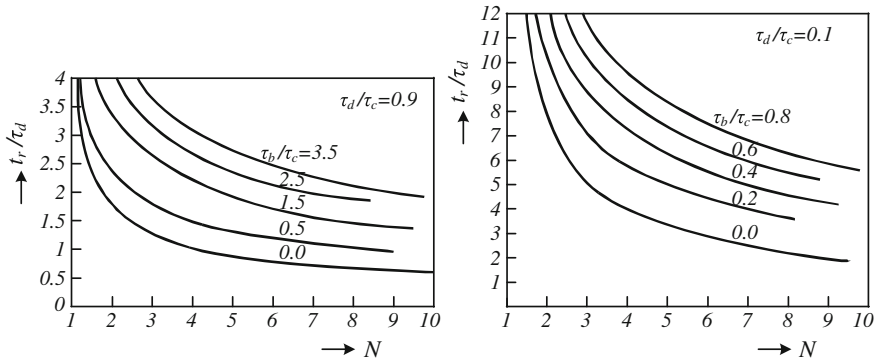


Fig. 4.13 Rise time as a function of the coefficient of transistor saturation

Fig. 4.14 Storage time as function of collector and diode currents

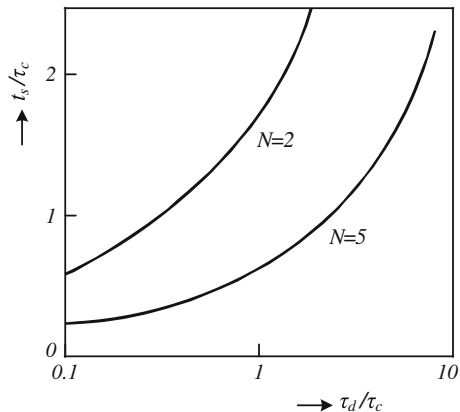
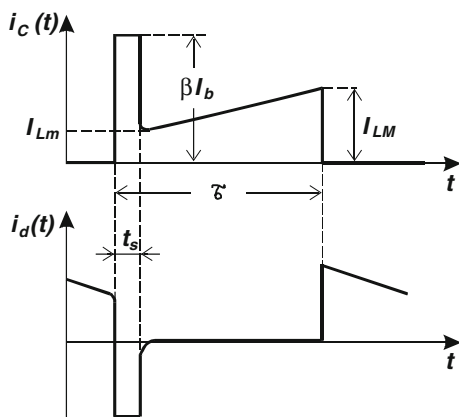


Fig. 4.15 Waveforms of τ_d/τ_c with the saturation factor as a parameter



When the storage time t_s is determined, it is then straightforward to determine the current overshoots for each specific case. Therefore, the maximum collector current is

$$I_m = \beta I_b \left[1 - \frac{1}{1 - \tau_b/\tau_c} e^{-t_r/\tau_c} + \frac{\tau_b/\tau_c}{1 - \tau_b/\tau_c} e^{-t_r/\tau_b} \right]. \quad (4.76)$$

Figure 4.16a, b shows a graphical representation of the dependence of the ratio I_{CM}/I_{Lm} on the transistor saturation coefficient for different ratios of the time constants τ_d/τ_c and τ_b/τ_c .

The dependence of the amplitude of the current pulses on the time constants is shown in Fig. 4.17.

It can be seen that the amplitude of the collector current increases with the increase of the saturation coefficient (the transistor is turned on faster) and with the

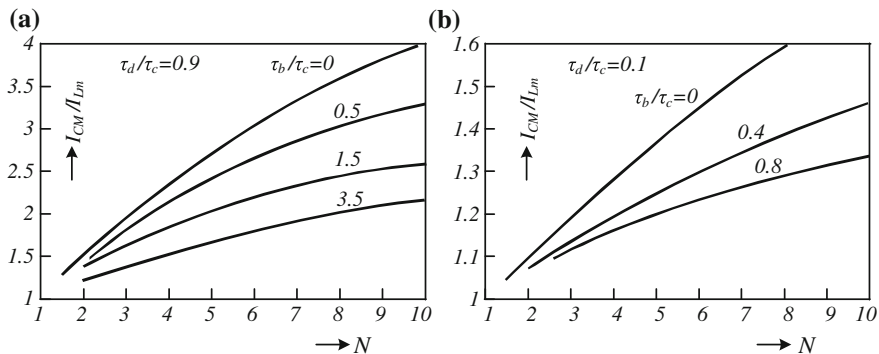
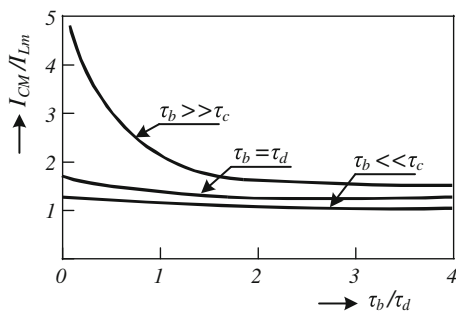


Fig. 4.16 Maximum collector current as a function of the saturation factor N with the ratio of the time constants τ_d/τ_c (a) and τ_b/τ_c (b) taken as a parameter

Fig. 4.17 I_{CM} as function of the ratio of the time constants



increase of the time constant τ_d (t_r increases). However, by increasing the time constant of the base current, I_{CM} decreases. Therefore, in the design of a converter a diode having as small time constant τ_d as possible should be selected, and if necessary, the turn-on process of the transistor should be slowed down by increasing τ_b .

Transistor Turn-Off

If the transistor is turned off by a negative base current $-I_{b2}$ and with the initial condition $Q(0) = \tau_c I_{CM}/\beta$, the application of the charge control method gives the collector current

$$i_c(t) = (I_{LM} + \beta I_{b2})e^{-t/\tau_c} - \beta I_{b2}, \quad (4.77)$$

where I_{CM} is the maximum current of the choke of the output filter. The turn-off time of the transistor can be determined from the condition $i_c(t) = 0$, so

$$t_f = \tau_c \ln \left(1 + \frac{1}{N_2} \right), \quad (4.77a)$$

where $1/N_2 = (I_{LM}/\beta I_{b2})$. If the negative base current is not provided ($N_2 = 0$), the turn-off time can be determined from the condition $i_c(t_f) = 0.1I_{LM}$, therefore, taking into account (4.77), it follows that $t_f = 2.3\tau_c$.

Power Losses

Power losses in semiconductor devices during transient processes consist of the losses during the storage time of the diode and the losses during the transistor turn-off process while the diode is conducting. Figure 4.18 shows the waveforms of the transistor and diode voltages and currents obtained with the integrated control at 50 kHz. Solid lines show current variations, and dotted lines voltage variations. During the transistor turn-on and turn-off, it may be assumed that the collector–emitter voltage is approximately equal to the input voltage.

Power losses in the transistor during turn-on are defined by

$$P_{tr} = \frac{V_1}{T} \int_0^{t_r} i_c(t) dt. \quad (4.78)$$

According to (4.65) and (4.78) it follows

$$P_{tr} = \frac{V_1 N(I_{LM}) I_{LM}}{T} \left\{ t_r - \frac{\tau_c (1 - e^{-t_r/\tau_c})}{1 - \tau_b/\tau_c} - \frac{\tau_b (1 - e^{-t_r/\tau_b})}{1 - \tau_c/\tau_b} \right\}. \quad (4.79)$$

Fig. 4.18 Voltage and current waveforms

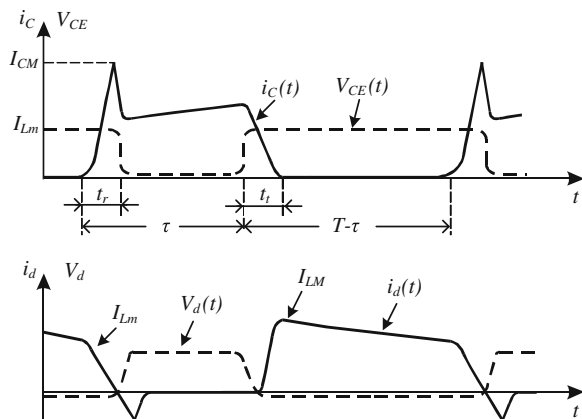


Figure 4.19a shows the relative dependence of the dynamic power losses in the transistor during its turn-on on the ratio τ_b/τ_d , for different ratios τ_d/τ_c . The power losses in the transistor during turn-off are defined by

$$P_{tf} \approx \frac{V_1}{T} \int_0^{t_f} i_c(t) dt. \quad (4.80)$$

where $i_c(t)$ and t_f are expressed by (4.77) and (4.78), respectively. The solution of (4.80), taking into account (4.78), turns out to be

$$P_{tf} = \frac{V_1 N_2 I_{LM}}{T} \left[\tau_c (1 - e^{-t_f/\tau_c}) - \left(1 - \frac{1}{N_2} \right) t_f \right]. \quad (4.81)$$

If instead of t_f in (4.81) one introduces (4.77a), then

$$P_{tf} = \frac{V_1 I_{LM} \tau_c}{T} \left[1 - N_2 \ln \left(1 + \frac{1}{N_2} \right) \right]. \quad (4.82)$$

By adding (4.79) and (4.82), one obtains the dynamic losses in the transistor during its turn-on and turn-off.

From the dependence of relative power losses in the transistor during turn-off on the factor N_2 (Fig. 4.19b) it is noticeable that increasing of N_2 decreases the power of losses, thus one should strive to make $N_2 > 1$. Since the turn-off time of power transistors is quite long, it is necessary to provide a negative base current in order to speed up the turn-off process.

The dynamic losses in the diode can be determined in a way similar to the one applied to the transistor. During the storage time the variation of the voltage across the diode can be neglected so it could be assumed that $V_d = V_{Dt}$ and

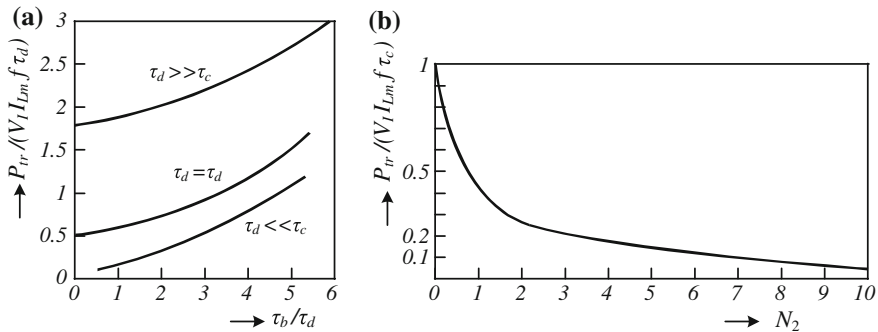


Fig. 4.19 Dynamic losses in the transistor during turn-on (a) and during turn-off (b)

$$P'_{\text{dd}} = \frac{V_{\text{Dt}}}{T} \int_0^{t_r} i_{\text{d}}(t) dt, \quad (4.83)$$

where the diode current is expressed by (4.66). From (4.83), upon rearrangement, one obtains that the average power of dissipation in the diode within one cycle during the storage time is

$$P'_{\text{dd}} = V_{\text{Dt}} I_{\text{Lm}} f t_r - \frac{V_{\text{Dt}}}{V_{\text{I}}} P_{\text{tr}}, \quad (4.84)$$

where P_{tr} is expressed by (4.79). The average power losses in the diode within one cycle during the transistor turn-off process are defined by

$$P''_{\text{dd}} = \frac{V_{\text{D}}}{T} \int_0^{t_f} i_{\text{d}}(t) dt. \quad (4.85)$$

Now the diode current is

$$i_{\text{d}}(t) = I_{\text{LM}} - i_{\text{c}}(t), \quad (4.86)$$

where the collector current of the transistor $i_{\text{c}}(t)$ is given by (4.77). Upon rearrangement

$$P''_{\text{dd}} = V_{\text{D}} I_{\text{LM}} f t_f - \frac{V_{\text{D}}}{V_{\text{I}}} P_{\text{tf}}, \quad (4.87)$$

where P_{tf} is determined by (4.82). The total power of dynamic losses is determined by (4.84) and (4.87). Since $V_{\text{Dt}} \approx V_{\text{D}}$

$$P_{\text{dd}} = V_{\text{D}} f (I_{\text{Lm}} t_r + I_{\text{LM}} t_f) - \frac{V_{\text{D}}}{V_{\text{I}}} (P_{\text{tr}} + P_{\text{tf}}). \quad (4.88)$$

4.1.1.6 Parameter Optimization

The calculation of the optimum parameters is one of the most important, and at the same time the most complex, tasks in the design of any system, thus the same is valid in the design of DC/DC converters. It comprises the exact description of the processes, power relations in all circuits and elements, the selection of a criterion function, and the corresponding optimization algorithm. The mathematical models of the circuits and devices include nonlinear functions; therefore the optimization can only be performed with the aid of a computer.

The optimization criteria depend on the goals, technical requirements, and output parameters. The most frequent technical requirements for converters are: maximum variation of the input voltage, output voltage stabilization, output power, electrical and thermal regimes. The goal functions are usually minimum weight, volume, price and maximum factor of efficiency. Consequently, optimization can be performed by parts. The problem of optimization as a whole can be solved through the application of specific subroutines for optimization of individual goal functions. Basically, the most complex and at the same time the most important problem in the design of converters is the optimization of the factor of efficiency. It is clear that the thermal regime, particularly the regimes of the semiconductor devices, is dependent on the power losses. Closely related are the cooling problems and also the volume and the weight of the cooling system whose share in the overall measures of the converter is very significant. Consequently, by determining the maximum factor of efficiency the solution is obtained not only for the problem of minimum losses but also for the problem of minimum weight and volume.

From the analysis of power losses it can be concluded that the total losses are dependent on three independent parameters: the saturation coefficient of the transistor (N), the frequency of the controlling transistor (f), and the time constant of the base current (τ_b). These are the parameters that a designer has to determine when selecting an adequate transistor and diode in accordance with the specific technical requirements. Therefore, the task of designing a minimum-loss converter (maximum coefficient of efficiency) is reduced to the determination of optimum parameters N , f , and τ_b . It should be noted that the listed parameters have limitations which are automatically introduced into the process of searching for the optimum values.

There are a number of optimization methods for nonlinear functions of several variables: the gradient method, method of second derivatives, and method of direct search. For practical reasons, here is the most suitable method of direct search.

4.2 Galvanically Isolated Forward Converter

Another class of DC/DC converters is the forward converter with galvanically isolated input and output (Fig. 4.20). In this converter, after the transistor T_r is turned on, the energy from the primary circuit is transferred directly to the secondary. Simultaneously, through the diode D_1 (D_2 is off) this energy is accumulated in the choke and fed to the load. While T_r is off, the energy from the choke is fed to the load by the diode D_2 . During this interval the core of the transformer is demagnetized through the third winding which is connected to the primary source by the diode D_3 . In this process one part of the energy is returned to the input.

The third winding has to be closely coupled with the primary winding in order to avoid voltage spikes while T_r is turning off. Usually these two windings have the same number of turns. Then, the collector voltage of T_r while off approaches $2V_i$.

The presentation of the voltage and current waveforms in Fig. 4.20b implies that the transformer and the switching elements (transistor and diodes) are ideal, and

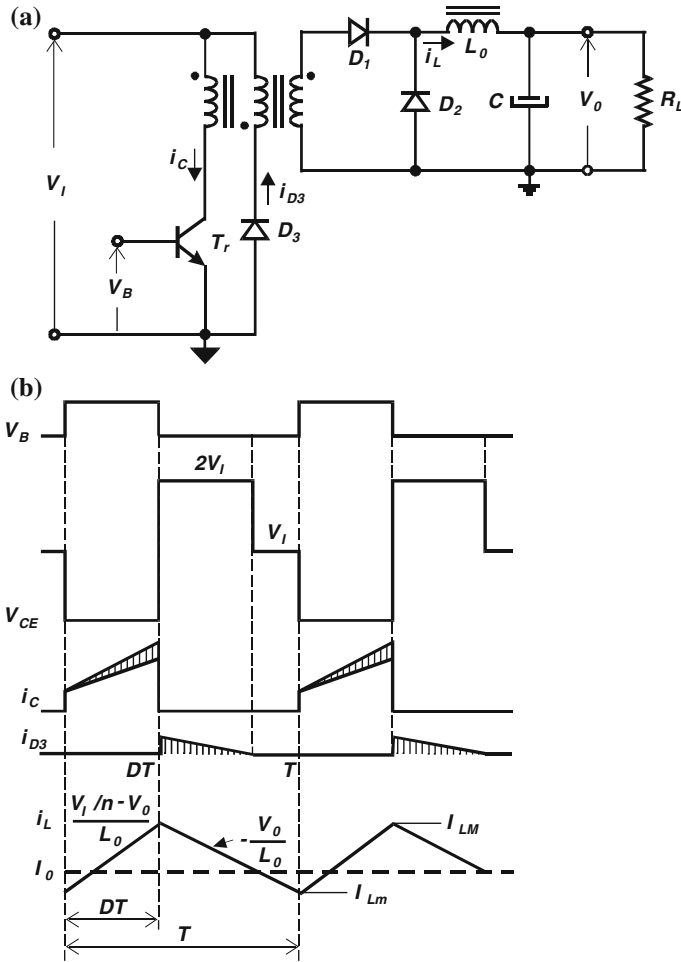


Fig. 4.20 Forward converter with separated input and output (a) and voltage and current waveforms (b) in continuous mode

that the variation of the output voltage is negligibly small. The current through the choke while T_r is conducting is given by

$$i_L(t) = I_{Lm} + \frac{V_1}{n} \frac{V_o}{L_0} t, \quad (4.89)$$

and while T_r is off

$$i_L(t) = I_{LM} - \frac{V_o}{L_o}t, \quad (4.90)$$

where I_{Lm} and I_{LM} are the minimum and maximum currents through the choke L_o , respectively. By equating the increase and the decrease of the current i_L the output voltage is obtained as

$$V_o = D \frac{V_I}{n}, \quad (4.91)$$

where $D = T_1/T$ is the duty cycle of the control pulses (the ratio of the interval of conduction of T_1 and the total cycle $T = T_1 + T_2$), and n is the ratio of the primary and the secondary number of turns. Thus, the output voltage does not depend on the load current but only on the duty cycle of the control pulses (V_I and n are constants).

The above analysis has been made under the assumption that the current through the output choke was continuous. This is possible; however, while the transistor is off the current drops to zero. Since filtering of the output voltage would then be much more difficult, this mode is considered unsuitable and to be avoided. If the discontinuity of the current through the choke L_o is to be avoided, the load current has to be higher than the average value of the ripple of the current i_L , i.e.,

$$I_0 > \frac{\Delta i_L}{2} = \frac{I_{LM} - I_{Lm}}{2}. \quad (4.92)$$

Since $I_{LM} = i_L(DT)$, from (4.89) and (4.91) the boundary between the continuous and the discontinuous mode of operation is

$$I_0 > \frac{V_I T}{2nL_o} D(1 - D) = I_{og}. \quad (4.93)$$

Figure 4.21 shows the normalized output characteristics of the converter for different values of the duty cycle. In the discontinuous operating mode (to the left of the dotted line) the output voltage is dependent on the load current. For this reason the discontinuous mode should be avoided. This is accomplished by connecting a constant load to the output (zero or intrinsic load) similarly to the converter without a galvanic separation between the input and the output.

The collector current of the transistor linearly increases and consists of the magnetization current of the primary winding and the current of the output winding referred to as the primary circuit, i.e.,

$$i_c = \frac{i_L}{n} + \frac{V_I}{L_1}t. \quad (4.94)$$

The collector current reaches maximum at the end of transistor conduction ($t = DT$), so

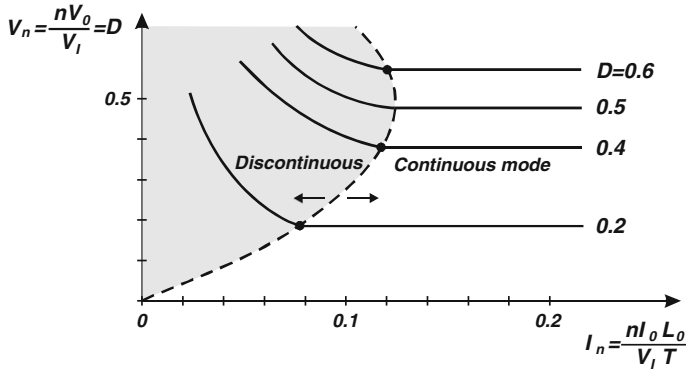


Fig. 4.21 Normalized output voltage as function of the load current and duty cycle

$$I_{C\max} = \frac{I_{LM}}{n} + \frac{nV_o}{L_I} T. \quad (4.95)$$

The magnetization current is represented by cross-hatched areas in Fig. 4.20b. Most of the time it can be neglected, so $I_{C\max} \approx I_{CM}/n$.

After the transistor is off, the demagnetization diode D_3 conducts and ensures the flow of the discharging current from the core of the transformer. The voltage of the third winding, approximately equal to $-V_I$, is referred to as the primary winding voltage. Owing to this the collector voltage is higher than V_I . Since the core discharging winding usually has the same number of turns as the primary, the maximum collector voltage is

$$V_{CE\max} = 2V_I. \quad (4.96)$$

Then the magnetization and demagnetization times are equal, so (4.96) applies during the interval DT (Fig. 4.20b). This also means that the maximum ratio pulse/(no pulse) has to be less than 0.5.

The required volume of the transformer core can be calculated by

$$V = \frac{\mu_o \mu_c I_{\text{mag}}^2 L_I}{B_{\max}^2}, \quad (4.97)$$

where $B_{\max}$ is the maximum induction in the given material, μ_o and μ_c are physical constants and

$$I_{\text{mag}} = \frac{nTV_o}{L_I}$$

is the magnetization current of the core.

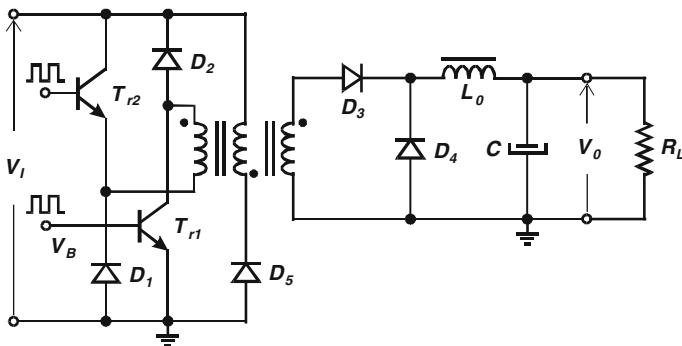


Fig. 4.22 Half-bridge forward converter

If the breakdown voltage of the selected transistor is lower than $2V_I$ ($BV_{CBO} < 2V_I$), the half-bridge forward converter using two transistors is recommended (Fig. 4.22). The transistors are controlled so that they are both on or off. When off, the diodes D_1 and D_2 are conducting, so

$$V_{CEmax} \approx V_I. \quad (4.98)$$

It should be emphasized that the forward converter can be used in a multioutput version (Fig. 4.23). The output voltages are practically independent. Their ratio is equal to the ratio of the number of the secondary turns.

The favorable features of the forward converters are:

- relative simplicity,
- the ripple (maximum variation) of the output voltage is significantly smaller than that of the flyback converters.

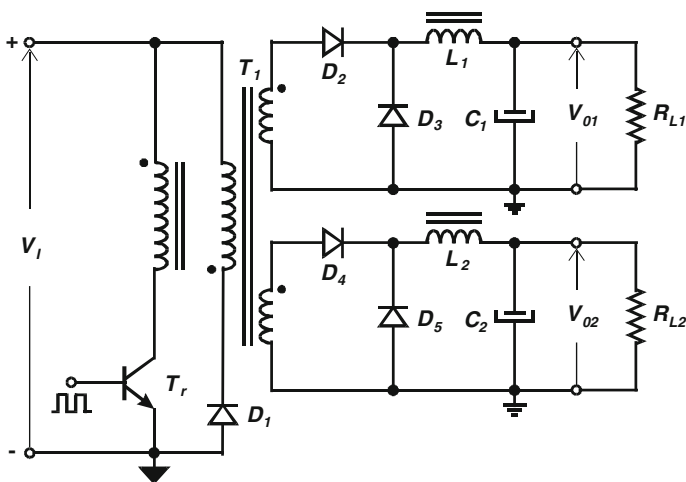


Fig. 4.23 Two-output forward converter

- the dimensions of the transformer are small and an air gap is not required, and
- there is no risk of the transformer core saturation.

Unfavorable features of the converters having isolated output are:

- the breakdown voltage of the switching transistor has to be twice the input voltage (the exception is the half-bridge circuit),
- a separate winding is required for the demagnetization of the core.

Example 4.3 A forward converter having galvanic isolation (Fig. 4.20) is characterized by the following parameters: $V_I = 48$ V, $L_o = 0.4$ mH, $C = 100$ μ F, $N_1/N_2 = 1.5$, $N_1/N_3 = 1$, $R_1 = 10$ Ω , $f = 35$ kHz, $D = 0.4$, and $L = 5$ mH. Determine:

- the output voltage,
- the maximum and minimum currents through the choke L_o ,
- the maximum collector current of the transistor,
- the load resistance when the converter operates at the boundary between the continuous and the discontinuous mode.

- According to (4.91): $V_o = DV_I(N_1/N_2) = 0.4 \times 48/1.5 = 12.8$ V
- The average value of the current through the choke L_o is equal to the load current, $I_I = I_O = V_o/R_L 12.8/10 = 1.28$ A.

The change of the current through the choke L_o is

$$\Delta i_L = \frac{V_I/(N_1/N_2) - V_o}{L_o} DT = \frac{(48/1.5 - 12.8) \times 0.4}{(0.4 \times 10^{-3})(35 \times 10^3)} = 0.55 \text{ A},$$

so the maximum and the minimum value are

$$I_{LM} = I_O + \Delta i_L/2 = 1.28 + 0.55/2 = 1.55 \text{ A}$$

$$I_{Lm} = I_O - \Delta i_L/2 = 1.28 - 0.55/2 = 1 \text{ A}$$

- Taking into account (4.95) it follows

$$I_{Cmax} = \frac{I_{LM}}{N_1/N_2} + \frac{V_o N_1/N_2}{L_1} T = \frac{1.55}{1.5} + \frac{12.8 \times 1.5}{(5 \times 10^{-3})(35 \times 10^3)} = 0.55 \text{ A},$$

$$I_{Og} = \frac{V_o}{R_{Lg}} = \frac{V_I}{2(N_1/N_2)L_o f} D(1 - D),$$

- so

$$R_{Lg} = 2L_o f / (1 - D) = 2(0.4 \times 10^{-3})(35 \times 10^3) / (1 - 0.4) = 46.67 \Omega.$$

4.3 Boost Converter

The supply voltages of some parts or of a complete unit are often higher than the voltage of the primary source, like in portable professional equipment where batteries are the primary source. In such cases the conversion and stabilization of the voltage is carried out mainly in two ways. The conventional solution employs a so called *push-pull* converter where the increase of the output voltage is accomplished, among other means, by an adequate transformer. The output voltage can be from several times to several hundred times higher than the input voltage. When the voltage ratio is $1 < V_o/V_I < 5$, the DC/DC converters—voltage boosters are mainly used. The basic scheme of such a converter is shown in Fig. 4.24.

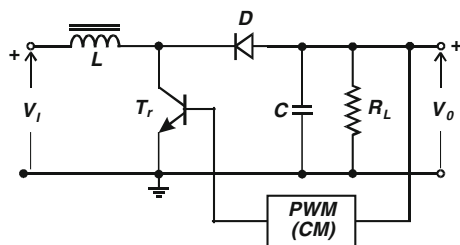
At the output of the control module (CB) a sequence of pulses is generated and fed to the switching transistor T_r . When the output of the control module is high, the transistor T_r is on and in saturation. The current and magnetic flux in the core start increasing. The diode D is off and it separates the load from the low-resistance part of the circuit (collector-emitter of the transistor). The load current is maintained by the energy stored in the capacitor. When the output of the control module is low, the transistor is off. Then the magnetic flux in the choke decreases and the electromotive forces in the winding are pulling in the direction opposite to that while the transistor was on. The diode is conducting and the output voltage is the sum of the input voltage and the voltage across the choke. The current through the choke decreases and reaches its minimum when the transistor is switched on. This cycle is repeated periodically.

The power delivered to the load can be divided in two parts. The first part is delivered directly by the input voltage (V_I) source. The second part is obtained on account of the electromagnetic energy that was stored in the choke while the transistor was in saturation. The ratio of the conduction and the nonconduction time of the transistor controls the stored electromagnetic energy and consequently the ratio of the output and the input voltage.

4.3.1 Analysis of the Basic Scheme

For the purpose of the analysis of the basic parameters the following justifiable assumptions will be made: the transistor and diode are ideal switches (instantaneous

Fig. 4.24 Basic scheme of boost converter



turning on or off, the on-resistance is negligibly small, the off resistance is infinitely large), the Ohmic resistance of the choke is negligible, the output voltage V_o and the load current I_o are constant.

When the transistor is on, the complete input voltage is across the choke, so

$$V_I = L \frac{di_L}{dt}. \quad (4.99)$$

By integrating the last equation, one obtains the current through the choke

$$i_L(t) = I_{Lm} + \frac{V_I}{L} t, \quad (4.100)$$

where I_{Lm} is the minimum current through the choke. After the transistor is turned off, the circuit is closed through the load R_L , the diode, the choke L , and the input V_I . By neglecting the voltage drop across the diode, it follows

$$V_I - V_o = L \frac{di_L}{dt}. \quad (4.101)$$

The integration of (4.101) gives

$$i_L(t) = I_{LM} + \frac{V_I - V_o}{L} t, \quad (4.102)$$

where I_{LM} is the maximum current through the choke. The minimum and maximum currents through the choke are obtained at the instant when the transistor is turned on and off, respectively. Namely

$$I_{Lm} = I_{LM} + \frac{V_I - V_o}{L} (T - \tau), \quad (4.103)$$

$$I_{LM} = I_{Lm} + \frac{V_I}{L} \tau. \quad (4.104)$$

By equating the changes of the current through the choke while the transistor is on and off, it turns out that

$$V_o = \frac{V_I}{(1 - D)}. \quad (4.105)$$

The variation of the output voltage as function of the duty cycle is shown in Fig. 4.25a. It can be seen that the output voltage is always higher than the input voltage. Since usually $D < 0.8$, the output voltage can be controlled within limits $V_I < V_o < 5V_I$. Essentially, the limitation on the ratio V_o/V_I is imposed by the real parameters of the elements of the converter. Namely, the resistances of the conducting transistor and diode are greater than zero. The series resistance of the

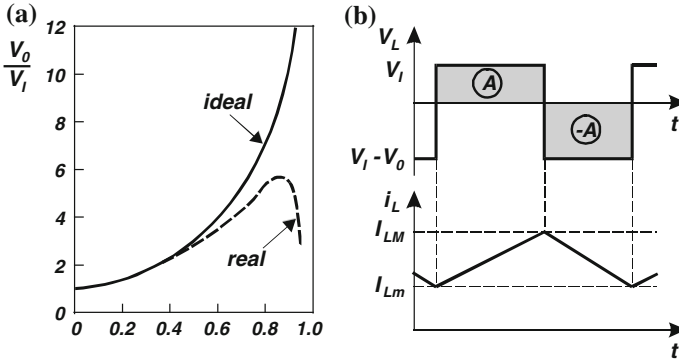


Fig. 4.25 Normalized output voltage as function of the duty cycle (a) and the current and voltage waveforms of the choke (b)

capacitor and the windings exists. The transient times are also not zero. All these contribute to the real characteristic $V_o/V_i = f(D)$ shown by the dashed line in Fig. 4.25a. The influence of the real parameters is particularly marked for large values of the duty cycle.

Since it has been assumed that the scheme was ideal, the power losses in the converter are negligible, thus $P_I = P_o$, or

$$V_I I_{Isr} = V_o I_o. \quad (4.106)$$

From (4.105) and (4.106) it turns out that the ratio of the output current and the average value of the input current of the converter is

$$\frac{I_o}{I_{Isr}} = 1 - D. \quad (4.107)$$

Example 4.4 Draw the characteristics $V_o/V_i = f_1(D)$ and $\eta = f_2(D)$ of a boost converter with $r_L/R_L = 0.01$ or $r_L/R_L = 0.05$, where r_L is the series resistance of the choke and R_L is the load resistance.

If other elements of the converter were ideal the power losses would exist only in the series resistance r_L of the choke. The input power is $P_I = P_o + P_{rL}$, or

$$V_I I_{Isr} = I_{Isr}^2 r_L + V_o I_o.$$

The average value of the current through the choke is determined by (4.107), so

$$V_I \frac{I_o}{1-D} = r_L \frac{I_o^2}{(1-D)^2} + V_o I_o.$$

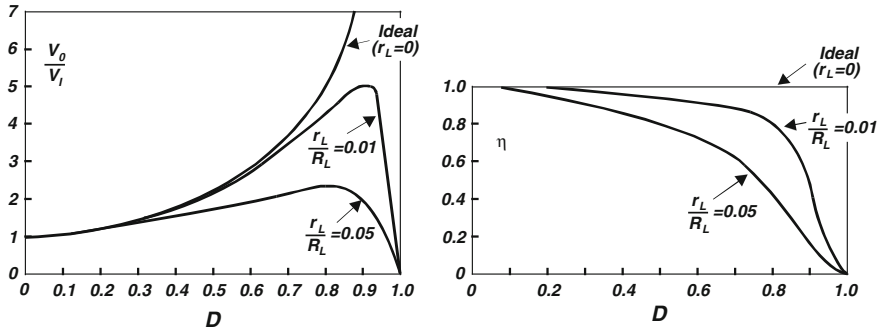


Fig. 4.26 $V_o/V_i = f_1(D)$ and $\eta = f_2(D)$

Since $I_O = V_o/R_L$, it turns out that

$$\frac{V_o}{I_O} = \frac{1}{1-D} \frac{1}{1 + \frac{r_L}{R_L(1-D)^2}}. \quad (4.108)$$

The coefficient of efficiency is specified as

$$\eta = \frac{P_o}{P_o + P_{r_L}} = \frac{V_o^2/R_L}{V_o^2/R_L + r_L I_{Lsr}^2} = \frac{V_o^2/R_L}{V_o^2/R_L + r_L \frac{(V_o/R_L)^2}{(1-D)^2}} = \frac{1}{1 + \frac{r_L}{R_L(1-D)^2}}. \quad (4.109)$$

On the basis of (4.108) and (4.109) follows

$$\frac{V_o}{V_i} = \frac{\eta}{1-D} = \eta \left(\frac{V_o}{V_i} \right)_{\text{ideally}}.$$

Functions $V_o/V_i = f_1(D)$ and $\eta = f_2(D)$ are shown in Fig. 4.26. It is obvious that losses in the series resistance of the choke rise sharply as the duty cycle approaches unity.

4.3.1.1 Operating Modes of the Transistor and Diode

The maximum currents and the maximum reverse voltages of the transistor and diode should be determined. Figure 4.25b shows the variation of the current through the choke, the transistor, and the diode as a function of time, neglecting transient phenomena. The maximum current of the transistor is equal to the maximum current of the choke I_{LM} .

It is of practical interest, however, to determine the relation between the maximum transistor current and the load current. Since the load current is given by

$$I_D = \frac{I_{Lm} + I_{LM}}{2} (1 - D),$$

it is straightforwardly shown that

$$I_{cmax} = I_O \frac{T}{T - \tau} - \frac{V_I - V_o}{2L} (T - \tau). \quad (4.110)$$

From (4.105) and $I_O = V_o/R_L$ it follows that

$$I_{cmax}/I_O = \frac{1}{1 - D} + \frac{R_L T}{2L} D(1 - D). \quad (4.111)$$

Figure 4.27 shows the ratio I_{cmax}/I_O as a function of the duty cycle and with the constant $K_1 = R_L T/L$ taken as a parameter. The maximum current through the diode is equal to the maximum current through the transistor.

By neglecting the voltage drop across the diode, the collector–emitter voltage of the transistor, when off, is equal to the output voltage. The same conclusion may be drawn for the reverse voltage of the diode, i.e.,

$$V_{CB} = |V_{Dinv}| = V_I/(1 - D).$$

In order to reduce the currents and the reverse voltages of the semiconductor devices, a three-terminal choke is used (Fig. 4.28).

This also simplifies the design of the control module because for a given ratio V_o/V_I the variation of the duty cycle is reduced. Let N_{12} and N_{13} be the number of turns between the points 1 and 2 and 1 and 3, respectively, and their ratio $n = N_{13}/N_{12}$. It can be shown that the output voltage as a function of the transformation ratio n is expressed by

Fig. 4.27 Normalized maximum current as function of the duty cycle

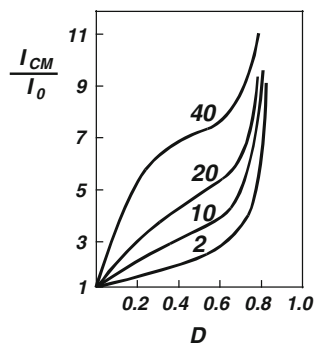
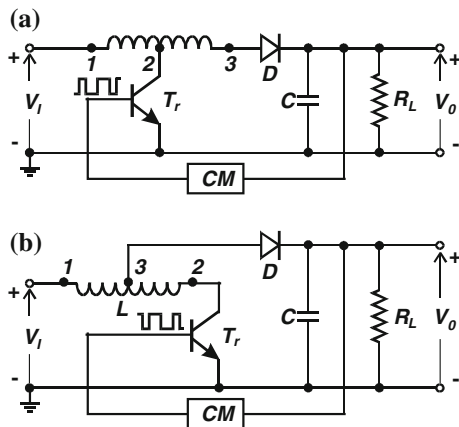


Fig. 4.28 Converter using three-terminal chokes with switching transistor (a), and diode (b) connected to middle terminal



$$V_o = V_I \left(1 + \frac{nD}{1-D} \right). \quad (4.112)$$

Therefore, (4.105) is a special case of (4.112) for $n = 1$. Figure 4.29a presents the dependence of the output voltage on the duty cycle with the transformation ratio taken as a parameter.

If the reverse voltage of the transistor is critical, the circuit in Fig. 4.29a is used. The maximum collector-base voltage in this case is lower than the output voltage and amounts

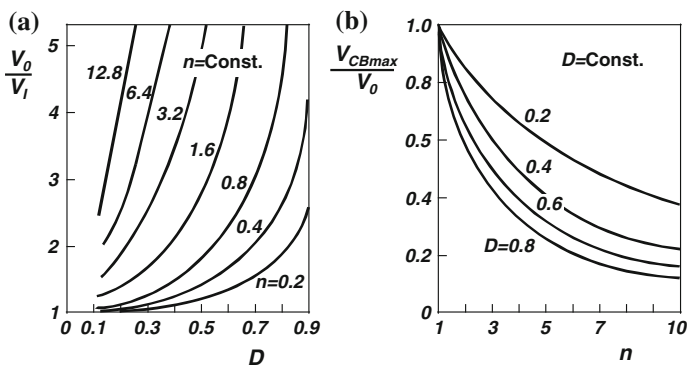


Fig. 4.29 Normalized output voltage (a) and normalized collector-base voltage as functions of n and D (b)

$$V_{CB\max} = \frac{V_o}{1 + D(n - 1)}. \quad (4.113)$$

Equation (4.113) applies only if $n > 1$, whereas for $n < 1$ (Fig. 4.29b) $V_{CB\max} = V_o$. Figure 4.29b presents the dependence of $V_{CB\max}/V_o$ on the transformation coefficient n with the duty cycle D taken as a parameter.

The maximum reverse voltage of the diode is

$$V_{D\text{inv}} = \frac{nV_I}{1 - D}. \quad (4.114)$$

4.3.2 Variation of the Output Voltage

The variation of the output voltage is equal to the variation of the voltage across the capacitor. While the transistor is on, the load current is kept constant on the account of the discharge of the capacitor C . The variation of the voltage across the capacitor is then

$$v'_c = V_{C\max} e^{-t/CR_L}, \quad (4.115)$$

where $V_{C\max}$ is the maximum output voltage which is obtained at the end of the interval when the transistor is off. At $t = \tau = DT$ the output voltage is at minimum and its variation is determined by

$$\Delta v'_c = V_{C\max}(1 - e^{-DT/CR_L}). \quad (4.116)$$

In order to keep the load current constant, the condition $DT \ll CR_L$ has to be fulfilled, so (4.116) is approximately

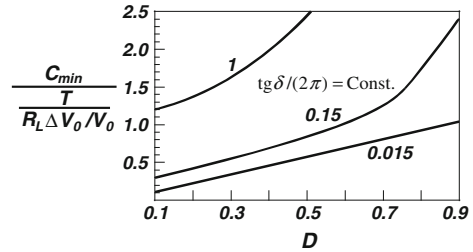
$$\Delta v'_c \approx V_{C\max} \frac{DT}{CR_L}. \quad (4.117)$$

Since $\Delta v'_c \ll V_o$ and taking into account (4.105), it follows that

$$\Delta v'_c \approx \frac{TV_I}{CR_L} \frac{D}{1 - D}. \quad (4.118)$$

The resistive component of the voltage variation across the capacitor is expressed by $i_c(t)R_C$ and it represents the voltage drop across the series active resistance of the capacitor. The maximum value of this voltage is obtained at the end of the pause, and it amounts

Fig. 4.30 Minimum capacitance versus duty cycle



$$\Delta v_c'' = R_C I_{Cmin}, \quad (4.119)$$

where

$$I_{Cmin} = \frac{V_1}{R_L(1-D)^2} - \frac{V_1 T D}{2L} \quad (4.120)$$

is the minimum collector current. The overall variation of the output voltage is

$$\Delta V_o = \Delta v_c' + \Delta v_c'' = \frac{V_1}{R_L} \left[\frac{T D}{C(1-D)} + \frac{R_C D}{(1-D)^2} - \frac{T D R_L R_C}{2L} \right]. \quad (4.121)$$

From (4.121), one can determine the minimum value of the capacitance for which the variation of the output voltage does not exceed a permitted variation

$$C > \frac{V_o T}{R_L \Delta V_o} \left[D + \frac{\text{tg} \delta}{2\pi} \left(\frac{1}{1-D} - \frac{K_1 D(1-D)}{2} \right) \right], \quad (4.122)$$

where $K_1 = TR_L/L$ and $\text{tg} \delta$ is the tangent of the angle of losses of the capacitor.

Figure 4.30 shows the relative dependence of the minimum capacitance on the duty cycle with the constant $\text{tg} \delta / (2\pi)$ as parameter. It can be seen that for a given ΔV_o the minimum capacitance increases with an increase of the duty cycle and this dependence is more pronounced for higher values of $\text{tg} \delta$.

Example 4.5 The boost converter (Fig. 4.24) is characterized by the following parameters: $V_1 = 50$ V, $\tau = DT = 50$ μ s, $L = 250$ μ H, and $R_L = 2.5$ Ω . The transistor and the diode can be considered ideal. One should determine:

- the frequency of control pulses for which the output voltage is 75 V, and the converter operates in the continuous mode,
- the average values of the input and the output current,
- the capacitance of the output capacitor for which the variation of the output voltage is not greater than 1 %.

- (a) According to (4.105) it follows that $D = 1 - V_I/V_O = 1 - 50/75 = 1/3$, and from $DT = 50 \mu\text{s}$: $T = 50/D = 50 \times 3 = 150 \mu\text{s}$, or $f = 1/T = 6.66 \text{ kHz}$.
- (b) The average value of the load current is $I_O = V_O/R_L = 75/2.5 = 30 \text{ A}$, and according to (4.107) the average value of the input current is

$$I_{Iav} = I_O/(1 - D) = 30/(1 - 1/3) = 90/2 = 45 \text{ A}.$$

The variation of the current through the choke is

$$\Delta i_L = \frac{V_I}{L} DT = \frac{50}{250 \times 10^{-6}} 50 \times 10^{-6} = 10 \text{ A}.$$

The maximum and the minimum current through the choke are respectively

$$I_{LM} = I_{Isr} + \Delta i_L/2 = 45 + 10/2 = 50 \text{ A},$$

$$I_{Lm} = I_{Isr} - \Delta i_L/2 = 45 - 10/2 = 40 \text{ A}.$$

The variations of the current and the voltage of the choke are shown in Fig. 4.31a.

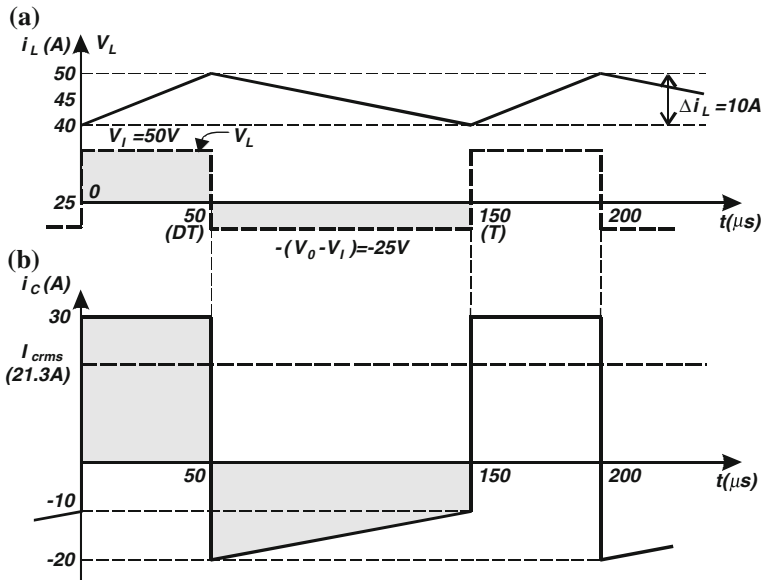


Fig. 4.31 Variations of the current and the voltage of the choke (a) and the waveform of the current through the capacitor (b)

- (c) Since the ESR of the output capacitor is neglected, the variation of the output voltage is determined by (4.116), so

$$C > \frac{TD}{R_L(\Delta V_o/V_o)} = \frac{50 \times 10^{-6}}{25 \times 0.01} = 200 \mu\text{F}.$$

The waveform of the current through the capacitor is shown in Fig. 4.31b. From this it follows that the average square value of the current through the capacitor is

$$I_{\text{Ceff}} = I_{\text{Crms}} = \sqrt{\frac{1}{T} \int_0^T i_C^2(t) dt} = \sqrt{\int_0^{50} 30^2 dt + \int_0^{100} \left(\frac{10}{100}t - 20 \right)^2 dt} = 21.3 \text{ A}.$$

$$I_{\text{Crms}} = 21.3 \text{ A}.$$

4.3.3 Boundary Between the Continuous and the Discontinuous Mode

The previous analysis applies if the current through the choke is continuous. At the boundary between the continuous and the discontinuous mode the minimum current through the choke is zero (Fig. 4.32a), so the average value of the current through the choke at this boundary is

$$I_{\text{Lg}} = \Delta i_L / 2 = I_{\text{LM}} / 2 = \frac{V_I}{2L} DT = \frac{V_o T}{2L} D(1 - D). \quad (4.123)$$

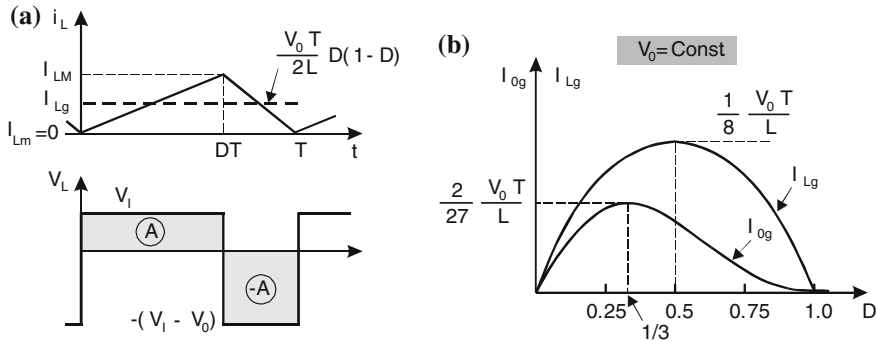


Fig. 4.32 The current and voltage of the choke as functions of time (a) and the output current and the average current through the choke at the boundary between the continuous and the discontinuous mode as functions of the duty cycle (b)

The average value of the current through the choke in the voltage boosters is equal to the average value of the input current. By combining (4.123) and (4.107) one obtains that the output current I_{Og} at the boundary of the continuous mode is

$$I_{Og} = I_{Lg}(1 - D) = \frac{V_o T}{2L} D(1 - D)^2. \quad (4.124)$$

The usual requirement is that the output voltage is constant. The boundary currents I_{Og} and I_{Lg} versus duty cycle, at $V_o = \text{const.}$, are shown in Fig. 4.32b.

The current through the choke has a maximum at $D = 0.5$

$$I_{Lg\max} = \frac{TV_o}{8L} = 0.125 \frac{TV_o}{L}, \quad (4.125)$$

whereas the maximum of the output current at the boundary is

$$I_{Og\max} = \frac{2}{27} \frac{TV_o}{L} = 0.074 \frac{TV_o}{L}, \quad (4.126)$$

at $D = 1/3$. The values of the boundary currents I_{Lg} and I_{Og} can be expressed in terms of their maximum values

$$I_{Lg} = 4D(1 - D)I_{Lg\max}, \quad (4.127)$$

$$I_{Og} = \frac{27}{4} D(1 - D)^2 I_{Og\max}. \quad (4.128)$$

4.3.4 Discontinuous Mode

As a consequence of an increase of the load resistance or a decrease of the load current the converter switches over to the discontinuous operating mode. Allowing the input voltage and the duty cycle in this process to be constant (in practice, the duty cycle varies to keep the output voltage constant, but this does not change the validity of the analysis under the assumption $D = \text{const.}$).

The current and the voltage of the choke are zero during $(D + D_1)T < t < T$, which corresponds to the interval D_2T (Fig. 4.33a). This leads to a decrease of the average value of the current through the choke I_L and an increase of the output voltage. Namely, the current $i_L \neq 0$ during $(D + D_1)T$, its average value during one cycle is

$$I_L = \frac{I_{LM}}{2} \frac{(D + D_1)T}{T} = \frac{V_1 D T}{2L} (D + D_1). \quad (4.129)$$

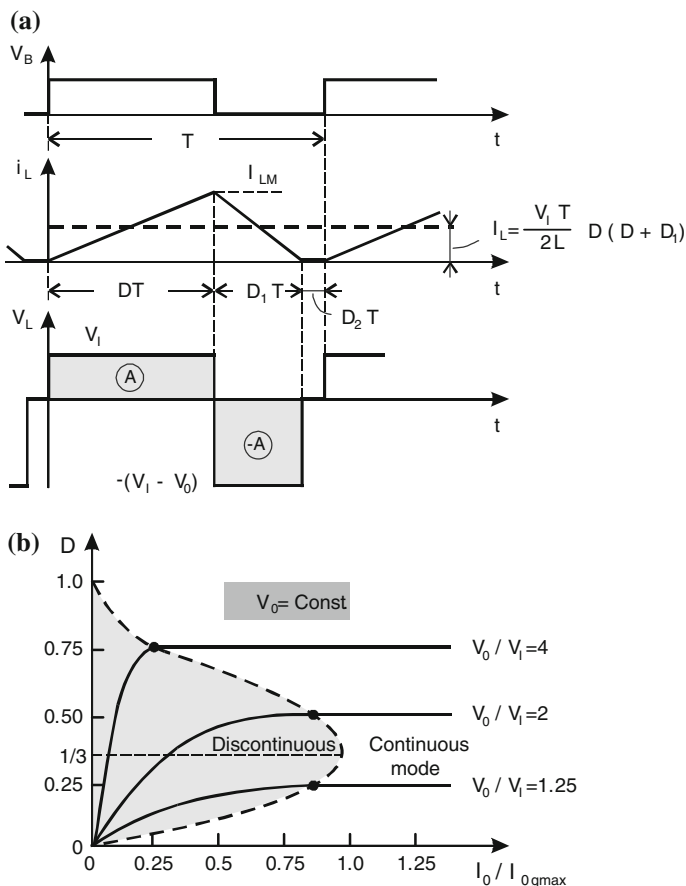


Fig. 4.33 Current and voltage of the choke in the discontinuous mode (a) and the duty cycle as function of the normalized output current and ratio V_o/V_i at a constant output voltage (b)

On the other hand, the integral part of the voltage across the choke during one cycle is zero, or the absolute values of the areas above and below the time axis are equal, i.e.,

$$V_I DT = -(V_I - V_o) D_1 T, \quad (4.130)$$

therefore

$$\frac{V_o}{V_I} = \frac{D + D_1}{D_1}. \quad (4.131)$$

Since the power losses of an ideal circuit are negligible, $P_I = P_o$ and

$$\frac{I_O}{I_{Isr}} = \frac{D_1}{D + D_1}. \quad (4.132)$$

The input current and the current through the choke are equal, so $I_{Iav} = I_L$. By combining (4.133) and (4.129) it turns out that the output current in the discontinuous mode is

$$I_O = \frac{V_1 T}{2L} D D_1. \quad (4.133)$$

In practice, the usual requirement is that $V_o = \text{const.}$ in the discontinuous mode too. This can be accomplished by varying the duty cycle D as a function of the output current while keeping the ratio V_o/V_1 constant. From (4.123), (4.125), and (4.126) one obtains that

$$D = \sqrt{\frac{4}{27} \frac{V_o}{V_1} \left(\frac{V_o}{V_1} - 1 \right) \frac{I_O}{I_{Ogmax}}}. \quad (4.134)$$

Figure 4.33b shows the duty cycle as a function of the normalized output current for different values of the ratio V_o/V_1 . The dashed line parabola is the boundary between the continuous and the discontinuous mode.

4.3.5 Power Losses

Power losses in individual elements will be analyzed in the manner similar to the one applied for the forward converters. Power losses in the saturated transistor are defined by

$$P_{ts} = \frac{1}{T} \int_0^{t_s} R_s i_c^2(t) dt, \quad (4.135)$$

where R_s is the output resistance of a saturated transistor. If the turn-on and the turn-off time of the transistor are neglected and taking into account (4.105), from (4.135), after rearrangement, it turns out that

$$P_{ts} = I_O^2 R_s \frac{D}{(1-D)^2} \left[1 + \frac{1}{12} \left(\frac{V_o T}{I_O L} \right)^2 D^2 (1-D)^4 \right]. \quad (4.136)$$

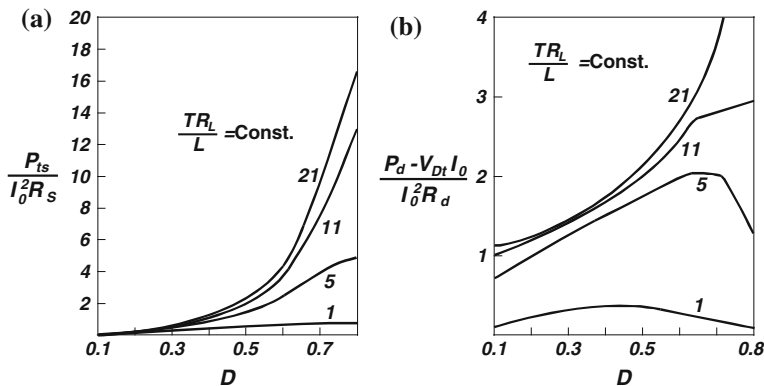


Fig. 4.34 Normalized losses in the transistor (a) and normalized losses in the diode (b)

The resistance R_s is defined by

$$R_s = \frac{\Delta V_{ce}}{\Delta I_c} = \frac{V_{ce}(I_{LM}) - V_{ce}(I_{Lm})}{I_{LM} - I_{Lm}}, \quad (4.137)$$

where I_{LM} and I_{Lm} are the maximum and the minimum transistor current, respectively and ΔV_{ce} is the variation of the collector–emitter voltage of a saturated transistor.

The average power losses during one cycle in a conducting diode is expressed by

$$P_d = I_o^2 R_d \frac{1}{1-D} \left[1 + \frac{1}{12} \left(\frac{V_o T}{I_o L} \right)^2 D^2 (1-D)^4 \right] + V_{Dt} I_o, \quad (4.138)$$

where R_d is the differential resistance of the diode

$$R_d = \Delta V_d / \Delta I_d,$$

ΔV_d is the variation of the voltage and $\Delta I_d = I_{LM} - I_{Lm}$ is the variation of the current of the conducting diode.

Figure 4.34a and b show the relative power losses of the conducting transistor and the diode as functions of the duty cycle with the constant $V_o T / (I_o L)$ as parameter.

It can be shown that the average power losses during one cycle in the Ohmic resistance of the choke and in the series resistance of the capacitor are respectively

$$P_L = I_o^2 R_L \frac{1}{(1-D)^2} \left[1 + \frac{1}{12} \left(\frac{V_o T}{I_o L} \right)^2 (1-D)^4 \right], \quad (4.139)$$

$$P_C = I_O^2 R_C \left[\frac{D}{1-D} + \frac{1}{12} \left(\frac{V_o T}{I_O L} \right)^2 D^2 (1-D)^3 \right]. \quad (4.140)$$

The average power losses during one cycle in the nonconducting transistor and diode are respectively

$$P_{tz} = V_I I_{co}, \quad (4.141)$$

$$P_{dz} = V_I I_{Do} \frac{D}{1-D}. \quad (4.142)$$

This analysis concerns the losses during the quasi-stable intervals. The dynamic losses in the semiconductor devices (diode and transistor) can be determined in a manner similar to the one applied for the forward converters.

4.4 Indirect Converter

The basic circuit is shown in Fig. 4.35. When the MOS transistor M is on, energy is accumulated in the choke. Simultaneously, the diode is off and it separates the input from the output. The load current is provided by the capacitor C . During the next half-cycle, while the transistor M is off, the diode is on. Now the energy is exchanged between the choke and the capacitor whereby the capacitor makes up for the energy lost during the previous half-cycle.

Therefore, here the transfer of energy from the input to the output is indirect (intermediary). Namely, during one half-cycle the input energy is accumulated in the choke and in the next half-cycle, when the choke is separated from the input, the accumulated energy is transferred to the output load. Sometimes the term “accumulation” is used since the energy during one half-cycle is accumulated in the choke and in the second half-cycle it is transferred to the load.

Fig. 4.35 Basic circuit of a indirect converter

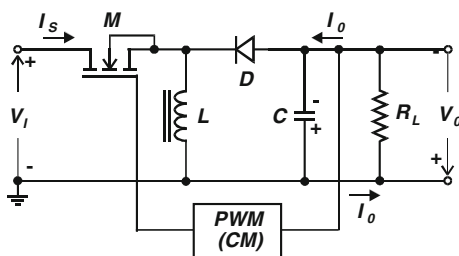
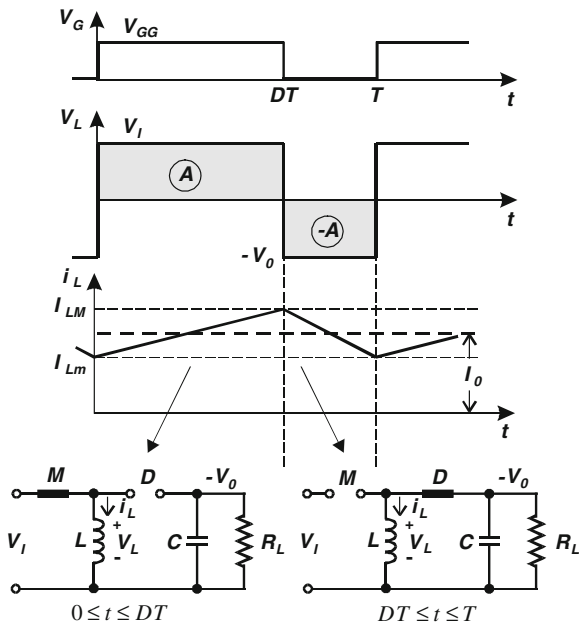


Fig. 4.36 Voltages and current of the choke and the equivalent circuit of the indirect converter



When the transistor M is on ($V_G = V_{GG}$), the voltage across the choke is constant and equal to $V_L = V_I - V_{DS} \approx V_I$ (Fig. 4.36), so the current through the choke is a linear function of time

$$i_L(t) = I_{Lm} + \frac{V_I}{L}t. \quad (4.143)$$

The diode is off, and the load current is provided only by the capacitor C (Fig. 4.36, during $0 < t < DT$).

During the second half-cycle ($T - DT$), when the transistor is off ($V_G = 0$), an electromotive force of the opposite sign is induced in the choke. Therefore, the voltage across the choke changes the sign, switching the diode to the state of conduction, so $V_L = -V_o - V_D \approx -V_o$. The capacitor is now being recharged by the energy accumulated in the choke (Fig. 4.36, for $DT < t < T$). If the variation of the output voltage is neglected, the current through the choke is determined by

$$i_L(t) = I_{LM} - \frac{V_o}{L}t. \quad (4.144)$$

In (4.143) and (4.144), I_{LM} and I_{Lm} are the maximum and the minimum current through the choke, respectively. The variations of the current i_L in both half-cycles are equal

$$\frac{V_1}{L}DT = \frac{V_o}{L}T(1-D), \quad (4.145)$$

therefore, it turns out that

$$V_o = V_1 \frac{D}{1-D}. \quad (4.146)$$

Since losses in idealized converter circuits are negligible, the power of the load is equal to the power of the primary source, i.e., $P_1 = V_1 I_1 = V_o I_o$, and taking into account (4.146)

$$I_o = I_1 \frac{1-D}{D}. \quad (4.147)$$

Depending on the duty cycle D any relation between the input and the output voltage is possible ($V_o > V_1$ or $V_o \leq V_1$). Namely, for $D > 0.5$, $V_o > V_1$; for $D < 0.5$, $V_o < V_1$ and for $D = 0.5$, $V_o = V_1$. For this reason these converters are often called Step Up/Step-Down or Buck–Boost converters.

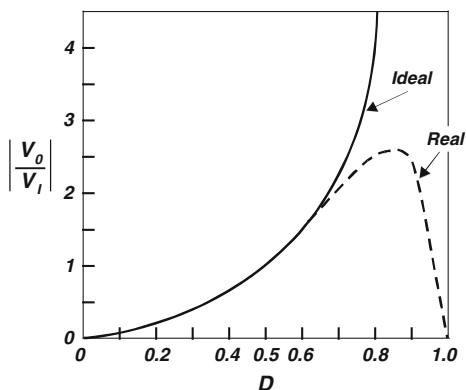
In addition, the output voltage is of the opposite polarity with respect to the input voltage, so the converter in Fig. 4.34 is often called the reverse or inverting converter.

The ratio V_o/V_1 as a function of the duty cycle D is shown in Fig. 4.37. The solid line corresponds to the idealized circuit Eq. (4.14).

If real parameters of the circuit elements are taken, the function $V_o/V_1 = f(D)$ is shown by the dashed line in Fig. 4.37. The drain–source voltage of the turned-off transistor is

$$V_{DS} = V_1 + V_o = V_1/(1-D) \quad (4.148)$$

Fig. 4.37 Ratio V_o/V_1 as function of duty cycle D



Therefore, the breakdown voltage of the transistor has to be $BV_{DS} > V_I/(1 - D)$, which may be several times larger than the input voltage. For instance, if $D = 0.8$, $BV_{DS} > 5V_I$.

4.4.1 Boundary Between the Continuous and the Discontinuous Mode

At the boundary of the continuous mode at $t = T$, the current through the choke is zero. With (4.144) in mind, the average current through the choke at the boundary between the continuous and the discontinuous mode is

$$I_{Lg} = \frac{1}{2}I_{LM} = \frac{V_I}{2L}DT = \frac{V_o T}{2L}(1 - D). \quad (4.149)$$

The output current is $I_O = I_L - I_I$, and according to (4.149) and (4.147)

$$I_{Og} = \frac{V_o T}{2L}(1 - D)^2. \quad (4.150)$$

The maximum values of the currents at the boundary are for $D = 0$

$$I_{Lgmax} = \frac{V_o T}{2L} = I_{Ogmax} \quad (4.151)$$

Now (4.150) can be written in the form

$$I_{Og} = I_{Ogmax}(1 - D)^2. \quad (4.152)$$

4.4.2 Discontinuous Mode

In the discontinuous mode, the current and the voltage of the choke are zero during the interval D_2T (Fig. 4.38a). The average value of the current through the choke is

$$I_L = \frac{V_I T}{2L}D(D + D_1). \quad (4.153)$$

The absolute values of the areas above and below the time axis of the waveform of the choke voltage (shaded areas in Fig. 4.38a) are equal, i.e.,

$$V_I DT = V_o D_1 T, \quad (4.154)$$

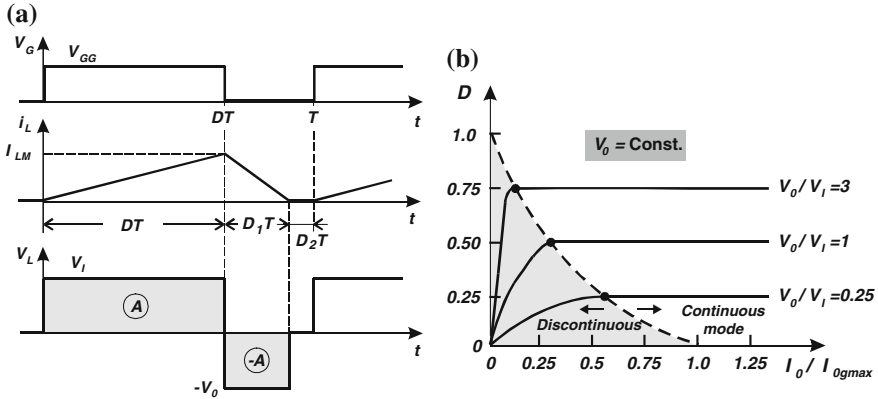


Fig. 4.38 Current and voltage of the choke in the discontinuous mode (a) and the duty cycle as function of the normalized output current and ratio V_o/V_I at $V_o = \text{const.}$ (b)

therefore it follows that

$$\frac{V_o}{V_I} = \frac{D}{D_1}. \quad (4.155a)$$

From the condition that the input and the output power are equal ($P_o = P_I$) and (4.155a) it follows

$$\frac{I_o}{I_I} = \frac{D_1}{D}. \quad (4.155b)$$

On the other hand, the output current is $I_o = I_L - I_I$, thus from (4.155b) and (4.153) one obtains

$$I_o = \frac{V_I T}{2L} D D_1 = \frac{V_o T}{2L} D_1^2 = I_{ogmax} \left(\frac{V_I}{V_o} \right)^2 D^2. \quad (4.156)$$

In order to maintain the output voltage constant the duty cycle has to be made variable. For this reason, it is useful to consider the dependence of the duty cycle on the load current at $V_o/V_I = \text{const.}$ From (4.156) it follows

$$D = \begin{cases} \frac{V_o}{V_I} \cdot \sqrt{\frac{I_o}{I_{ogmax}}}, & I_o < I_{og}, & \text{discontinuous mode} \\ \text{const.}, & I_o > I_{og}, & \text{continuous mode} \end{cases} \quad (4.157)$$

Equation (4.157) is shown graphically in Fig. 4.38b. The dashed line denotes the boundary between the continuous and the discontinuous mode. In the range of the continuous mode, the duty cycle does not depend on the output current but only on the ratio V_o/V_I .

Example 4.6 For the indirect converter in Fig. 4.39:

- derive expressions for the V_o/V_I versus duty cycle D in continuous mode,
- draw the waveforms of voltages and currents of the transistor, the inductor and the diode,
- derive expressions for V_o/V_I as a function of the duty cycle D in the discontinuous mode, and
- repeat (b) for the discontinuous mode.

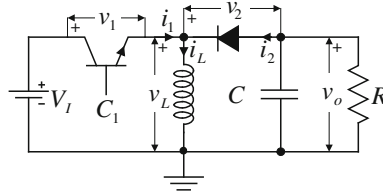


Fig. 4.39 Indirect DC/DC converter

- In the case of $D < 1/2$ it follows that $V_o < V_I$, while if $D > 1/2$ one obtains that $V_o > V_I$. In the continuous mode the waveforms of the marked voltages and currents are shown in Fig. 4.40a.

For the time interval $0 < t < DT_S$, when transistor T leads, we get
 $i_1 = i_L$, $v_1 = 0$, $i_2 = 0$, $v_2 = V_I + V_O$, $v_L = V_I$. In this time interval the input voltage source delivers energy to the inductor.

In the interval $DT_S < t < T_S$, the diode D leads, and the inductor delivers energy to the load, so it follows

$$i_1 = 0, \quad v_1 = V_I + V_O, \quad i_2 = i_L, \quad v_2 = 0, \quad v_L = -V_O.$$

Based on the condition that the average value of the voltage on the inductor is equal to 0 it follows

$$\bar{v}_L = 0 \Rightarrow V_I DT_S - V_O(1 - D)T_S = 0 \Rightarrow \frac{V_o}{V_I} = \frac{D}{1 - D}, \quad \frac{I_O}{I_I} = \frac{1 - D}{D} \\ (P_o = P_I).$$

- (b) Waveforms of voltages and currents at the transistor, diode and inductor are shown in Fig. 4.40a.
- (c) For discontinuous mode it can be written that

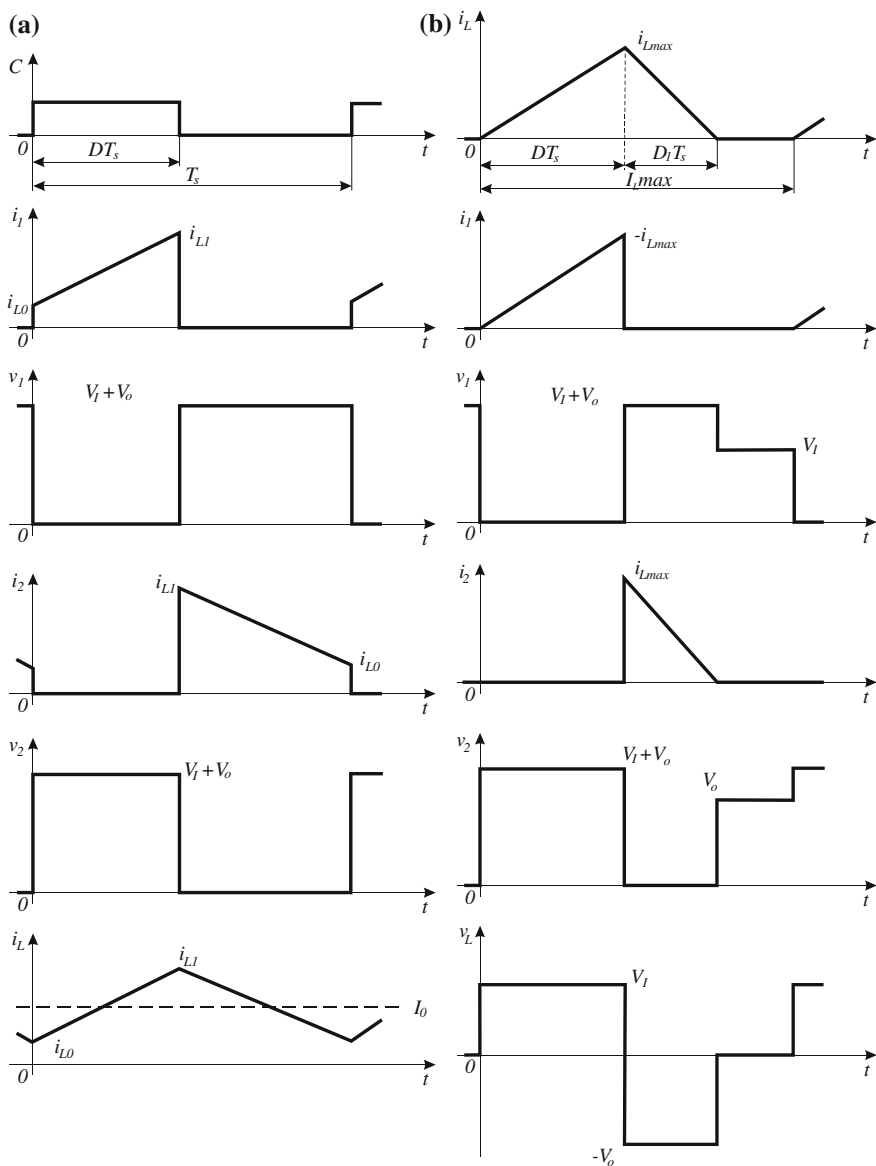


Fig. 4.40 Waveforms of marked voltages and currents of indirect converter for continuous (a), and discontinuous working mode (b)

$$\begin{aligned}
(D + D_1)T_S < t < T_S, \quad i_L = 0, \quad i_2 = 0, \\
i_1 = 0, \quad v_L = 0, \quad v_2 = V_o, \quad v_1 = V_1, \\
\bar{v}_L = 0 \Rightarrow V_1 D T_S - V_o D_1 T_S = 0 \\
\Rightarrow \frac{V_o}{V_1} = \frac{D}{D_1} \Rightarrow D_1 = D \frac{V_1}{V_o}; \\
I_O = \bar{i}_2 = \frac{1}{2} i_{L\max} D_1 \Rightarrow i_{L\max} = \frac{V_o}{L} D_1 T_S \\
\Rightarrow I_O = \frac{V_o T_S}{2L} D_1^2 = \frac{V_o T_S}{2L} D^2 \frac{V_1^2}{V_o^2} = \frac{V_o}{R} \\
\Rightarrow \left(\frac{V_o}{V_1} \right)^2 = \frac{RT_S}{2L} D^2 = \frac{D^2}{k}, \quad k = \frac{2L}{RT_S}, \\
\frac{V_o}{V_1} = \frac{D}{\sqrt{k}}.
\end{aligned}$$

The operating conditions in the continuous mode are obtained from the boundary value for the parameter D_1 , which is $D_1 = 1 - D$. From this condition it follows

$$k = D^2 \left(\frac{V_1}{V_o} \right)^2 \Rightarrow k_B = D^2 \frac{(1-D)^2}{D^2}, \text{ where } k_B = (1-D)^2.$$

For $k > k_B$ converter is in the continuous mode and $D_1 > 1 - D$. For $k < k_B$ the converter is in the discontinuous mode and $D_1 < 1 - D$.

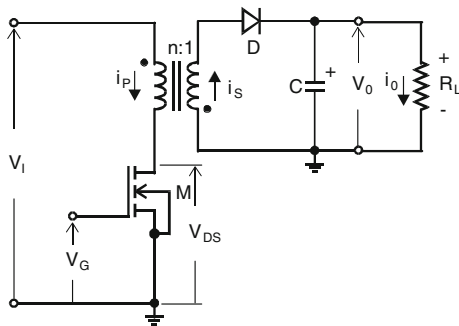
- (d) The waveforms of voltages and currents at the transistor, the diode and the inductor for the discontinuous mode are given in Fig. 4.40b.

4.4.3 Indirect Converter with Galvanic Separation

The indirect converter with galvanic isolation (flyback converter) (Fig. 4.41) has found a very wide use. Here in addition to the galvanic separation of the input and output, it is possible to have multiple outputs. The output can be of the same sign as the input. The switching transistor is less loaded (lower maximum current) compared to the basic circuit in Fig. 4.35.

The principle of operation is the same as for the basic circuit (Fig. 4.35). This converter uses a choke with a double winding. The current flows alternately through the primary and the secondary. While the transistor M is on ($0 < t < DT$), the diode is off, so that the current flows only through the primary winding. During the second quasi-stable interval ($DT < t < T$), the diode D is on and the transistor M is

Fig. 4.41 Flyback converter having galvanic separation



off. The energy accumulated in the primary is transferred to the load via the secondary. In the idealized equivalent circuit (Fig. 4.41), the transformer is represented by an ideal transformer, having a transformation ratio $n = N_1/N_2$, and the winding having magnetization inductance L_m .

During the interval $0 < DT$ (Fig. 4.42a), the primary voltage is $V_1 = V_I = \text{const.}$ and the primary current is

$$i_1 = I_{Lm,m} + \frac{V_I}{L_m} t, \quad 0 \leq t \leq DT \quad (4.158)$$

where $I_{Lm,m}$ is the minimum magnetization current. The primary and the secondary winding are wound up in the opposite directions, thus the secondary voltage is negative and the diode is off ($i_D = 0$). The current I_{DS} of the conducting transistor is equal to the input current, and it reaches maximum at $t = DT$, i.e.,

$$I_{IM} = I_{Lm,M} = I_{DSM} = I_{Lm,m} + \frac{V_I}{L_m} DT. \quad (4.159)$$

During $DT < t < T$, the transistor M is off and the diode is conducting (Fig. 4.42b). The secondary voltage is equal to the output voltage, so the primary voltage is $V_1 = nV_O$. The current of the magnetization winding

$$i_{Lm} = I_{Lm,M} - \frac{nV_O}{L_m} (t - DT), \quad DT \leq t \leq T, \quad (4.160)$$

is referred to the secondary as

$$i_D = ni_{Lm} = nI_{Lm,M} - \frac{n^2 V_O}{L_m} t, \quad DT \leq t \leq T, \quad (4.161)$$

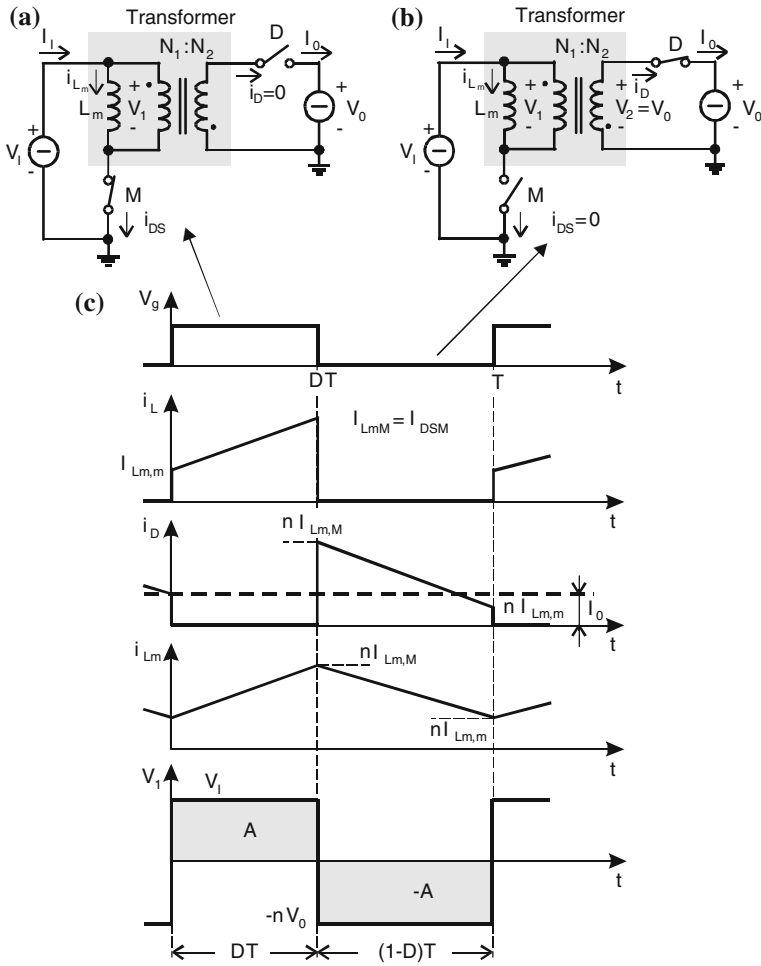


Fig. 4.42 Equivalent circuits of the idealized circuit (a) and (b) and the characteristic waveforms in the continuous mode (c)

The average value of the voltage V_1 is zero. In other words, the areas of the voltage V_1 waveform with respect to the time axis are equal, i.e.,

$$V_1 DT = nV_0(1-D)T, \quad (4.162)$$

therefore it follows that

$$V_0 = \frac{V_1}{n} = \frac{D}{1-D}. \quad (4.163)$$

Therefore, compared to the basic circuit (Fig. 4.35) the output voltage of the flyback converter with galvanic separation is lower $n = N_1/N_2$ times.

The DC component of the output current I_O is equal to the average value of the secondary current, or of the diode D, i.e.,

$$I_O = \frac{1}{T} \int_0^T i_D(t) dt = \frac{n}{T} \int_{DT}^T \left[I_{Lm,M} - \frac{nV_o}{L_m}(t - DT) \right] dt. \quad (4.164)$$

After rearrangement it follows that

$$I_O = n(1 - D) \left[\frac{I_{Lm,M} + I_{Lm,m}}{2} + \frac{nV_o}{L_m} DT \right]. \quad (4.165)$$

The preceding analysis concerns the continuous mode of the current through the magnetization winding. In the discontinuous mode in the part of the quasi-stable interval $T - DT$, when the transistor is off, the magnetization current i_{Lm} and the voltage V_I are equal to zero. Namely,

$$i_{Lm} = \begin{cases} 0, & 0 \leq t \leq DT \\ I_{Lm,M} - \frac{nV}{L_m}(t - DT), & DT \leq t \leq (D + D_1)T \\ 0, & (D + D_1)T \leq t \leq DT, \end{cases} \quad (4.166)$$

while

$$V_I = \begin{cases} V_I, & 0 \leq t \leq DT \\ -nV_o, & DT \leq t \leq (D + D_1)T \\ 0, & (D + D_1)T \leq t \leq DT. \end{cases} \quad (4.167)$$

The positive and the negative area of the waveform of the voltage V_I with respect t the time axis are equal, i.e.,

$$V_I DT = nV_o D_1 T, \quad (4.168)$$

therefore it follows that

$$\frac{V_o}{V_I} = \frac{D}{nD_1}. \quad (4.169)$$

In the idealized circuit, the input and the output power are equal ($P_I = V_I I_I = P_o = V_o I_o$), and the ratio of the average values of the input and the output current is

$$\frac{I_O}{I_I} = \frac{nD_1}{D}, \quad (4.170)$$

where

$$I_I = \frac{1}{T} \int_0^T i_1(t) dt = \frac{1}{T} \int_0^{DT} \frac{V_I}{L_m} t dt = \frac{V_I T}{2L_m} D^2. \quad (4.171)$$

On the basis of (4.171), (4.169), and (4.168) it follows that

$$\frac{nV_o}{V_I} = \frac{D^2}{2I_{On}}, \quad (4.172)$$

where

$$I_{On} = I_O / (nV_I T / L_m) = \frac{I_O L_m}{nV_I T} \quad (4.173)$$

is the normalized output current. The normalized output static characteristics $nV_o/V_I = f(I_{On})$ for different values of the duty cycle are shown in Fig. 4.41. At the boundary between the continuous and discontinuous mode the output voltages values according to (4.172) are equal, i.e.,

$$\frac{D}{1-D} = \frac{D^2}{2I_{Ong}}, \quad (4.174)$$

where I_{Ong} is the normalized boundary value of the output current

$$I_{Ong} = D(1-D)/2. \quad (4.175)$$

The maximum value of the drain–source voltage of a nonconducting transistor is

$$V_{DSmax} = V_I + nV_o = V_I / (1-D). \quad (4.176)$$

Thus, the breakdown drain–source voltage has to be (Fig. 4.43)

$$BV_{DS} > V_I(1-D). \quad (4.177)$$

If this condition is not met, a circuit using two transistors (Fig. 4.44) is used. Both transistors are simultaneously on or off. In the off state of M_1 and M_2 , the diodes D_1 and D_2 are conducting and keep the drain–source voltage to value $V_{DSmax} = V_I + V_D \approx V_I$.

Fig. 4.43 Normalized output static characteristics $nV_o/V_i = f(I_{on})$ for different values of the duty cycle

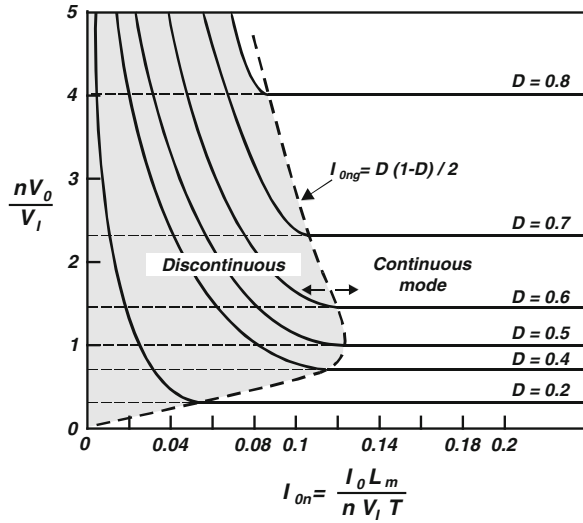
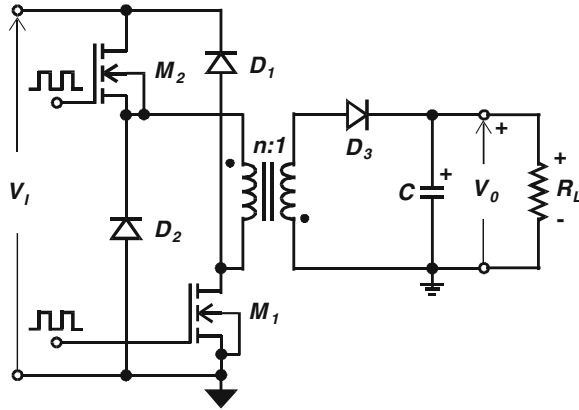


Fig. 4.44 Flyback converter using two transistors (half-bridge converter)

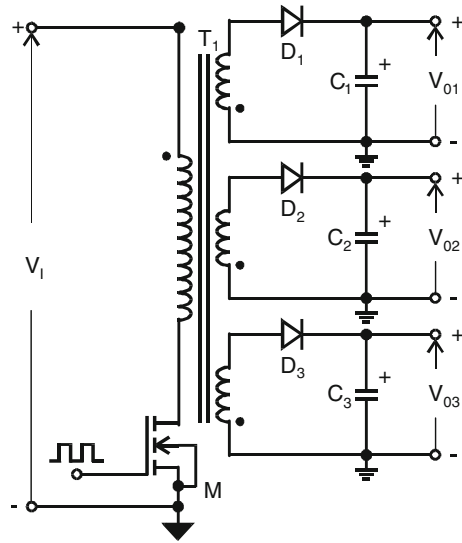


The output of the flyback converter can be multiplied easily (Fig. 4.45). The core of the transformer is common. For each additional output a secondary winding, a diode and a capacitor are required. In doing so, it is possible to realize positive or negative outputs. A negative output is obtained by the inverse winding of the secondary and by inverting the diode.

The favorable properties of the flyback converters are:

- simplicity and low cost,
- insensitivity to shorting the output, and
- easy multiplication of the output.

Fig. 4.45 Three-output flyback converter



The shortcomings are:

- drain current of the transistor is quite high,
- high stray inductance,
- the need for high power transformers in order to avoid core saturation (the cores with an air gap are used), and
- at high output current a large capacitor is required for filtering the output voltage.

Example 4.7 The indirect (flyback) converter in Fig. 4.41 has $V_I = 24$ V, $n = 3$, $L_m = 1$ mH, $R_L = 5$ Ω , $C = 100$ mF, $f = 50$ kHz and $V_o = 5$ V (semiconductor components can be considered ideal).

- Calculate the duty ratio D in the continuous working mode.
 - Calculate currents at the transistor and the diode.
 - Derive an expression for V_O/V_I in the discontinuous working mode.
 - Draw the waveforms of voltages and currents at the transistor and the diode for the continuous and the discontinuous mode.
- (a) Magnetization is done from the primary side of the transformer and demagnetization from the secondary side. A transformer with an air gap is used. Also, there are $v_S = v_P/n$ (always) and $i_d = ni_t$ (only during the transition

process), where i_d is the diode current and i_t is the transistor current. The average current of the magnetization inductance is equal to 0, so the following equations can be written (Fig. 4.46).

$$V_1 D T_S = n V_o (1 - D) T_S \Rightarrow \frac{V_o}{V_1} = \frac{D}{n(1 - D)} \Rightarrow D = 0.384.$$

$$I_i = \bar{i}_d = \frac{I_{d1} + I_{d0}}{2} (1 - D) = \frac{V_o}{R_L},$$

$$I_{d1} + I_{d0} = \frac{2V_o}{R_L(1 - D)}$$

$$I_{d1} - I_{d0} = \frac{V_o(1 - D) T_S n^2}{L_m}$$

$$(b) \quad \Rightarrow I_{d1} = \frac{V_o}{R_L(1 - D)} + \frac{n^2 V_o (1 - D) T_S}{2L_m} = 1.9 \text{ A analogously}$$

$$I_{d0} = \frac{V_o}{R_L(1 - D)} - \frac{n^2 V_o (1 - D) T_S}{2L_m} = 1.346 \text{ A.}$$

$$I_{t1} = \frac{V_o}{nR_L(1 - D)} + \frac{V_1 D T_S}{L_m} = 0.725 \text{ A}$$

$$I_{t0} = \frac{V_o}{nR_L(1 - D)} - \frac{V_1 D T_S}{L_m} = 0.357 \text{ A.}$$

(c) For the discontinuous mode the following equations can be written

$$V_1 D T_S = n V_o D_1 T_S \Rightarrow \frac{V_o}{V_1} = \frac{D}{n D_1}$$

$$I_o = \frac{V_o}{R_L} = \frac{I'_{d1} D_1}{2}, \quad D_1 = \frac{2V_o}{R_L I_{d1}};$$

$$I'_{d1} = n I'_{t1} = n \frac{V_1 D T_S}{L_m}$$

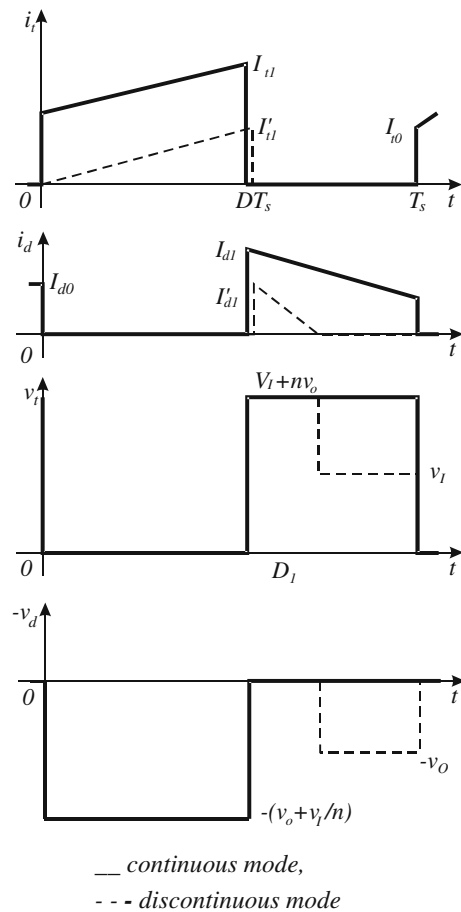
$$\Rightarrow D_1 = \frac{2V_o L_m}{n R_L V_1 D T_S}$$

$$\Rightarrow \frac{V_o^2}{V_1^2} = \frac{D^2 R_L T_S}{2L_m};$$

$$k = \frac{2L_m}{R_L T_S} \Rightarrow \frac{V_o}{V_1} = \frac{D}{\sqrt{k}} \Rightarrow V_o = \frac{V_1 D}{\sqrt{k}}.$$

(d) Fig. 4.46.

Fig. 4.46 Waveforms of voltages and currents at transistor and diode in continuous and discontinuous current mode for the converter from Fig. 4.41



4.5 Push–Pull (Symmetric) Converters

This converter belongs to the group of symmetric converters because, compared to the forward and flyback converters, it utilizes the magnetization curve of the transformer in both quadrants. Practically, a symmetric converter (Fig. 4.47) consists of two forward converters operating in push–pull, often called the counter-cycle converters. One of the converters consists of transistor T_{r1} and diode D_1 and the other of transistor T_{r2} and diode D_2 , including, of course, the corresponding transformer windings. One converter is active alternately to the other so that double power is obtained at the output compared to the basic forward converter. Namely, during one cycle of the control pulses the energy is transferred twice to the output choke L_o via the transformer. The energy accumulated in L_o is transferred to the load when both transistors are off, also twice within one cycle. Therefore, within one cycle a push–pull converter performs twice the action of the forward converter.

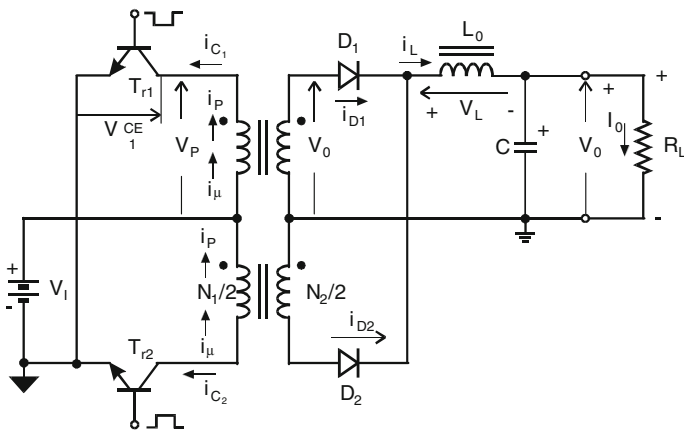


Fig. 4.47 Basic circuit of a push-pull converter

The transistors are controlled in such a way that they must not be on simultaneously in order to avoid short-circuiting of the transformer. Therefore, the duty cycle has to be

$$D = \frac{\tau}{T} < 0.5, \quad (4.178)$$

where τ is the interval of conduction of one of the transistors. For this reason the duty cycle for a half-cycle is often defined:

$$\delta = \frac{\tau}{T/2} = 2D. \quad (4.179)$$

Since the transistors T_{r1} and T_{r2} must not be on simultaneously, the maximum time of conduction is

$$\tau_{\max} = \frac{T}{2} - t_{\text{off}} = \frac{T}{2} - (t_s + t_f), \quad (4.180)$$

where t_{off} is the turn-off time, t_s is the storage time, and t_f is the falloff time of the collector current. Therefore

$$\delta < \frac{\tau_{\max}}{T/2} = 1 - \frac{t_{\text{off}}}{T/2}. \quad (4.181)$$

The difference

$$T_{\text{DT}} = \frac{T}{2} - \tau \quad (4.182)$$

is called the safety pause or the dead time and it denotes the interval when both transistors are off. The minimum dead time is $T_{DTmin} = t_{off}$.

The favorable property of the push–pull converter compared to the forward converter is that the transformer and the output filter are smaller, thus a higher output power is possible with the same type of transistor. The shortcomings are: there are more components in the basic circuit and the rectifier assemblies are more complex.

4.5.1 Analysis of Idealized Circuit in Continuous Mode

The continuous mode implies a mode where the current through the output choke is always greater than zero. In order to obtain the basic relations between voltages and currents, the idealized circuit of a push–pull converter will be analyzed first. This implies that:

- the transistors and the diodes are ideal switches (instantaneous switch-on and switch-off, short circuit when on, open circuit when off),
- the conduction times of transistors are equal ($\tau_1 = \tau_2$),
- the Ohmic resistances of the transformer and the choke are negligible (zero),
- the stray magnetic flux is negligible, and
- the load current I_o and the output voltage V_o are constant.

Figure 4.48 shows the waveforms of the characteristic voltages and currents in the idealized circuit. Depending on the levels of transistor currents one cycle consists of four different intervals.

4.5.1.1 I Interval

This interval starts at $t = 0$ and ends at $t = t_1$. At the beginning of the interval ($t = 0$) the transistor T_{r1} is turned off so that both transistors are off. The equivalent circuit during this interval is shown in Fig. 4.49a. The primary circuit is open. Since there are no variations of the magnetic flux, the secondary voltage is zero.

Both diodes are on and they close the circuit for the current through the choke. If the resistances of the diodes D_1 and D_2 are equal, each of them takes one half of the choke current. The current I_s which maintains the magnetic flux accomplished previously by the magnetization current, $I_{\mu m}$, also flows through the diodes D_1 and D_2 . Until the primary circuit is open (the transistors are off) this current cannot flow. Because only T_{r1} was open previously, it follows that

$$\frac{N_1}{2} i_p = -\frac{N_2}{2} I_s - \frac{N_2}{2} I_s + \frac{N_1}{2} I_{\mu m} + \frac{N_2}{2} \frac{I_L}{2} - \frac{N_2}{2} \frac{i_L}{2}. \quad (4.183)$$

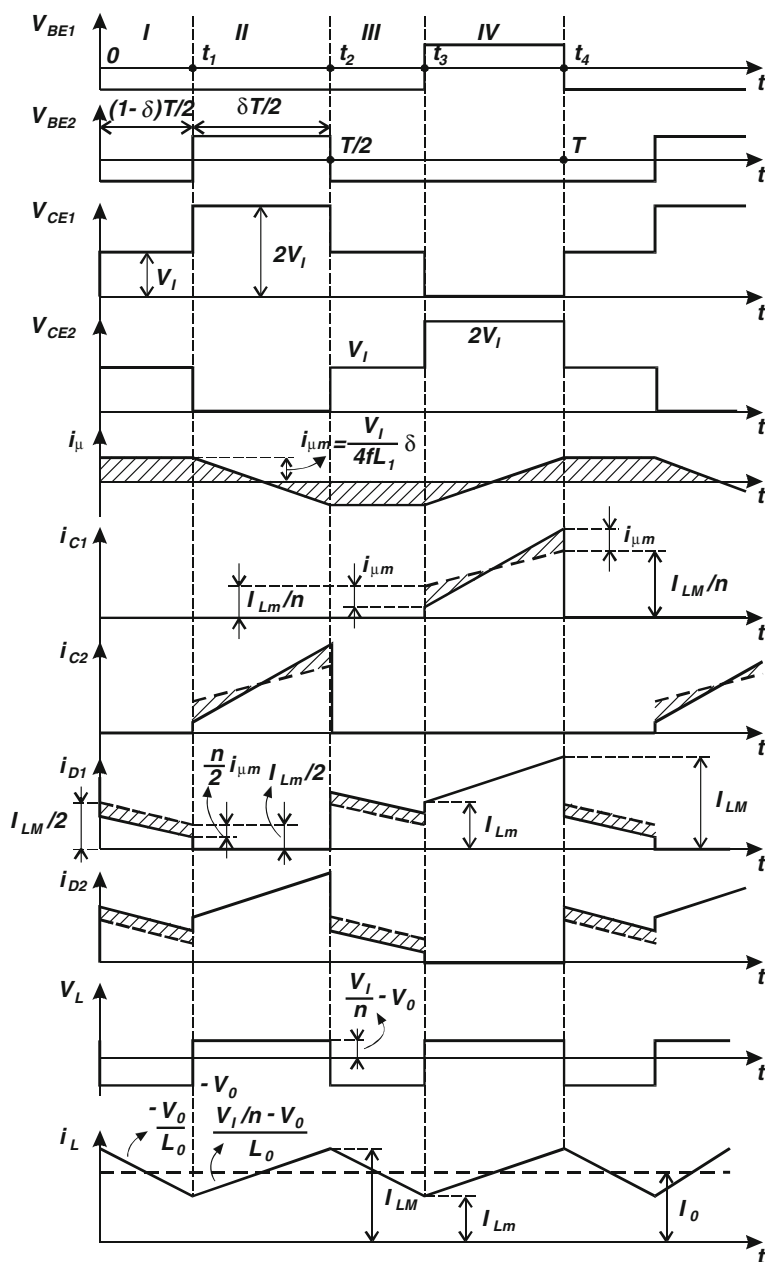


Fig. 4.48 Current and voltage waveforms of the idealized circuit in the continuous operating mode

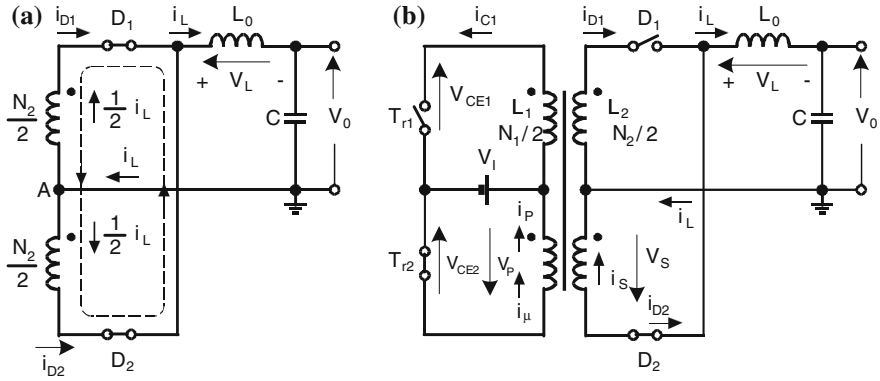


Fig. 4.49 Equivalent circuit in the I interval (a) and in the II interval (b) with the indicated directions of the voltages and currents

Since $i_p = 0$, the secondary equivalent of the magnetization current is determined by

$$I_s = \frac{1}{2} n I_{\mu m}, \quad (4.184)$$

where

$$n = \frac{N_1/2}{N_2/2}.$$

This current flows through the diode D_1 in the reverse direction. This is possible because one half of the choke current flows through D_1 in the forward direction. In order to have positive total current, one half of the minimum choke current has to be

$$\frac{I_{Lm}}{2} > I_s. \quad (4.185)$$

This is, at the same time, the condition of continuity.

Since the secondary voltage is zero and the voltages across diodes are negligible, the voltage across the choke is $V_L = -V_o = \text{const}$. The current through the choke is thus linear and is represented by

$$i_L(t) = I_{LM} - \frac{V_o}{L_0} t, \quad 0 \leq t \leq t_1, \quad (4.186)$$

where I_{LM} is the maximum current through the choke. The currents through the diodes D_1 and D_2 are, thus, determined by:

$$\begin{aligned} i_{D1} &= \frac{1}{2}i_L - I_s = \frac{1}{2}\left(I_{LM} - nI_{\mu m} - \frac{V_o}{L_0}t\right), \\ i_{D2} &= \frac{1}{2}i_L + I_s = \frac{1}{2}\left(I_{LM} + nI_{\mu m} - \frac{V_o}{L_0}t\right). \end{aligned} \quad (4.187)$$

The collector–emitter voltages of the transistors are equal to the input voltage, i.e.,

$$V_{CE1} = V_{CE2} = V_I. \quad (4.188)$$

4.5.1.2 II Interval

In the II interval ($t_1 \leq t \leq t_2$) the transistor T_{r2} is on and T_{r1} is off ($V_{CE2} = 0$, $i_{C1} = 0$). The diode D_1 is off and D_2 is on (Fig. 4.49b). Since the secondary circuit containing the diode D_1 is open, then:

$$\begin{aligned} \frac{N_1}{2}i_p &= \frac{N_1}{2}i_\mu + \frac{N_2}{2}i_s, \\ V_o + V_p - V_{CE2} &= 0. \end{aligned} \quad (4.189)$$

From (4.189) one obtains

$$i_{C2} = -i_\mu + \frac{i_L}{n} \quad \text{and} \quad V_p = -V_o, \quad (4.190)$$

because $V_{CE2} = 0$, $i_p = -i_{C2}$, and $i_s = -i_L$. Since the primary voltage is constant, from $V_p = L_1 di_\mu/dt$ it follows that the magnetization current is

$$i_\mu = I_{\mu m} - \frac{V_I}{L_I}(t - t_1). \quad (4.191)$$

The voltage across the choke is

$$V_L = -V_s - V_o. \quad (4.192)$$

In additions, $V_p/V_s = n$, so

$$V_L = \frac{V_I}{n} - V_o. \quad (4.193)$$

Because $V_L = \text{const.}$, the current through the choke is linear determined by

$$i_L = I_{Lm} + \frac{\frac{V_I}{n} - V_o}{L_0}(t - t_1). \quad (4.194)$$

Since D_1 is off ($i_{D1} = 0$), $i_{D2} = i$. The collector–emitter voltage of the nonconducting transistor (T_{r1}) is

$$V_{CE1} = V_I - V_p = 2V_I, \quad (4.195)$$

and the collector current of the conducting transistor (T_{r2})

$$i_{C2} = -I_{\mu m} + \frac{V_1}{L_1}(t - t_1) + \frac{1}{n} \left[\frac{V_1 - V_0}{L_0}(t - t_1) + I_{Lm} \right]. \quad (4.196)$$

4.5.1.3 III Interval

In this interval both transistors are off again, but this time at the beginning of the interval T_{r2} switches from the conducting to the nonconducting state. The equivalent circuit (Fig. 4.50) is the same as for interval I. The accumulated magnetic energy in the choke L_o is now transferred to the load. By an analysis analogous of the I interval, one obtains the following relations

$$\begin{aligned} I_s &= \frac{n}{2} I_{\text{lim}}, \\ V_L &= -V_o, V_{\text{CE1}} = V_{\text{CE2}} = V_1, \\ i_L(t) &= I_{\text{LM}} - \frac{V_o}{L_0}(t - t_2). \end{aligned} \quad (4.197)$$

Now the secondary equivalent of the magnetization current flows through the diode D_2 in the reverse direction. The currents through D_1 and D_2 are

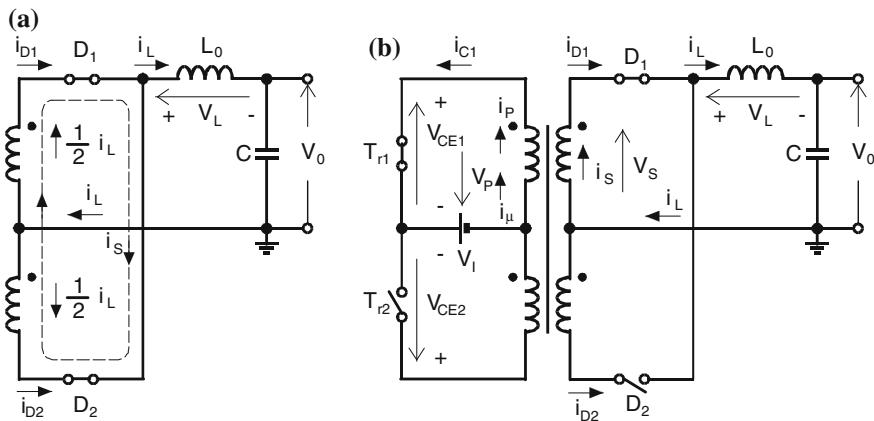


Fig. 4.50 Equivalent circuit in the III interval (a) and in the IV interval (b)

$$\begin{aligned} i_{D1} &= \frac{1}{2}i_L + I_s = \frac{1}{2} \left[I_{LM} + nI_{\mu m} - \frac{V_o}{L_0}(t - t_2) \right], \\ i_{D2} &= \frac{1}{2}i_L + I_s = \frac{1}{2} \left[I_{LM} - nI_{\mu m} - \frac{V_o}{L_0}(t - t_2) \right]. \end{aligned} \quad (4.198)$$

4.5.1.4 IV Interval

The situation in this interval is presented in Fig. 4.50b. The equivalent circuit is similar to the one of the II interval (Fig. 4.49b) except that the states of the transistors and diodes are reversed (T_{r1} and D_1 are conducting, T_{r2} and D_2 are off). Therefore, the analysis can be carried out analogously to the one carried out for the II interval. The primary voltage has changed the polarity ($V_p = V_1$) because $V_{CE1} = 0 = V_1 - V_p$. The magnetization current is now

$$i_{\mu} = -I_{\mu m} + \frac{V_1}{L_1}(t - t_3), \quad (4.199)$$

and the currents through the choke, the diode D_1 , and the transistor T_{r1} are

$$\begin{aligned} i_L &= i_{D1} = I_{Lm} + \frac{\frac{V_1}{n} + V_o}{L_0}(t - t_3), \\ i_{C1} &= -I_{\mu m} + \frac{V_1}{L_1}(t - t_3) + \frac{1}{n} \left[I_{Lm} + \frac{\frac{V_1}{n} - V_o}{L_0}(t - t_3) \right]. \end{aligned} \quad (4.200)$$

The characteristic voltages are

$$V_{CE2} = 2V_1, \quad V_s = \frac{V_1}{n}, \quad V_L = \frac{V_1}{n} - V_o. \quad (4.201)$$

The maximum magnetization current $I_{\mu m}$ can be obtained by introducing in (4.199) $i_{\mu}(t_4) = I_{\mu m}$ or in (4.191) $i_{\mu}(t_2) = I_{\mu m}$. If it is assumed that the conduction times of the transistors T_{r1} and T_{r2} are equal, i.e.,

$$t_4 - t_3 = t_2 - t_1 = \delta \frac{T}{2}, \quad (4.202)$$

it turns out that

$$I_{\mu m} = \frac{V_1 \delta \frac{T}{2}}{2L_1} = \frac{V_1 \delta}{4L_1 f}. \quad (4.203)$$

Finally, it may be stressed again that during the intervals $t_2 - t_1$ and $t_4 - t_3$ the energy directly transferred to the load via the transformer. At the same time

magnetic energy is accumulated in the output choke, L_o , which is transferred to the load during intervals $t_1 - 0$ and $t_3 - t_2$ when both transistors are off.

By equating the positive (I and III intervals) and negative (II and IV intervals) changes of the current through the output choke, one obtains

$$\frac{V_o}{L_o} t_2 = \frac{V_o}{L_o} (t_3 - t_2) = \frac{\frac{V_1}{n} - V_o}{L_o} (t_2 - t_1) = \frac{\frac{V_1}{n} - V_o}{L_o} (t_4 - t_3). \quad (4.204)$$

Taking into account (4.201) and $t_3 - t_2 = (1 - \delta)(T/2)$, from (4.204), after rearrangement, it follows

$$V_o = \delta \frac{V_1}{n} = 2D \frac{V_1}{n}. \quad (4.205)$$

Consequently, the output voltage does not depend on the load current, but only on the duty cycle.

The load current is equal to the average value of the current through the choke, i.e.,

$$I_o = \frac{1}{T} \int_0^T i_L dt = 2 \left[\frac{1}{T} \int_0^{(1-\delta)T/2} \left(I_{LM} - \frac{V_o}{L_o} t \right) dt + \frac{1}{T} \int_0^{\delta T/2} \left(I_{Lm} + \frac{\frac{V_1}{n} - V_o}{L_o} t \right) dt \right], \quad (4.206)$$

therefore it follows that

$$I_o = \frac{1}{2} (I_{LM} + I_{Lm}). \quad (4.207)$$

The variation of the current through the choke is determined by

$$\Delta i_L = I_{LM} - I_{Lm} = \frac{\frac{V_1}{n} - V_o}{L_o} \delta \frac{T}{2}. \quad (4.208)$$

From (4.207), (4.208), and (4.205) it follows that the maximum and the minimum current through the choke, as functions of the load current and the duty cycle, are given by

$$\begin{aligned} I_{LM} &= I_o + \frac{1}{2} \Delta i_L = I_o + \frac{V_1}{4nL_o f} \delta (1 - \delta), \\ I_{Lm} &= I_o - \frac{1}{2} \Delta i_L = I_o - \frac{V_1}{4nL_o f} \delta (1 - \delta). \end{aligned} \quad (4.209)$$

The ripple of the output voltage is determined by the variation of the voltage across the capacitor C of the output filter which can be expressed as

$$v_c(t) = \frac{1}{C} \int_0^t i_c(t) dt, \quad (4.210)$$

where

$$i_c(t) = i_L(t) - I_O. \quad (4.211)$$

In interval I, when both transistors are off, from (4.186), (4.207), (4.208), and (4.202) it follows

$$i_c(t) = \frac{\Delta i_L}{2} - \frac{2\Delta i_L}{(1-\delta)T}t; \quad t \in \left[0, (1-\delta)\frac{T}{2}\right]. \quad (4.212)$$

From (4.210) and (4.211) it turns out that the variation of the voltage across the capacitor during interval I is

$$v_c(t) = \frac{\Delta i_L}{2C}t - \frac{\Delta i_L}{C(1-\delta)T}t^2. \quad (4.213)$$

The current and the voltage during interval II are determined by

$$i_c(t) = -\frac{\Delta i_L}{2} + \frac{2\Delta i_L}{\delta T}t, \quad (4.214)$$

$$v_c(t) = -\frac{\Delta i_L}{2C}t + \frac{2\Delta i_L}{C\delta T}t^2, \quad t \in \left[0, \delta\frac{T}{2}\right]. \quad (4.215)$$

The variations of $i_c(t)$ and $v_c(t)$ during intervals I and II ($0 \leq t \leq T/2$) are shown in Fig. 4.51. In intervals III and IV ($T/2 \leq t \leq T$) they repeat periodically. The maximum and the minimum voltages across the capacitor occur at the instants when the first derivatives of (4.213) and (4.214) are equal to zero.

Upon rearrangement, it follows

$$V_{Cmax} = \frac{\Delta i_L T}{16C} (1-\delta), \quad (4.216)$$

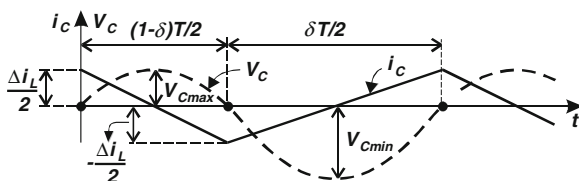


Fig. 4.51 Voltage and current waveforms of the output capacitor

$$v_{Cmin} = -\frac{\Delta i_L T}{16C} \delta. \quad (4.217)$$

Therefore, on the basis of (4.216), (4.217), (4.208), and (4.205) the peak-to-peak variation of the output voltage $\Delta V_o = \Delta V_c = V_{Cmax} - V_{Cmin}$ is given by

$$\Delta V_o = \frac{V_i}{n} \frac{(1 - \delta)\delta}{32L_0 f^2 C}. \quad (4.218)$$

4.5.2 Output Characteristics

The normalized output characteristics of the push–pull converter are shown in Fig. 4.52. The normalized output voltage and current are respectively given by

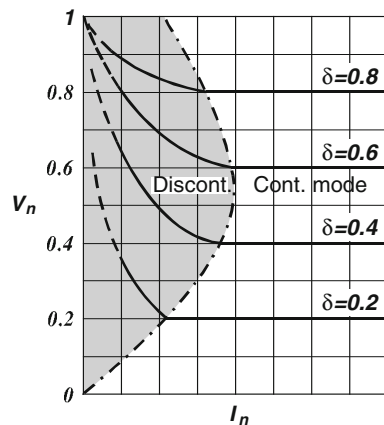
$$V_n = \frac{nV_o}{V_i} = \delta, \quad (4.219)$$

$$I_n = \frac{4nL_0}{V_i T} I_0. \quad (4.220)$$

It can be shown that the hyperbola denoting the boundary between the continuous and the discontinuous mode is

$$I_n = V_n \left(1 + \frac{L_0}{L_2} \right) - V_n^2. \quad (4.221)$$

Fig. 4.52 Normalized output characteristics of idealized push–pull converter



To the left of the hyperbola is the discontinuous mode where the output voltage is a function of the load current. In this mode the current through the choke during one cycle is zero at two subintervals. The discontinuous mode should be avoided due to the instability of the output voltage. In order to avoid the break of the current through the choke, the minimum load current has to be

$$I_{\text{omin}} > \frac{\Delta i_L}{2}. \quad (4.222)$$

From (4.221) and (4.208) the continuous operating mode condition is

$$L_o > \frac{(1 - \delta)}{2f_{\text{omin}}} V_o. \quad (4.223)$$

The output characteristics are influenced by some realistic parameters not considered in the idealized circuit. These are, first of all, the stray flux of the transformer, the reverse conduction of the diode, and the output resistance of the converter. For instance, at the turn-on of the transistor T_{r2} , the commutation of the current from the diode D_1 to the diode D_2 is not instantaneous because of the existence of stray inductances whose resistance to the change of the magnetic flux has to be overcome. The same process occurs at the turn-on of T_{r1} ($t = t_3$ in Fig. 4.49) when the commutation of the current from D_2 to D_1 takes place. Figure 4.53a shows a simplified equivalent circuit immediately after the transistor T_{r2} is turned on. The current i_2 has

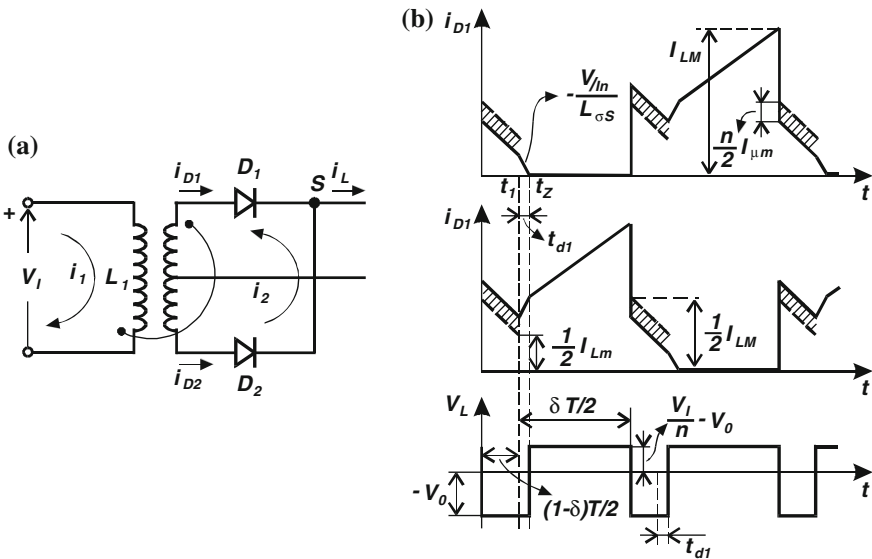


Fig. 4.53 Equivalent circuit during commutation of current from D_1 to D_2 (a) and real variations of currents i_{D1} and i_{D2} (b)

such a direction that the current through D_1 reduces and through D_2 increases. The commutation is ended when i_{D1} drops to zero (Fig. 4.53b). Then the circuit is in the state described in interval II. By assuming that during t_{d1} the variations of the choke current $i_L = I_{Lm}$ and the magnetization current are negligible, it can be shown that the commutation time is

$$t_{D1} \approx \frac{I_{Lm} - nI_{\mu m}}{2V_1} nL_{os}, \quad (4.224)$$

where L_{os} is the total stray inductance of the secondary. The time during which the secondary voltage is zero and the choke voltage is $-V_o$, is extended by t_{d1} (Fig. 4.53b). The same process occurs immediately upon the switch-on of the transistor T_{r1} . Now the commutation time is determined by the time required for the current through D_2 to drop to zero.

Practically the interval of energy accumulation by the choke L_o is shortened by t_{d1} . This means that the output voltage decreases. This is obtained from (4.204) when t_2 is increased and $t_2 - t_1 = t_4 - t_3$ decreased by t_{d1} , i.e.,

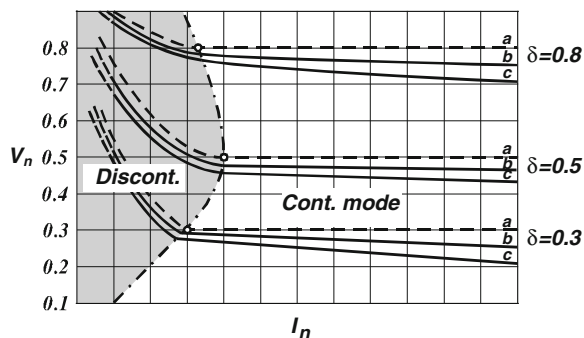
$$\left[(1 - \delta) \frac{T}{2} + t_{d1} \right] V_o = \left(\delta \frac{T}{2} - t_{d1} \right) \left(\frac{V_1}{n} - V_o \right). \quad (4.225)$$

From (4.225) it follows

$$V_o = \delta \left(1 - \frac{2t_{d1}}{T} \right) \frac{V_1}{n}. \quad (4.226)$$

Because t_{d1} is load current dependent, since $I_{Lm} = f(I_o)$ (4.209), the output voltage is also load current dependent even in the continuous mode (Fig. 4.54). The reduction of the output voltage increases with an increase of the stray inductance. It is very important to take care that the quality of the transformer is good so that the stray inductance is as small as possible.

Fig. 4.54 Normalized output characteristics versus stray inductance: *a* $L_{os} = 0$, *b* L_{os1} , *c* L_{os2} ($L_{os1} < L_{os2}$)



The output characteristics are also affected by the output resistance of the converter. With respect to the output terminals a converter can be represented by a voltage source V_{oo} and its internal resistance R_o . Then

$$V_o = \frac{V_{oo}}{1 + \frac{R_1}{R_2}} = V_{oo} - R_o I_O, \quad (4.227)$$

where R_o is the output resistance of the converter and $V_{oo} = V_o$ for $R_o = 0$. Increasing the load current increases the losses in R_o which reduces the output voltage across the load. By combining (4.226) and (4.227) it turns out that the output voltage is

$$V_o = \delta \left(1 - 2 \frac{t_{di}}{T} \right) \frac{V_1}{n} - R_o I_O. \quad (4.228)$$

The final qualitative form of the output characteristics is achieved when the slope due to the stray inductance, shown in Fig. 4.54, is increased by the corresponding slope due to the output resistance.

4.5.3 Selection of Components

Transistors and diodes. The basic requirements are related to the maximum current or power, breakdown voltage, and dynamic characteristics (turn-on and turn-off times). In general, transistors and diodes with minimal turn-on and turn-off times should be selected. The maximum collector-emitter voltage is $2V_1$, so the breakdown voltage of the transistor should be

$$BV_{CB0} > (1.2-1.5)2V_{1\max}, \quad (4.229)$$

where $V_{1\max}$ is the maximum value of the input voltage and (1.2–1.5) is the safety factor. The maximum permitted collector current (catalog data) has to be

$$I_{cd} > 1.5I_{c\max} \quad (4.230)$$

where $I_{c\max}$ is the maximum collector current in the circuit and 1.5 is the safety factor. $I_{c\max}$ is determined according to the maximum load. Then $\Delta i_L \ll I_O$, so it may be assumed that $I_{LM} \approx I_{Lm} \approx I_O$, and

$$I_{c\max} \approx \frac{I_O}{n}. \quad (4.231)$$

The worst case is that the conducting transistor is in saturation, i.e.,

$$I_B > \frac{I_{C\max}}{\beta_{\min}}, \quad (4.232)$$

where $\beta_{\min}$ is the minimum common emitter current gain of the transistor. Usually the minimum saturation factor is (1.2–1.5), so

$$I_B = (1.2 - 1.5) \frac{I_O}{n\beta_{\min}}. \quad (4.233)$$

In order to keep the base current as low as possible (lower losses in the control circuit), a high $\beta_{\min}$ transistor should be selected. For power transistors it is standard that $\beta_{\min}$ is several tens.

The maximum current through the diode is equal to the maximum current through the choke (4.209). Since at maximum load the variation of the current through the choke can be neglected, the maximum permitted diode current has to be

$$I_{Dd} > (1.2-1.5)I_O. \quad (4.234)$$

The maximum reverse voltage across the diode occurs during intervals II and IV. Then

$$V_{DR} = V_L + V_o + \frac{V_{I\max}}{n}. \quad (4.235)$$

The voltage across the choke V_L is given by (4.193), so

$$V_{DR} = 2 \frac{V_{I\max}}{n}. \quad (4.236)$$

If a safety factor of at least 1.3 is taken, the breakdown voltage of the diodes has to be

$$BV_D > 1.3V_{DR}. \quad (4.237)$$

Owing to the smallest storage time during the turn-off process, Schottky diodes are recommendable.

Control module frequency. In order to avoid short-circuiting of the transformer during transients, control of the push–pull converters is carried out in two shifted phases. This shift in terms of time is a safety pause, often called “dead time”. The half-cycle of the control pulses has to be

$$\frac{T}{2} > \tau_{\max} + T_{DT\min}, \quad (4.238)$$

where $T_{D\min} = t_{\text{off}} = t_s + t_f$ is the minimum dead time and:

$$\tau_{\max} = \delta_{\max} \frac{T}{2} = n \frac{V_o}{V_{\min}} \frac{T}{2} \quad (4.239)$$

is the maximum conduction time of the transistor. From (4.238) and (4.239) one obtains

$$T > \frac{2T_{\text{DTmin}}}{1 - n \frac{V_o}{V_{\min}}}. \quad (4.240)$$

Compared to the characteristics of a selected transistor, the minimum cycle should be approximately ten times longer than the maximum sum of the turn-on and turn-off times. Usually the frequency of the control pulses is several tens of kHz.

Output filter. The value of the capacitor C is determined on the basis of the required peak-to-peak variation of the output voltage, V_{pp} , i.e.,

$$\Delta V_o < V_{\text{pp}}. \quad (4.241)$$

From (4.241) and (4.218) it follows that

$$C > \frac{\delta(1 - \delta)}{32L_o f^2} \frac{V_I}{nV_{\text{pp}}}. \quad (4.242)$$

On the other hand, the capacitor has to be selected to withstand the rms current:

$$I_{\text{ceff}} = \sqrt{\frac{2}{T} \int_0^{T/2} i_c^2(t) dt}, \quad (4.243)$$

where $i_c(t)$ is the current through the capacitor determined by (4.212) and (4.214). Upon rearrangement one obtains

$$I_{\text{ceff}} = \frac{\delta(1 - \delta)}{4\sqrt{3}L_o f} \frac{V_I}{n}. \quad (4.244)$$

The maximum voltage across the capacitor has to be higher than the maximum possible output voltage V_I/n obtainable for $\delta = 1$. The capacitor should be of the high frequency type having as low series resistance as possible.

The inductance of the output choke is usually determined from the condition that the variation of the current through the choke should be much smaller than the maximum load current, i.e.,

$$\Delta i_L = \frac{\delta(1 - \delta)}{2L_o f_o} \frac{V_I}{n} < 0.1I_o. \quad (4.245)$$

Therefore

$$L_o > 5 \frac{\delta(1-\delta)}{L_o f_0} \frac{V_{\text{Imax}}}{n}. \quad (4.246)$$

When condition (4.242) is fulfilled, further calculation is the same as for a DC choke. The number of turns is determined by

$$N = \sqrt{\frac{L_o I_{\text{ef}} H}{A_{\text{ef}} B}}, \quad (4.247)$$

where B and H are the selected magnetic induction and magnetic field, respectively, A_{ef} is the effective cross section of the core, and I_{ef} is the average length of the magnetic line. The air gap is approximately determined by

$$I_v = \mu_0 \frac{N^2 A_{\text{ef}}}{L_o}, \quad (4.248)$$

where $\mu_0 = 4 \times 10^{-7}$ [H/m] is the magnetic permeability of vacuum.

The cross section of the copper wire is determined by

$$S_{\text{cu}} = \frac{A_w F_w}{N} = \frac{d^2 \pi}{4}, \quad (4.249)$$

where A_w is the core opening area, F_w is the filling factor (catalog data for the selected core).

In order that the converter operates in the continuous mode, the output is loaded by a zero (intrinsic) load. The resistance of this load is determined from (4.223) when $I_{\text{Omin}} = V_o / R_{\text{Lmax}}$

$$R_{\text{Lmax}} < \frac{2fL_o}{1-\delta}. \quad (4.250)$$

Transformer. The transformer is of the high frequency type. Typical operating frequencies are from several tens of kHz to 100 kHz. The basic requirements as regards the selection of the core are low losses, small dimensions, and the ability of transferring the maximum power. With the geometric characteristics A_w , A_{ef} , and F_w of the selected core, the maximum power that can be transferred to the load is determined by

$$P_{\text{omax}} \leq \sqrt{2} f J B A_w A_{\text{fe}} F_w, \quad (4.251)$$

where J is the current density in the conductor. The flux change in the primary winding is proportional to the input voltage. Namely

$$V_1 = \frac{N_p}{2} \frac{d\Phi}{dt} = \frac{N_1}{2} \frac{2BA_{ef}}{\delta T/2}. \quad (4.252)$$

The number of turns of the primary (assuming the worst case $V_{I\max}$, $\delta_{\max} = 1$) is

$$\frac{N_1}{2} = \frac{V_{I\max}}{4A_{ef}Bf}. \quad (4.253)$$

The number of turns of the secondary is

$$\frac{N_2}{2} = \frac{N_1/2}{n}. \quad (4.254)$$

The transformation ratio, n , depends on the ratio of the input and the output voltage (4.205). As high as possible n is recommended in order to keep the transistor current low. However, according to (4.179), there is a limit because of the limitation on δ . Usually $0.2 \leq \delta \leq 0.9$. The filling factor δ , within permitted limits, varies with the variation of the input voltage $V_{I\min} \leq V_I \leq V_{I\max}$. If the average value of δ is used, i.e.,

$$\delta_s = \frac{\delta_{\min} + \delta_{\max}}{2}$$

one obtains

$$n = 2\delta_s \frac{V_{I\max}}{V_o} \frac{1}{1 + V_{I\max}/V_{I\min}}. \quad (4.255)$$

The cross section of the conductor is determined by

$$S_{cu} = \frac{I_{rms}}{J}, \quad (4.256)$$

where I_{rms} is the rms value of the current through the conductor. In the primary winding this current is equal to the rms value of the transistor current, i.e.,

$$I_{rmsp} = I_{rmst} = \sqrt{\frac{1}{T} \int_0^T i_c^2(t) dt}, \quad (4.257)$$

where i_c is the collector current of one transistor. In the worst case, when the load current is maximum, the variations of the current through the choke are negligible.

Then, during $\tau = \delta T/2$, while the transistor is on, the collector current is approximately constant $i_c \approx I_{\text{omax}}/n$. Therefore

$$I_{\text{rmsp}} = \sqrt{\frac{1}{T} \int_0^{\delta T/2} \frac{I_{\text{omax}}^2}{n^2} dt} = \frac{I_{\text{omax}}}{n} \sqrt{\frac{\delta}{2}}. \quad (4.258)$$

In (4.258) it should be assumed that $\delta = \delta_{\text{max}}$. On the basis of (4.257) and (4.258) the diameter of the primary conductor is calculated as

$$d_p = 2 \sqrt{\frac{I_{\text{omax}}}{nJ\pi} \sqrt{\frac{\delta_{\text{max}}}{2}}}. \quad (4.259)$$

The rms value of the secondary current is equal to the rms value of the current through the diode. By assuming, like in the case of the transistor, that the load current is maximum, the variation of the current through the diode is shown in Fig. 4.55.

From $I_{\text{rmss}} = I_{\text{rmsD}} = \sqrt{\frac{1}{T} \int_0^T i_D^2 dt}$ and Fig. 4.55 one obtains that

$$I_{\text{rmss}} = \frac{\sqrt{1+\delta}}{2} I_{\text{omax}}. \quad (4.260)$$

Therefore

$$d_s = 2 \sqrt{\frac{\sqrt{1+\delta_{\text{max}}}}{2\pi J} I_{\text{omax}}}. \quad (4.261)$$

While winding up the transformer care should be taken that the stray magnetic flux remains as low as possible. For this reason the height of the winding should be as small as possible, and the width of the winding as large as possible. The distance between one pair of half-windings primary–secondary has to be as small as possible. Since in one half-cycle the current flows through the half-windings I and III and in the other half-cycle through the half-windings II and IV, the manner of arranging the windings is shown in Fig. 4.56.

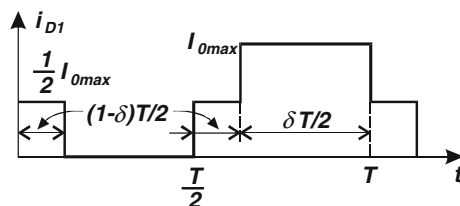


Fig. 4.55 Variation of the current through the diode D_1 at maximum load current when $D_i L \ll I_o$

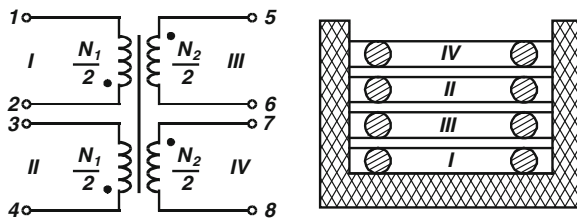


Fig. 4.56 The manner of winding up the transformer

The inductances of the primary winding, L_1 , and of the secondary winding, L_2 , are expressed by

$$L_1 = \mu_o \mu_a \left(\frac{N_p}{2} \right)^2 \frac{1}{C_j}, \quad L_2 = \frac{L_1}{n^2}, \quad (4.262)$$

where μ_o is the relative permeability of the core and C_c [1/mm] is constant of the transformer core.

Example 4.8 The push–pull converter shown in Fig. 4.47 has $V_1 = 24$ V, $n = N_1/N_2 = 1.5$, $D = 0.2$, $L_0 = 100$ μ H, $R_L = 5$ Ω , $C = 1$ mF and $f = 25$ kHz (semiconductor components can be consider ideal). The magnetization inductance of the transformer L_m is equal to 1 mH.

- Determine the output voltage V_o versus duty ratio D in continuous working mode.
- Determine the minimum and maximum current of the inductor L_0 .
- Determine currents at the transistor.
- Draw waveforms of voltages and currents at the transistor and the diode for continuous working mode.

- The output voltage V_o can be calculated from the Eq. (4.205)

$$V_o = \frac{2V_1 D}{n} = 6.4 \text{ V}.$$

- The average current of the inductor L is equal to

$$I_O = \frac{V_O}{R_L} = \bar{i}_L = \frac{I_{L1} + I_{L0}}{2} = 1.28 \text{ A. The maximum and the minimum current of the inductor } L \text{ can be calculated from (4.209) (Fig. 4.57)}$$

$$I_{LM} = I_O + \frac{\Delta i_L}{2} = I_O + \frac{\frac{V_1}{n} - V_o}{L_0} \delta \frac{T}{2} = 2.05 \text{ A},$$

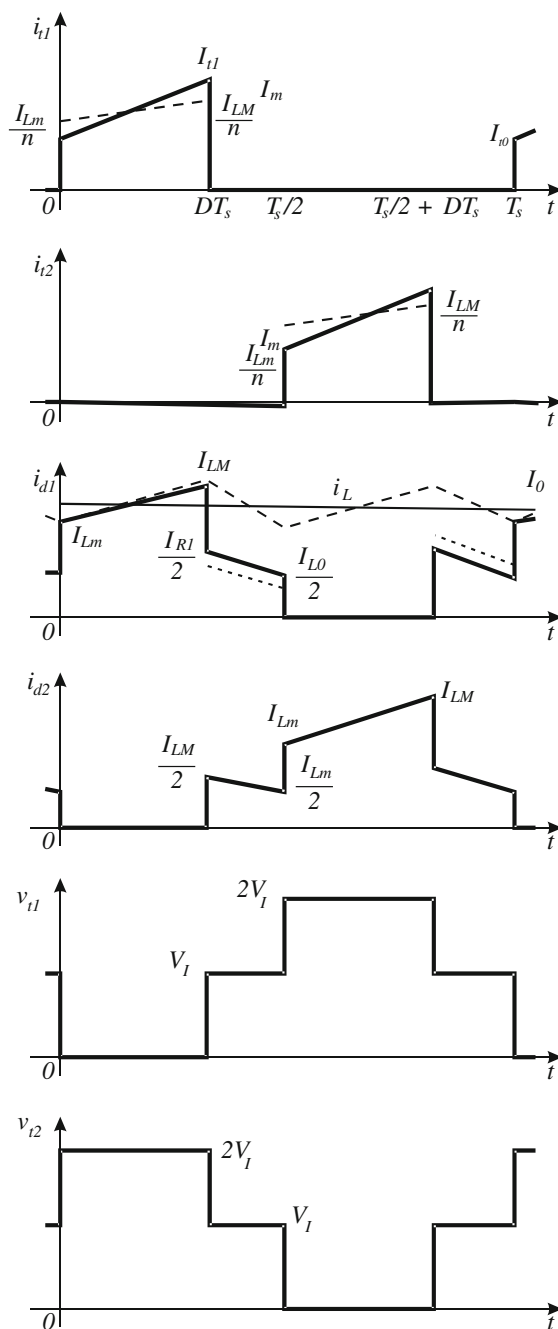
$$I_{LM} = I_O - \frac{\Delta i_L}{2} = I_O - \frac{\frac{V_1}{n} - V_o}{L_0} \delta \frac{T}{2} = 0.51 \text{ A}.$$

$$I_{t1} = \frac{I_{LM}}{n} + I_m = 1.26 \text{ A},$$

- $$I_{t0} = \frac{I_{LM}}{n} - I_m = 0.41 \text{ A}, \quad 2I_m = \frac{V_1 D T_S}{L_m} = 0.192 \text{ A}.$$

- See Fig. 4.57.

Fig. 4.57 Waveforms of voltages and currents at transistor and diode for the converter from Fig. 4.47



4.5.4 DC Premagnetization of the Core

DC premagnetization or asymmetric magnetization of the core is introduced because of:

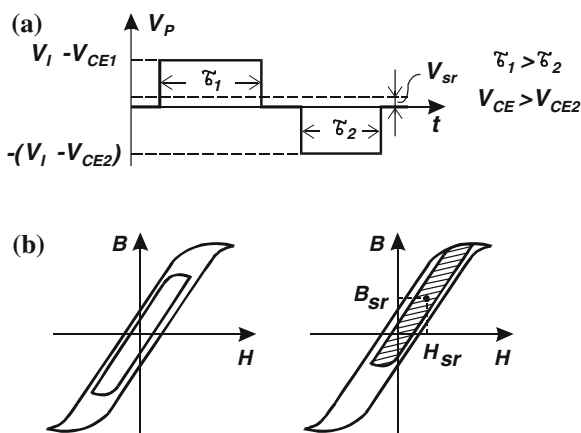
- unequal voltage drops on the conducting transistors,
- unequal conduction times of the transistors caused by the difference in the dynamic characteristics (times t_s and t_f) or by asymmetry of the base driving circuits, and
- imperfect manufacture of the transformer or unequal number of turns of some of the windings.

The third cause can be avoided by careful manufacturing procedure, but not the first two. Namely, the discrepancies in characteristics (parameter spread) from one transistor to another are inevitable and can be quite noticeable. Besides, these discrepancies are random and they are a consequence of the nature of the technological process itself so they can not be exactly calculated in advance. A consequence of the quoted phenomena is different length of pulses in the transformer primary (Fig. 4.58). This leads to the appearance of a DC component V_{av} which causes a DC premagnetization current to flow through the primary winding.

$$I_{av} = \frac{V_{av}}{r_p}. \quad (4.263)$$

Owing to the small Ohmic resistance r_p of the primary, this current may be significant. This causes a shift of the operating point along the HB magnetization curve which may, followed by the same change of the magnetic flux, lead to the saturation of the core at one side (Fig. 4.56). When the core goes into saturation, the inductance of the transformer drops, and the currents of the primary and the transistor increase sharply. The appearance of large instantaneous values of transistor currents, unless a protection is provided, may lead to transistor destruction.

Fig. 4.58 Creation of the DC component of the primary (a) and the magnetization curves for symmetric (b) and asymmetric magnetization of the core (c)



The problem of the core saturation can be resolved by a drastic reduction of the maximum permitted induction in the transformer core or by an air gap in the core. This, however, reduces considerably the efficiency of the transformer, since only a small part of the hysteresis loop is used. By doing so one also loses the basic favorable feature of the push–pull converters compared to other types.

In principle, the asymmetry problem can be eliminated by the permanent control of the integral transformer voltage and correction of the times of transistor conduction. However, such solutions are very complex. In practice the problem of increasing transistor current due to asymmetry is quite successfully solved by insertion of capacitors in series with the transformer.

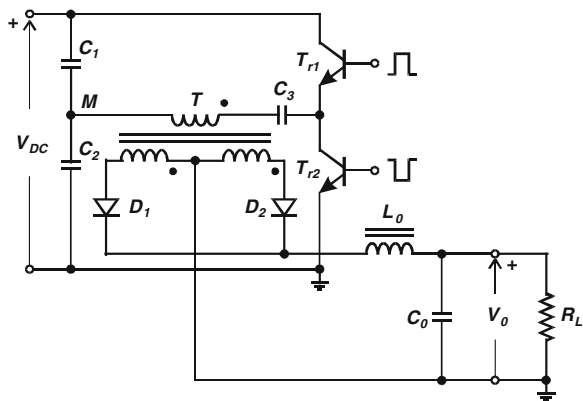
4.5.5 Half-Bridge Converter

The common point, M , of the half-bridge converter (Fig. 4.59) is between the capacitors $C_1 = C_2$ at a potential $V_I/2$. For this reason the transformer voltage varies between $-V_I/2$ and $V_I/2$ and the maximum collector–emitter voltage of the transistor is $V_{CEmax} = V_I$. Therefore, compared to the basic push–pull converter circuit the voltage load is halved.

The capacitor C_3 in series with the transformer primary eliminates the flow of DC current through the transformer. Owing to the alternate conduction of the transistors T_{r1} and T_{r2} the capacitor C_3 will pass alternately positive and negative pulses of amplitude $V_I/2$. Thus a low series resistance, nonpolarized capacitor has to be used. Several capacitors connected in parallel are often used.

When the conduction times of the transistors are equal, the DC voltage across C_3 is zero. If these times are different, a DC voltage will appear across this capacitor which will compensate the DC component in the transformer primary and thus minimize the chance for the transformer core saturation.

Fig. 4.59 Half-bridge push–pull converter



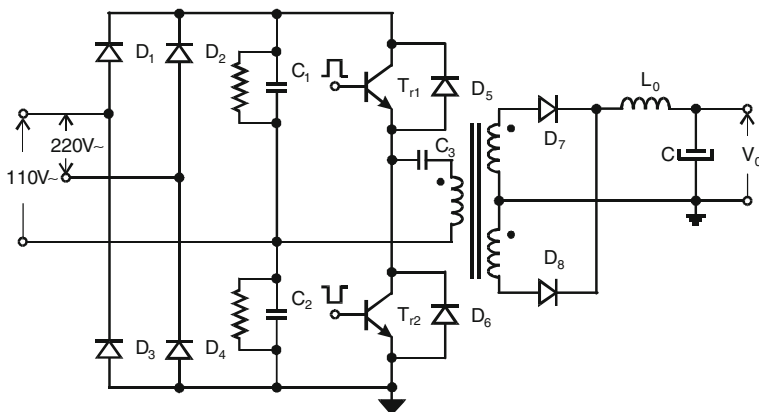


Fig. 4.60 Half-bridge converter having AC input 110 and 220 V

The approximate value of C_3 is chosen by applying the condition that the resonant frequency of the series resonant primary circuit is several times lower than the operating frequency of the converter, i.e.,

$$f_r = \frac{1}{2\pi\sqrt{L_r C}} \approx (0.15-0.4) \frac{1}{T}, \quad (4.264)$$

where C is the total capacitance of the primary and $L_r = n^2 L_o$ is the output inductance referred to the primary. The half-bridge converter is used when the primary source is AC voltage 110 and 220 V (Fig. 4.60).

The relaxation of the voltage load of the transistors is then very significant. The diodes D_5 and D_6 keep the reverse collector–emitter voltages of the transistors.

In fact, their purpose is twofold:

- They protect transistors against reverse conduction and possible destruction. Namely, if the load is cut off abruptly, the flux in the transformer increases. This causes oscillations which may induce reverse emitter–collector bias (collector at a lower potential). Then either D_5 or D_6 turns on and keeps the collector–emitter voltage at $V_{CE} = V_D$.
- When the corresponding transistor turns off, they direct the energy of the stray inductance back to the DC source.

4.5.6 Bridge Converter

The difference compared to the half-bridge converter is that the capacitors C_1 and C_2 are replaced by the transistors T_{r1} and T_{r2} (Fig. 4.61). The transistor pairs in the arms of the bridge (T_{r1} with T_{r3} and T_{r2} with T_{r4}) are on and off alternately,

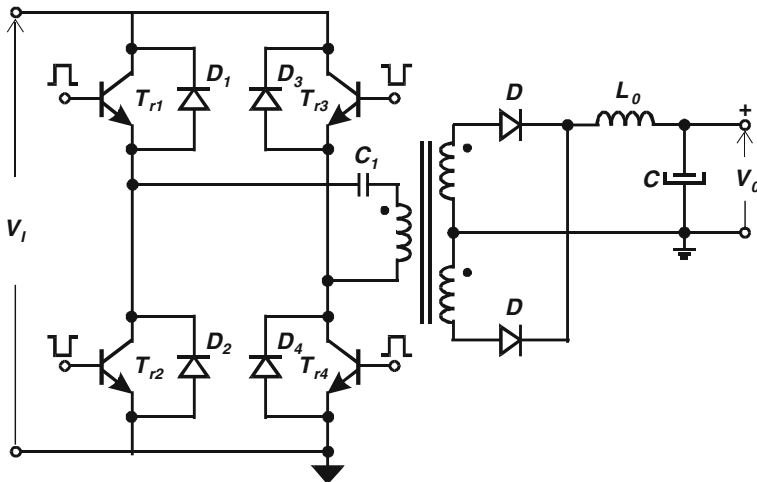


Fig. 4.61 Bridge circuit of the push–pull converter

connecting the transformer primary alternately to one or to the other side of the input. The primary voltage is thus $+V_I$ or $-V_I$. In one arm of the bridge when one of the transistors is on, the other is off (e.g., when T_{r1} is on, T_{r2} is off and vice versa) so

$$V_{CE\max} = V_I. \quad (4.265)$$

Therefore, the voltage load is halved and the current load is the same as that of the basic push–pull converter.

Both half-bridge and bridge converters have simpler transformers compared to those of the basic push–pull converter. This can be further simplified if only one primary and one secondary are used (Fig. 4.62). Then a diode rectifier bridge (diodes D_1 – D_4) is used in the secondary circuit. The pulse waveforms of the characteristic voltages and currents are shown in Fig. 4.62b.

When the transistor pair T_{r1} and T_{r3} is on, the core of the transformer is magnetized in one direction, whereas when the pair T_{r2} and T_{r4} is on, it is magnetized in the other direction of the magnetization curve. This creates a variation of the magnetic flux in the core. The AC rectangular voltage induced in the secondary is rectified by the diode bridge. The rectified voltage is $V_r = V_I/n$ and the variation of the current through the choke in this interval is

$$\Delta i_{L1} = \frac{V_I/n - V_o}{L_o} \delta \frac{T}{2}. \quad (4.266)$$

When none of the transistor pairs is on, the circuit of the magnetization current closes through the diode bridge. The transformer is short-circuited. The magnetic flux is the same as when the transistors went off. Within this interval the energy

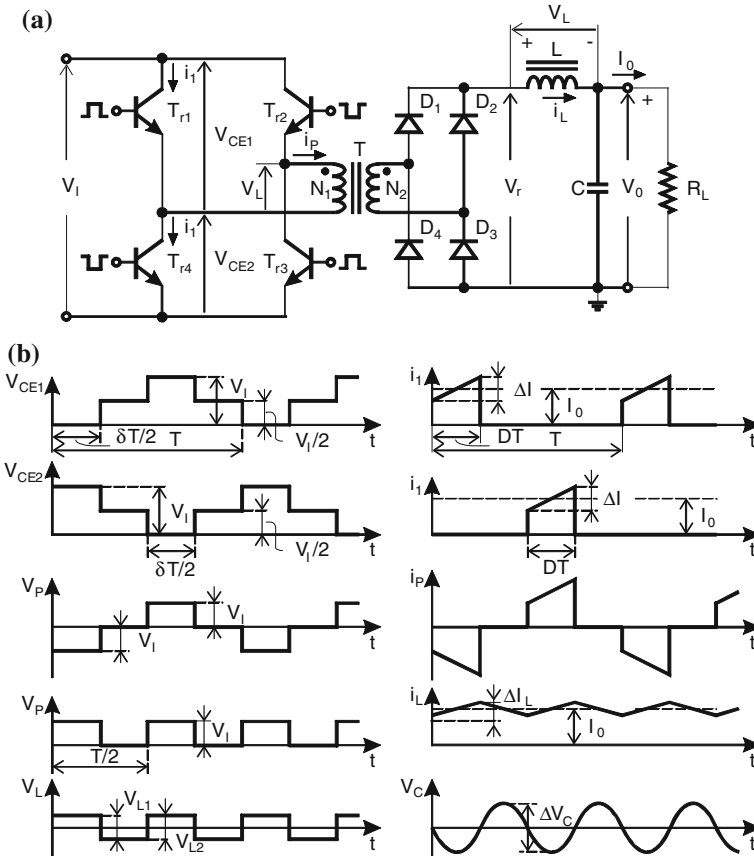


Fig. 4.62 Bridge circuit including diode bridge rectifier (a) and the characteristic pulse waveforms (b)

accumulated in the output choke is transferred to the load through the diode bridge. The rectified voltage is then $V_r = 0$. The current through the output choke decreases and its variation in this interval is

$$\Delta i_{L_2} = \frac{V_o}{L_1} (1 - \delta) \frac{T}{2}. \quad (4.267)$$

By equating (4.266) and (4.267) one obtains:

$$V_o = \delta \frac{V_I}{n}. \quad (4.268)$$

The influence of the realistic parameters is similar to the one identified for the basic push-pull converter. Here the emphasis should be placed on the phenomena arising during the turn-on and the turn-off processes. During the turn-on current

overshoots may occur (the collector current). Owing to this, the transistor may for a short cycle leave the saturation region which may increase considerably the losses in it. At sharp current changes, particularly in power converters, voltage oscillations on the secondary side of the transformer may occur. The instantaneous values of these voltages may exceed considerably the reverse breakdown voltages of the diodes. For this reason high-voltage diodes should be chosen. However, these diodes are characterized by longer recovery times which further increase the instantaneous current values. During the turn-off transient processes also arise that may cause reverse collector–emitter voltages.

A specific problem associated with the bridge converters is a relatively high complexity of the control circuitry. The control of the bridge transistors has to be done independently and is carried out by means of pulse transformers. Between the turn-on and the turn-off process a safety interval (dead time) has to exist.

The favorable properties of the bridge circuits are:

- simple transformer,
- relatively low collector–emitter voltage of transistors, and
- high output power.

4.5.7 Hamilton Circuit

The input of the improved bridge circuit (Fig. 4.63) [2] is a modified forward converter (with no filter capacitor) and its output is a modified bridge converter (with no output choke). The output choke is moved to the input. Owing to this, this circuit has the following favorable features:

- The need for balancing the DC components of the transformer is avoided, so no transistor is overloaded due to transformer core saturation.

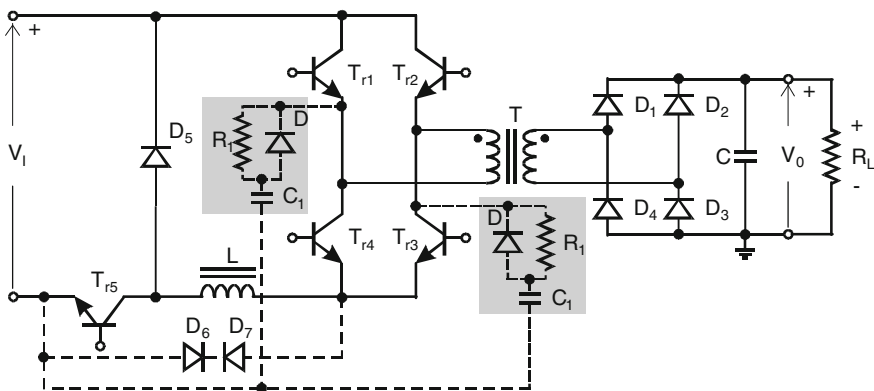


Fig. 4.63 Hamilton converter

- The limiting diodes (D_6 and D_7 —dotted lines in Fig. 4.63) very efficiently suppress output voltage transients that may arise due to sharp changes of the load and/or due to a sharp turn-on of the converter at a very high duty cycle.

Except for moving the choke from the output to the input, this circuit includes another two significant changes. The transistor T_{r5} and the diode D_5 have an additional control function. The transistors T_{r1} – T_{r4} in the bridge operate with a fixed duty cycle of 50 %. Consequently, the control of the output voltage is carried out by the transistor T_{r5} . This simplifies considerably the control circuit which is quite complex for the basic bridge circuit.

With the R–C–D network (dashed line in Fig. 4.63) the total reduction of the dynamic losses in the transistors is one order of magnitude higher compared to the basic bridge circuit. The selection of C and R in accordance with the following equations is recommended

$$C = \frac{I_L t_f}{V_1 + V_D}, \quad (4.269)$$

$$R = \frac{1}{6fC}, \quad (4.270)$$

where I_L is the maximum current through the choke, t_f is the falloff time of collector current and V_D is the voltage across the limiting diodes D_5 and D_6 . By introducing a current monitor in the circuit of the input choke it is possible, by means of a fast circuit and overcurrent protection, to keep efficiently the currents of all semiconductor elements below selected values.

Various authors emphasize that from the analysis of the idealized circuit one cannot identify a need for T_{r5} . The additional transistor T_{r5} , the diode D_5 , and the choke which is moved from the output to the input can well be justified if one looks at the phenomena arising in real circuits (circuits involving real parameters).

4.6 Ćuk Converters

By synthesizing the basic circuits of the forward and flyback converters Dr. Slobodan Ćuk has obtained several topologies of DC/DC converters which have been called Ćuk converters. A common property of these converters, making them different from other types, is that beside the electromagnetic, they also have the electrostatic energy transfer. In addition, Ćuk converters include a system of the coupled input–output coils which theoretically permits a complete elimination of current variations at the input and the output of the converter. This is very important from the point of view of elimination of the pulse noise inherent to all pulse DC/DC converters.

The basic circuit of a Ćuk converter (Fig. 4.64), similarly to a flyback converter, behaves like an inverter (the input and the output voltage are of the opposite

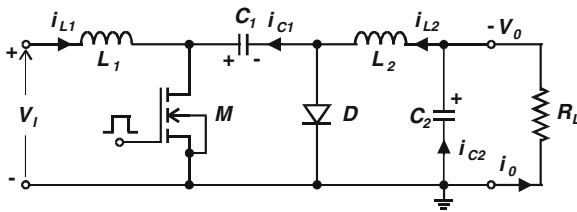


Fig. 4.64 Basic circuit of Ćuk converter

polarities), where the absolute value of the output voltage may be lower, higher or equal to the input voltage. To show this an idealized converter circuit will be considered (the transistor and the diode are ideal switches, output voltage and current are constant, power losses in the circuit are negligible).

When the transistor T_r is in saturation, the diode is off (Fig. 4.65a). The voltage across the input choke L_1 is constant and

$$i_{L1} = I_{L1m} + \frac{V_I}{L_1}t. \quad (4.271)$$

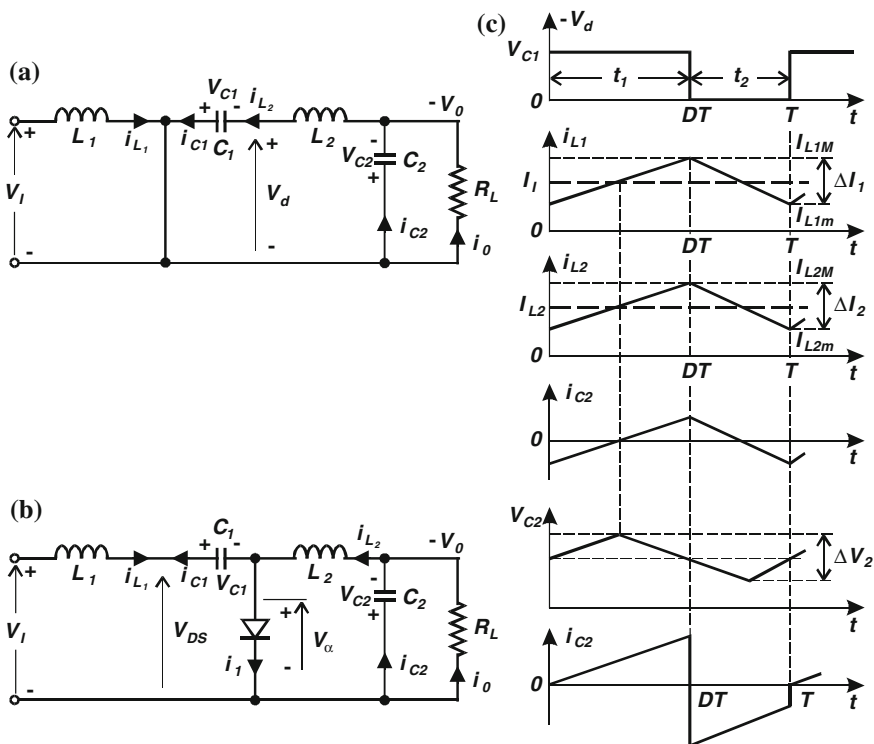


Fig. 4.65 Equivalent circuits during quasi-stable intervals t_1 (a), t_2 (b), and the characteristic waveforms of the voltages and currents (c)

Within this interval the energy accumulated in C_1 is transferred to the choke and to the load. If the variation of the voltage across C_1 is neglected and taking into account the assumption that the output voltage is constant, the voltage across L_2 is also constant. Therefore

$$i_{L2} = I_{L2m} - \frac{V_{C1} - V_o}{L_2} t. \quad (4.272)$$

During the quasi-stable interval $t_2 = (1 - D)T$ the transistor is off and the diode is on (Fig. 4.65b). Now the currents through the chokes L_1 and L_2 decrease linearly and are determined by

$$i_{L1} = I_{L1M} - \frac{V_{C1} - V_1}{L_1} t, \quad (4.273)$$

$$i_{L2} = I_{L2M} - \frac{V_o}{L_2} t. \quad (4.274)$$

The positive and negative changes of these currents are equal (Fig. 4.56c), i.e.,

$$\frac{V_1}{L_1} DT = \frac{V_{C1} - V_1}{L_1} (1 - D)T, \quad (4.275)$$

$$\frac{V_{C1} - V_o}{L_2} DT = \frac{V_o}{L_2} (1 - D)T. \quad (4.276)$$

From (4.275) it follows that

$$V_{C1} = \frac{V_1}{1 - D}, \quad (4.277)$$

and from (4.276) and (4.277)

$$V_o = \frac{D}{1 - D} V_1. \quad (4.278)$$

The variations ΔI_1 and ΔI_2 of the respective currents i_{L1} and i_{L2} are determined by

$$\Delta I_1 = \frac{DV_1}{fL_1}, \quad (4.279)$$

$$\Delta I_2 = \frac{DV_1}{fL_2}, \quad (4.280)$$

where $f = 1/T$ is the frequency of the control pulses. If $L_1 = L_2$ then $\Delta I_1 = \Delta I_2$. The voltages across the chokes are equal in both quasi-stable states. During the interval t_1

$$V_{L1} = V_I; \quad V_{L2} = V_{C1} - V_o = V_I, \quad (4.281)$$

and during the interval t_2

$$V_{L1} = V_{C1} - V_I = \frac{D}{1-D} V_I = V_o; \quad V_{L2} = V_o. \quad (4.282)$$

While the transistor is off, the capacitor C_1 is charged by the input current. If the average value of this current is I_1 , then peak-to-peak variation of the voltage across C_1 is approximately given by

$$\Delta v_{C1} \approx \frac{1}{C_1} \int_0^{t_2} I_1 dt = \frac{I_1(1-D)}{C_1 f}. \quad (4.283)$$

If the losses in the circuit are neglected, then $V_I I_1 = V_o I_o$ and

$$I_1 = \frac{D}{1-D} I_o, \quad (4.284)$$

where I_o is the load current.

The characteristic voltage and current waveforms are shown in Fig. 4.65c.

Example 4.9 The Ćuk converter shown in Fig. 4.64 has $V_I = 12$ V and $D = 0.6$. Determine the output voltage V_o .

As the average value of voltage at each inductance equal to 0, it can be written that

$$\begin{aligned} \bar{v}_{L1} = 0 : \quad V_I D T_S &= (V_{C1} - V_I)(1-D)T_S \Rightarrow V_{C1} = \frac{V_I}{1-D}; \\ \bar{v}_{L2} = 0 : \quad (V_{C1} - V_o) D T_S &= V_o(1-D)T_S \Rightarrow V_o = D V_C \\ \Rightarrow V_o &= \frac{D}{1-D} V_I = 18 \text{ V}. \end{aligned}$$

4.6.1 Elimination of the Current Ripple

The main favorable property of Ćuk converters is the existence of the possibility to eliminate the ripple from the input and/or the output current. This is accomplished by coupling both coils with a common core (Fig. 4.66).

This is possible since the variations of the voltages across these coils are equal. By a suitable choice of the coupling coefficient it is possible to eliminate completely the ripple of the currents. Figure 4.66a shows an example of a Ćuk converter having coupled coils for the purpose of elimination of the output current ripple.

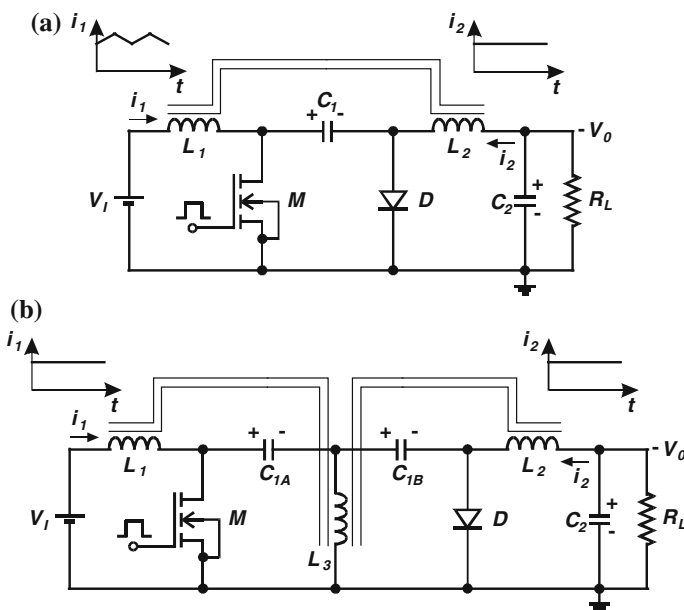


Fig. 4.66 Ćuk converters comprising coupled coils for elimination of the ripple: (a) of the output current, (b) of the input and output currents

The relations valid for the circuit will remain unchanged if the capacitor C_1 is split in two series capacitors C_{1A} and C_{1B} , so that the total capacitance is C_1 and if a third choke is added (Fig. 4.64b) under the condition that $L_3 \gg L_1$ and $L_3 \gg L_2$. Since the impedance of the third choke is much higher, its influence on the basic relations within the circuit is negligible. This, however, allows the elimination of the ripple of the input and output currents by coupling L_3 with L_1 and L_2 . All three coils are wound on a common core.

4.6.2 Ćuk Converters with Galvanic Isolation

If the third coil, L_3 , is replaced by an isolation transformer one obtains a Ćuk converter with galvanic isolation (Fig. 4.67). By coupling the transformer with the coils L_1 and L_2 (Fig. 4.67b) it is possible to eliminate completely the ripple of both the input and the output current.

The transformer and the input and output coils are wound on the same core. It is difficult to achieve such coupling that the current ripple is eliminated entirely. For this reason in practice tuning coils of small inductance on the primary or/and secondary side are used.

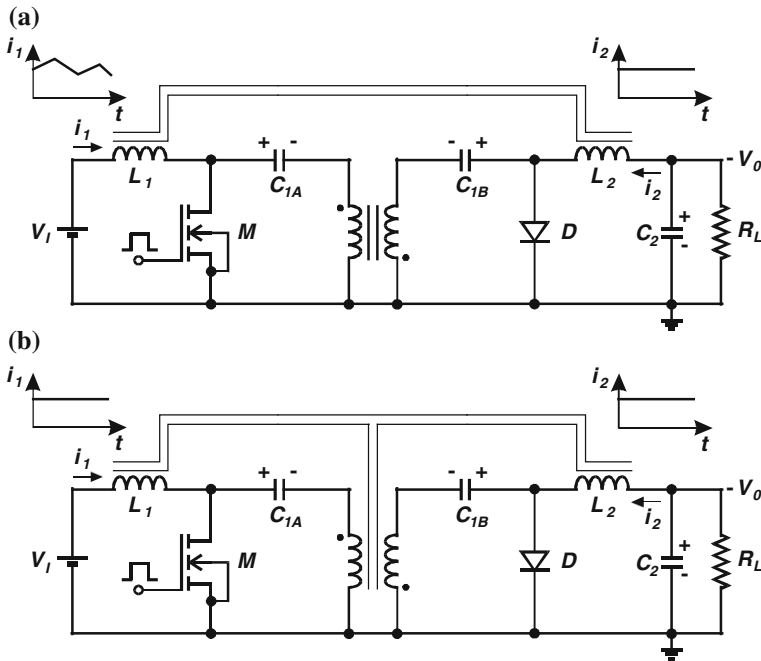


Fig. 4.67 Ćuk converters comprising galvanic isolation and current ripple elimination: (a) of the output current and (b) of both input and output currents

It should be emphasized that, with the assumption that the transformer is ideal, the relations between voltages and currents in the circuit remain the same as in the nonisolated circuits. The difference is that the circuits in Fig. 4.65 have positive output voltages and that the transistor and diode are loaded more, since they also conduct the current with regard to the input or output.

Thanks to the capacitors C_A and C_B there is no DC component in the transformer windings. This allows a full exploitation of the core which, compared to flyback converters, considerably reduces the size of the transformer.

Problems

- 4.1 Design a buck converter (Fig. 4.3) if $V_1 = 48$ V, $V_0 = 18$ V, $R_L = 10$ Ω so the variation of the output voltage is less than 0.5 %. The converter should operate in the continuous mode.
- 4.2 For the buck converter from Fig. 4.3, which has all components ideal (a) derive expressions for the V_0/V_1 in continuous mode, and (b) calculate and draw the waveforms of voltages and currents at the transistor and the diode during one period of the control signal.
- 4.3 The forward converter from Fig. 4.20a has: $V_1 = 36$ V, $L_o = 0.5$ mH, $R = 10$ Ω , $C = 150$ mF, $N_1/N_2 = 2$, $N_1/N_3 = 1$, $f = 50$ kHz and $D = 0.3$. All the used components are ideal.

- 4.8 The push–pull from Fig. 4.47 has the following parameters: $V_S = 48\text{ V}$, $D = 0.4$, $f = 35\text{ kHz}$, $L = 400\text{ }\mu\text{H}$, $C = 100\text{ }\mu\text{F}$, $N_1/N_2 = 1.5$, $N_1/N_3 = 1$ and $R = 10\text{ }\Omega$. Calculate and draw the waveforms of the following variables: v_o , i_L , i_{t1} and i_{D1} .
- 4.9 The Ćuk converter from Fig. 4.64 has the following parameters: $V_I = 18\text{ V}$, $L_1 = L_2 = 1\text{ mH}$, $C_1 = C_2 = 20\text{ }\mu\text{F}$, $D = 0.6$, $R = 10\text{ }\Omega$ and $f = 20\text{ kHz}$.
- (a) Determine the output voltage.
 - (b) Determine average, minimum and maximum current in L_1 and L_2 .

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2. Calkin, E.T., Hamilton, B.H.: A conceptually new approach for regulated DC to DC converters employing transistor switchers and pulsewidth control. IEEE Trans. Ind. Appl. **IA-12**(4), 369–377 (1976)

Chapter 5

Control Modules

The control modules (CM) of the pulse voltage stabilizers close the automatic control loop between the input (pulse amplifier and power transistor) and the output (output *LC* filter) of the stabilizer, which maintains the load voltage constant within a pre-assigned accuracy. Control is accomplished by converting the error signal into a pulse sequence, which drives a pulse amplifier.

There are several different structures of control modules. In principle, however, they can all be divided into two groups. The first group consists of the CM having a relay transfer characteristic. Depending on the value of the input signal, the output stage of the control module is either on or off. Stabilizers having this type of CM are called relay or two-state stabilizers. This group is classified into the pulse DC/DC converters with linear microelectronic stabilizers. The second group consists of control modules generating sequences of pulses of variable duty cycles. The duty cycle is error signal dependent with the frequency remaining constant—pulse-width modulation (PWM), or the frequency is variable with the pulse width remaining constant—frequency pulse modulation (FPM) (in some cases both types of modulation proceed simultaneously).

In a relay voltage stabilizer, the output voltage is compared with a stable voltage reference. The comparison is continuous and the state at the output of the control module changes when the error signal (the difference between the output and the reference voltage) reaches a level equal to the value of the voltage hysteresis of the CM relay characteristic. In a pulse-width modulation stabilizer, the error signal changes the state of the CM at discrete time intervals. Thus, it could be said that the dynamic properties of the relay stabilizers are superior to those of the pulse-width modulation stabilizers. However, the advantage of the relay stabilizers as regards the continuity of the comparison does not show because the dynamic characteristics of all pulse stabilizers are mostly determined by the characteristics of the output *LC* filter. On the other hand, the relay stabilizers suffer from a number of shortcomings. First of all, the frequency of control pulses is dependent on the load current and the input voltage variations. This leads to considerably more rigorous requirements for the output filter design. Also, the variable component of the output voltage contains significantly more harmonics that are often undesirable. This also applies to the FPM stabilizers. The operating frequency of the pulse-width modulation stabilizers

is either constant or its variations are very small. This is exactly the reason that in practice a CM based on pulse-width modulation is more commonly employed.

The control modules involving current programming where the ratio signal/pause is determined by the time required that the current through the switch reaches a certain value (current threshold) are becoming increasingly interesting. The current threshold is determined by the control signal of the control module. The CM involving current programming is characterized by a precisely defined current through the switch, an overload protection, an even distribution of the load when operating in parallel and superior control dynamics. Two techniques of current programming are in use: constant frequency and constant pause but variable frequency.

Control modules employing constant frequency and a variable duty cycle are most widespread today. These are, therefore, circuits based on the pulse-width modulation (PWM). These circuits will be analyzed in this chapter.

5.1 Basic Principles and Characteristics of PWM Control Modules

The basic block-scheme of a pulse-width modulator (PWM), shown in Fig. 5.1, consists of two comparators A and B (B involves hysteresis—Schmitt trigger), two current generators, an electronic switch S_w , and a timing capacitor C . The current generator switch S_w , the capacitor C , and the comparator B constitute a generator of triangular voltage. The triangular voltage form V_2 (Fig. 5.1b) is generated through the process of charging and discharging of the capacitor C by the constant currents I_1 and I_2 . Namely, if the output of the comparator B is at a low voltage level, the switch S_w is in position (5.1). Then, the capacitor is charged by the current I_1 and the voltage V_2 grows:

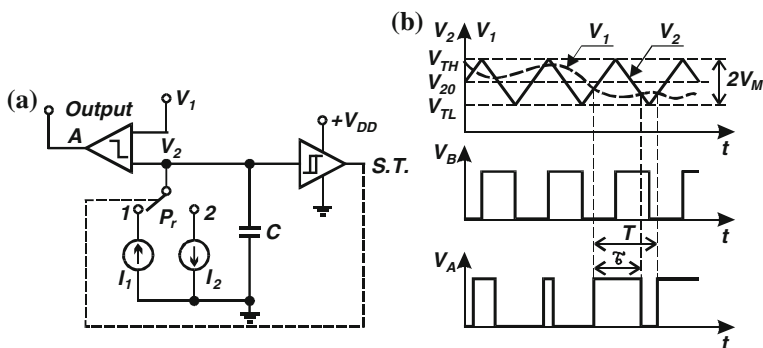


Fig. 5.1 Basic block-scheme of a PWM (a) and the voltage waveforms (b)

$$V_2(t) = V_{TL} + \frac{1}{C} I_1 t.$$

When the voltage level is high at the output of comparator B , the generator of current I_2 is on and the voltage V_2 is

$$V_2(t) = V_{TH} - \frac{1}{C} I_2 t.$$

V_{TH} and V_{TL} are the respective high and low threshold voltages of the Schmitt trigger (ST). The state of its output changes at the instant when V_2 equals V_{TH} or V_{TL} , and the cycle of generator oscillation is

$$T = C \left(\frac{1}{I_1} + \frac{1}{I_2} \right) V_H, \quad (5.1)$$

where V_H is the width of the voltage hysteresis of ST. The amplitude V_M and the DC component V_{20} of the triangular voltage are defined by

$$V_M = \frac{V_H}{2}, \quad V_{20} = \frac{V_{TH} + V_{TL}}{2}. \quad (5.2)$$

DC component V_{20} coincides with the center of the hysteresis of the ST, i.e., $V_{20} = V_{ch}$.

Pulse-width modulation is accomplished by feeding the triangular voltage V_2 and a fraction of the output voltage to the inputs 1 and 2 of the comparator A

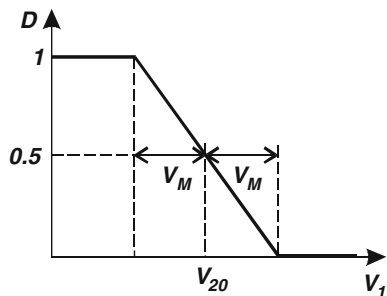
$$V_1 = k_0 V_0, \quad (5.3)$$

where $0 < k_0 < 1$. If $V_1 > V_2$, at the output of the comparator A there will be a low voltage level, but if $V_1 < V_2$, the output will be at high a voltage level (Fig. 5.1). Obviously, by varying the voltage V_1 , the time intervals of the signal and the pause at the output of the comparator A will vary. The frequency will be constant and equal to the frequency of the triangular voltage. By using the time diagrams of the voltages V_1 and V_2 (Fig. 5.1), it can be shown that the time interval of the signal within one cycle T , neglecting the variation of V_1 , is determined by

$$\tau = \frac{V_{20} + V_M - V_1}{2V_M} \quad T = \frac{V_{TH} - V_1}{V_H} T. \quad (5.4)$$

The static characteristic of PWM is the dependence of the duty cycle D of the control pulses on the variation of the output voltage of the stabilizer (Fig. 5.2). PWM is realized in the linear region of the static characteristic. For $V_1 < V_{20} - V_M$, $D = 1$ and for $V_1 > V_{20} + V_M$, $D = 0$, the system of automatic control is interrupted and the control transistor of the DC/DC converter will remain in either the on or the off state.

Fig. 5.2 Static characteristic of PWM, the dependence of duty cycle D of the control pulses on the variation of the output voltage of the stabilizer



5.1.1 Circuit Analysis

The instability of the output voltage of the stabilizer as a function of the circuit parameters will be analyzed first. To keep the output voltage unchanged within the pre-assigned limit ΔV_0 when the input voltage varies by ΔV_I , it is necessary that the duty cycle is changed by ΔD . With (4.11) in view

$$\Delta D = \frac{V_0 + \Delta V_0}{V_I + \Delta V_I} - \frac{V_0}{V_I}, \quad (5.5)$$

where V_I and V_0 are the nominal values of the input and the output voltage, respectively. On the other hand, a change of V_0 will cause a change of V_I

$$\Delta V_I = k_0 \Delta V_0. \quad (5.6)$$

The change of the duty cycle is proportional to the change of the input voltage V_I and the slope of the static characteristic of the control module, i.e.

$$\Delta D = \frac{dD}{dV_I} \Delta V_I. \quad (5.7)$$

By differentiating (5.4) over V_I and introducing (5.7), one obtains

$$\Delta D = -\frac{k_0}{2V_M} \Delta V_0. \quad (5.8)$$

By equating (5.5) and (5.8), taking into account that always $V_0 \gg \Delta V_0$, the instability of the output voltage is obtained as

$$\delta_o = \frac{\Delta V_0}{V_0} = \frac{2V_M \delta_I}{k_0 V_I (1 + \delta_I)}, \quad (5.9)$$

where $\delta_I = \Delta V_I / V_I$ is the instability of the input voltage. The coefficient of voltage stabilization is defined as

$$K_n = \frac{\delta_I}{\delta_o} = k_0 \frac{V_I(1 + \delta_I)}{2V_M}. \quad (5.10)$$

The output resistance of the stabilizer depends on the coefficient of stabilization and is determined by

$$R_o = \frac{R_L}{K_n} \frac{V_0 \Delta I_{cav}}{V_I \Delta I_L} = \frac{2 \Delta I_{cav}}{k_o(1 + \delta_I)} \frac{V_0}{V_I^2} V_M. \quad (5.11)$$

From (5.10) and (5.11), it is seen that the coefficient of stabilization and the output resistance are dependent on the amplitude V_M of the auxiliary signal of the control module. The coefficient of stabilization is inversely proportional to the amplitude V_M and the output resistance directly. Therefore, the amplitude of the triangular voltage should be as small as possible. However, it is certain that there exists a low limit below which the pulse-width modulation will not proceed. For instance, if $V_M = 0$, then $V_2 = k_0 V_0$ (Fig. 5.3) and relay stabilization is accomplished. At that, the frequency f_r of the control transistor is known in advance and is dependent on the parameters of the output LC filter, the input voltage V_I , and the load current I_L . Let the frequency of the triangular voltage be several times higher than f_r . Then, when V_M increases, it is possible that the operating frequency of the stabilizer f_s falls between f and f_r , i.e., $f_r < f_s < f$ (Fig. 5.3c). In that case, as shown in Fig. 5.3c, the change of the load current or of the input voltage leads to a step change of the operating frequency of the stabilizer, thus to an instability of the operation. A further increase in the amplitude of the triangular voltage leads to an operating mode where $f_r = f$ (Fig. 5.3d). The pulse-width modulation is accomplished. The principle of pulse-width modulation will be realized if at instants t_0 , t_2 , and t_4 , when the state at the output of the control module is changed, the following condition is fulfilled:

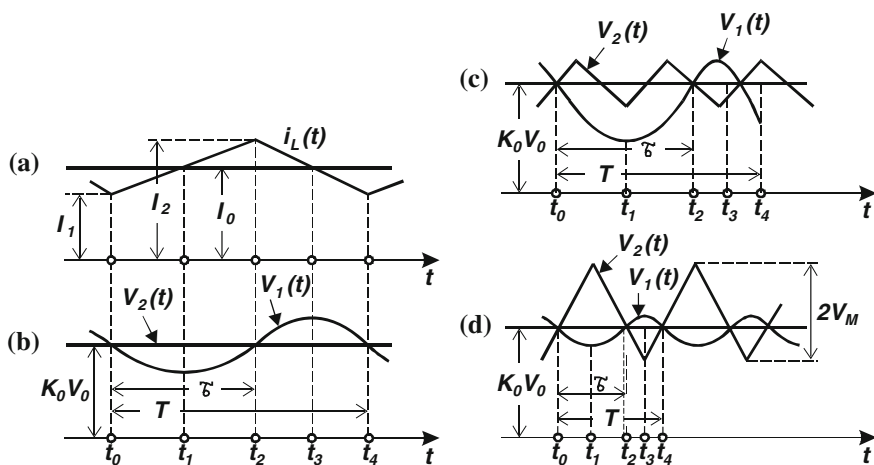


Fig. 5.3 Voltage waveforms for different amplitudes of the auxiliary voltage (a, b, c and d)

$$\left| \frac{dV_2}{dt} \right| > \left| \frac{dV_1}{dt} \right|. \quad (5.12)$$

After differentiating (4.15) over t and rearranging, one obtains

$$\left| \frac{dV_1}{dt} \right|_{t=\tau} = 4k_0 f \frac{D + 2\xi}{D + 4\xi^2/(1-D)} \Delta V_0, \quad (5.13)$$

where the change of the output voltage ΔV_0 is given by (4.17). From the time diagram of Fig. 5.1b, it can be shown that

$$V_2(t) = V_{TL} + \frac{2V_M}{aT}t, \quad (5.14)$$

where $0.5 < a < 1$ is the coefficient of asymmetry of the triangular voltage.

From (5.14), one obtains

$$\left| \frac{dV_2}{dt} \right| = \frac{2V_M}{a}f. \quad (5.15)$$

By combining (5.12), (5.13), and (5.15), it follows that

$$V_M > 2ak_0 \frac{D + 2\xi}{D + 4\xi^2/(1-D)} \Delta V_0. \quad (5.16)$$

The condition (5.12) has to be fulfilled for all values of the duty cycle ($D_{\min} < D < D_{\max}$). Since the right-hand side of (5.16) is maximal when the duty cycle is minimum, the minimum amplitude of the triangular voltage will be dependent on $D_{\min}$. From (5.16), it is also seen that V_M depends on the coefficient of asymmetry of the triangular voltage and that it is minimal for $a = 0.5$ and maximal for $a = 1$.

The dependence of the error of the amplitude V_M , according to (5.16), with respect to a purely capacitive change of the output voltage ($\xi = 0$), on the constant ξ with the duty cycle D as parameter is expressed as

$$\Delta V_M = \frac{V_M - \Delta V_c}{\Delta V_c} = \frac{2\xi}{D + 2\xi}.$$

For instance, for $D = 0.2$ the error is from 50 to 90 %. Inequality (5.16) allows the selection of the optimum amplitude of the triangular voltage for any ξ . The usual practice is that ξ is not greater than 0.1. For instance, for $\xi = 0.1$, $D_{\min} = 0.2$ and a symmetrical triangular voltage, it follows that

$$V_M > 1.6 k_0 \Delta V_0. \quad (5.17)$$

5.1.2 Simple PWM

From (5.17), it can be seen that the amplitude of the triangular voltage should be of the same order of magnitude as the maximum variation of the output voltage of the stabilizer. This variation, depending on various technical requirements, is usually within several hundreds of mV. If the permissible variation of the output voltage is higher than several tens of mV, one can use the simple circuit shown in Fig. 5.4a as PWM, where the resistor R replaces the current generators. The output of the Schmitt trigger is inverted. The input resistance of ST has to be much higher than R . The ST with a resistance and a capacitance constitutes a stable generator with the cycle of oscillation

$$T = RC \ln \frac{(V_{OH} - V_{TL})V_{TH}}{(V_{OH} - V_{TH})V_{TL}}. \quad (5.18)$$

V_{OH} is the voltage of logical one at the output of ST, whereas the voltage of logical zero is neglected. Since the capacitor is charged and discharged through the resistance R , the variation of $V_2(t)$ is exponential (Fig. 5.4b). Owing to this, the static characteristic of the control module will be nonlinear. It will be almost linear if the voltage hysteresis is much smaller than the lower threshold, i.e.

$$V_H = V_{TH} - V_{TL} \ll V_{TL}. \quad (5.19)$$

Then, the variation of voltage V_2 compared to its DC component is negligibly small, so the current through the resistance R is constant and its direction depends on the voltage at the output of ST. When the voltage at this output is high, the current charging the capacitor is

$$I_1 \approx \frac{V_{OH} - V_{20}}{R}, \quad (5.20)$$

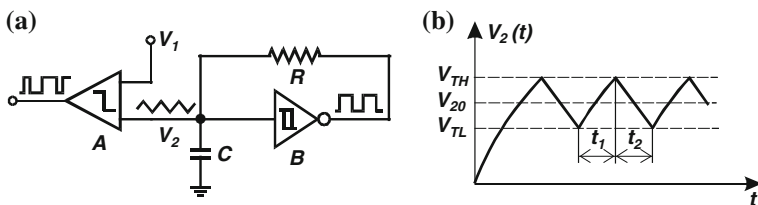


Fig. 5.4 Basic block-scheme of a simple PWM (a) the waveform of the auxiliary voltage (b)

where $V_{20} = (V_{TH} + V_{TL})/2$. Then

$$V_2(t) = V_{TL} + \frac{I_1}{C}t. \quad (5.21)$$

From the above equation and the condition $V_2(t_1) = V_{TH}$, one obtains

$$t_1 = RC \frac{V_{TH} - V_{TL}}{V_{OH} - V_{20}} = RC \frac{V_H}{V_{OH} - V_{20}}. \quad (5.22)$$

Now the voltage at the output of ST is low and the capacitor is charged in the opposite direction by the current

$$I_2 \approx \frac{V_{20} - V_{OL}}{R} \approx \frac{V_{20}}{R}, \quad (5.23)$$

where the low voltage level is $V_{OL} \approx 0$. Therefore

$$V_2(t) = V_{TH} - \frac{V_{20}}{RC}t. \quad (5.24)$$

The next change of state at the output of ST will occur at $V_2(t_2) = V_{TL}$, so that

$$t_2 = RC \frac{V_{TH} - V_{TL}}{V_{220}} = RC \frac{V_H}{V_{20}}. \quad (5.25)$$

The cycle time $T = t_1 + t_2$ is thus

$$T = RC \frac{V_H}{V_{20}(1 - V_{20}/V_{OH})}. \quad (5.26)$$

In order to obtain a symmetric triangular voltage, the currents I_1 and I_2 have to be equal, wherefrom it follows that the DC component should be equal to one half of the high-voltage level

$$V_{20} = \frac{V_{OH}}{2}. \quad (5.27)$$

Quite often, however, a sawtooth voltage ($a = 1$) is used as the auxiliary voltage. Then, the stability of the frequency is higher. The basic block-scheme of the sawtooth voltage generator shown in Fig. 5.5 contains a non-inverting Schmitt trigger. The additional element is the transistor T_r , which enables discharge of the capacitor C . When the condition (5.19) is fulfilled, the current generator can be

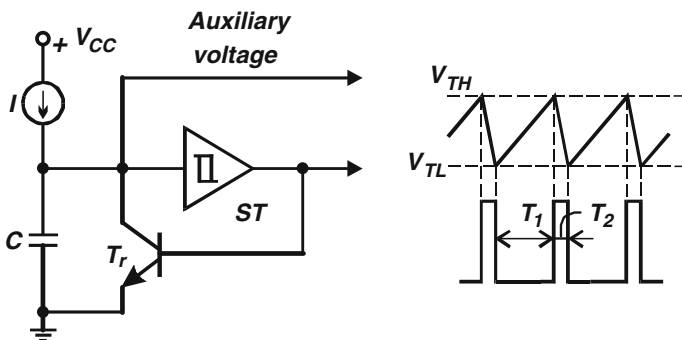


Fig. 5.5 Basic block-scheme of the sawtooth voltage generator

replaced by a resistor. The input resistance of ST has to be very high. Let the output of ST be low. T_r is then off and C is being charged

$$V_c(t) = V_{TL} + \frac{1}{C} It. \quad (5.28)$$

From $V_c(T_1) = V_{TH}$ and (5.21), it follows

$$T_1 = C \frac{V_H}{I}. \quad (5.29)$$

Now the output of ST is high and T_r is on and in the active region. The capacitor C is being discharged, so

$$V_c(t) = V_{TH} - \frac{1}{C} (\beta I_B - I)t, \quad (5.30)$$

where β is the current gain of the transistor T_r . This quasi-stable interval ends at $V_c(T_2) = V_{TL}$

$$T_2 = C \frac{V_H}{\beta I_B - I}. \quad (5.31)$$

If the generator waveform should be sawtooth, then it is mandatory that $T_1 \gg T_2$, thus $\beta I_B \gg I$. Then

$$T_2 \approx C \frac{V_H}{\beta I_B}, \quad (5.32)$$

and the cycle time of the auxiliary voltage is $T = T_1 + T_2 \approx T_1$. Here too, the DC component of the auxiliary voltage is equal to the center of the hysteresis.

Example 5.1 Determine the base current of the transistor T_r in circuit shown in Fig. 5.5, so that it is $T_1/T_2 = 100$. The transistor current gain β is 100.

From (Eq. 5.22) and (Eq. 5.24), it follows that

$$\frac{T_1}{T_2} = \beta I_B / I - 1 = 100, \text{ so } I_B = 1.01 I.$$

5.1.2.1 Auxiliary Voltage Generators in Integrated Circuit Form

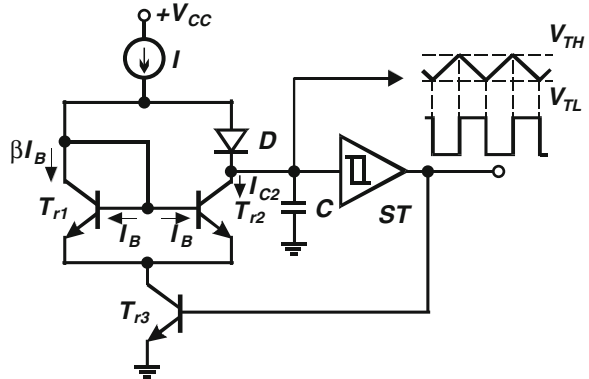
Figure 5.6 shows the basic scheme of a generator of symmetric triangular voltage containing one current generator. This approach is employed when the generator is implemented as a constituent part of a monolithic (integrated) circuit. Thanks to the current mirror constituted by the transistors T_{r1} and T_{r2} the capacitor is charged and discharged by the current I of the generator. Namely, when the output is low, T_{r3} is cut off. Owing to this, T_{r1} and T_{r2} are off. The diode D is conducting and C is being charged by the current I . It is implied that the input current of the ST is obviously negligibly small. Then

$$v_c(t) = V_{TL} + \frac{I}{C} t. \quad (5.33)$$

When the output of ST is high, T_{r3} is saturated. T_{r1} and T_{r2} are on and the diode D is off. The currents of the transistors T_{r1} and T_{r2} for this half-cycle are marked in Fig. 5.6. It is implied that the characteristics of the transistors are identical. Then

$$I_{C2} = \frac{\beta}{\beta + 2} I.$$

Fig. 5.6 Basic scheme of the generator of symmetric triangular voltage



Since D is off, the capacitor C is being discharged by the current I_{c2} . For $\beta \gg 2$, $I_{c2} \approx I$ and

$$v_c(t) = V_{TH} - \frac{I}{C}t. \quad (5.34)$$

The cycle of oscillation is

$$T = 2C \frac{V_H}{I}. \quad (5.35)$$

One of the possible versions of the current generator is shown in Fig. 5.7. I_E is the polarization current of the transistor. If the emitter junction voltages of T_{r1} and T_{r2} are equal, the voltage drop across R is $V_{CC} - V_x$. Since the base current of T_{r2} can be neglected, the current I is equal to the current through R , i.e.

$$I = \frac{V_{CC} - V_x}{R}. \quad (5.36)$$

By introducing (5.35) in (5.36), the frequency of the generator

$$f = \frac{1}{T} = \frac{1}{2RC} \frac{V_{CC}}{V_H} \left(1 - \frac{V_x}{V_{CC}} \right) \quad (5.37)$$

is obtained as a linear function of the control voltage V_x .

The stability of the frequency and amplitude of the triangular voltage are dependent on the thresholds of ST. In addition to a high stability, a possibility for a simple threshold control with negligibly small variations from circuit to circuit should exist. All this can be accomplished by using the basic scheme of ST shown in Fig. 5.8. The differential comparators K_1 and K_2 have the respective thresholds

$$V_{T1} = V_{REF}, \quad V_{T2} = \frac{R_2}{R_1 + R_2} V_{REF}. \quad (5.38)$$

Fig. 5.7 Constant current source

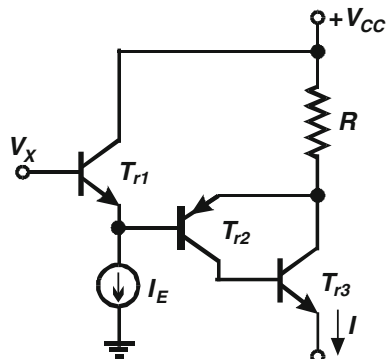
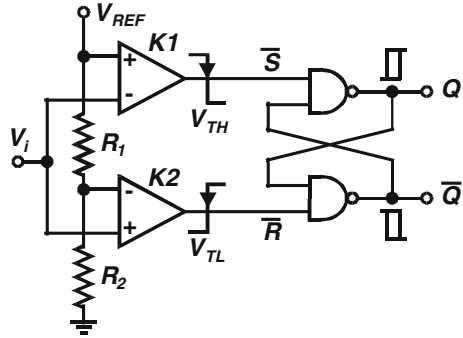


Fig. 5.8 Basic scheme of an integrated Schmitt trigger



V_{REF} is the output of the reference voltage source common for the whole integrated circuit of which ST is only a small part. Thanks to the RS latch, the transfer characteristic at the outputs Q and $\bar{Q}$ is of the hysteresis form.

Let the input rise from 0 to V_{CC} . For $V_i = 0$, at the outputs of K_1 and K_2 one has $S = 1$ and $R = 0$. Therefore, $Q = 0$. At $V_i = V_{T2} < V_{T1}$, $R = 1$, but the state at the output of the RS latch does not change because $S = R = 1$. Only when $V_i = V_{T1}$, $S = 0$ and the output Q becomes high. When the input decreases from V_{CC} to 0, since $V_{T1} > V_{T2}$ the output of K_2 changes first and becomes high at $V_i = V_{T1}$. Since both inputs of the latch are now high, i.e., $S = R$, the state of the output remains unchanged ($Q = 1$). Only when $V_i = V_{T2}$, $R = 0$, and the latch is erased ($Q = 0$). Therefore, in the course of a positive variation of the input voltage the output Q becomes high when $V_i = V_{TH} = V_{T1}$, whereas for a negative variation Q becomes low when $V_i = V_{TL} = V_{T2}$. Thus, the thresholds of the ST are given by

$$V_{TH} = V_{REF}, \quad (5.39)$$

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_{REF}. \quad (5.40)$$

It should be emphasized that the RS latch can be realized by applying NOR logic circuitry. Then, compared to Fig. 5.8 the inputs of K_1 and K_2 should be changed. Namely, the comparator K_1 should be non-inverting (V_i to “+” and V_{REF} to “-” input), whereas K_2 should be inverting.

Example 5.2 A symmetrical triangular voltage generator is realized using the circuits shown in Figs. 5.6 and 5.8. Its voltage is changed from 2 to 6 V. Determine:

- The reference voltage V_{REF} and the resistance R_1 if $R_2 = 2 \text{ k}\Omega$.
- The capacitance C , if $I = 32 \text{ }\mu\text{A}$, and the frequency of generator is $f = 40 \text{ kHz}$.
- Triangular voltage varies between the thresholds of the Schmitt trigger, so that $V_{TL} = 2 \text{ V}$ and $V_{TH} = 6 \text{ V}$. From (Eq. 5.39) follows $V_{REF} = 6 \text{ V}$, and based on (Eq. 5.40) one obtains $R_1 = 2R_2 = 4 \text{ k}\Omega$.
- From (Eq. 5.34) it follows that

$$C = \frac{I}{2(V_{TH} - V_{TL})f} = \frac{32 \times 10^{-6}}{2(6 - 2) \times 40 \times 10^3} = 100 \text{ pF}.$$

5.2 Voltage-Controlled PWM

The pulse-width controller (PWM) is in the feedback loop between the output and the input of a DC/DC converter. The feedback loop maintains the constant designed output irrespective of the input voltage or load variations. The x control is realized in such a way that a variation of the input signal of the feedback loop, or of the PWM, changes the width of the control pulse applied to the switch at a constant frequency. Depending on the character of the PWM input signal, voltage or current, one deals with:

- voltage control or
- current control.

The block diagram of a voltage-controlled forward DC/DC converter is shown in Fig. 5.9. Since the variations of the output voltage are very small (below 100 mV), the control signal is taken from the output of the error amplifier EA so that

$$V_1 = V_c = A_v(k_o V_0 - V_{REF}), \quad (5.41)$$

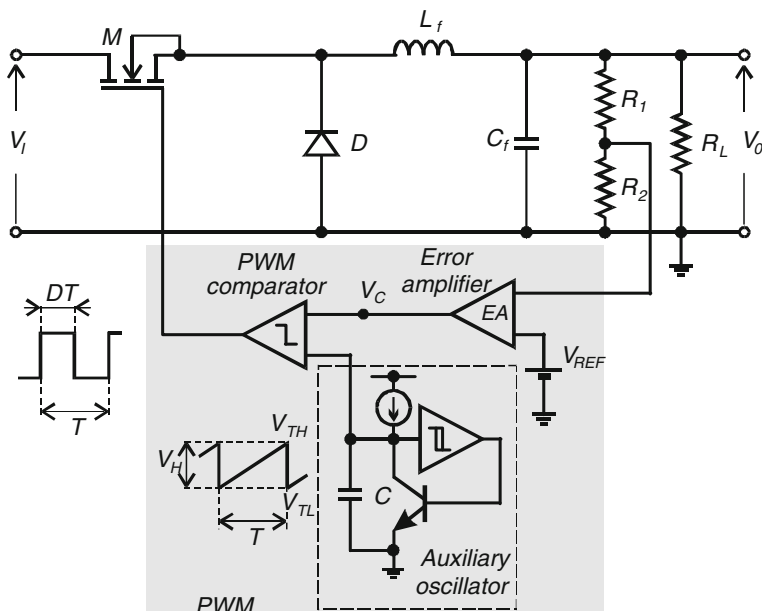


Fig. 5.9 Block diagram of a voltage-controlled forward converter

where A_v is the voltage gain of the error amplifier, V_{REF} is the temperature and voltage compensated reference voltage, and

$$k_o = \frac{R_2}{R_1 + R_2}. \quad (5.42)$$

A sample of the output voltage variation is taken from the voltage divider R_1, R_2 , it is compared with the reference voltage, and amplified by the error amplifier. Amplification A_v is calculated to ensure that within the permitted range of the variations of the output voltage V_o , the control voltage V_c remains within limits

$$V_{\text{TL}} < V_c < V_{\text{TH}}, \quad (5.43)$$

where V_{TH} and V_{TL} are the threshold voltages of the Schmitt trigger of the auxiliary oscillator.

Since for the forward DC/DC converter $V_o = DV_I = (\tau/T)V_I$, from (5.4) it follows

$$V_o = \frac{A_v V_{\text{REF}} V_I / V_H}{1 + A_v k_o V_I / V_H} \left(1 + \frac{V_{\text{TH}}}{A_v V_{\text{REF}}} \right). \quad (5.44)$$

In practice, it is always $V_I > V_H$, $k_o < 1$ and $A_v \gg 1$. The ratio of the upper threshold V_{TH} of the Schmitt trigger and the reference voltage V_{REF} may be arbitrary, but for the majority of PWM integrated circuits $0.5 < V_{\text{TH}}/V_{\text{REF}} < 2$. Bearing this in mind, it follows that $A_v k_o V_I / V_H \gg 1$ and $1 \gg V_{\text{TH}} / (A_v V_{\text{REF}})$ so

$$V_o \approx \frac{V_{\text{REF}}}{k_o} = \left(1 + \frac{R_1}{R_2} \right) V_{\text{REF}}. \quad (5.45)$$

Therefore, the output voltage depends neither on the load current nor on the input voltage of the converter, but only on the reference voltage V_{REF} and the resistance ratio R_1/R_2 .

Example 5.3 If $V_{\text{REF}} = 4 \text{ V}$ and $R_1 + R_2 = 1 \text{ k}\Omega$, determine the R_1 and R_2 so that the output voltage is 5 V .

From (Eq. 5.45) it follows that

$$R_1/R_2 = V_o/V_{\text{REF}} - 1 = 0.2, \text{ so } R_2 = 433 \text{ }\Omega \text{ and } R_1 = 567 \text{ }\Omega.$$

5.3 Current-Controlled PWM

In addition to the voltage control, current control of PWM DC/DC converters is also used. In essence here one has two feedback loops: the voltage and the current one (Fig. 5.10a). The voltage loop acts through the error amplifier to the PWM comparator. The elements of this loop determine the level of the output voltage V_o . The other feedback loop is current-based. It consists of a small (ten to several

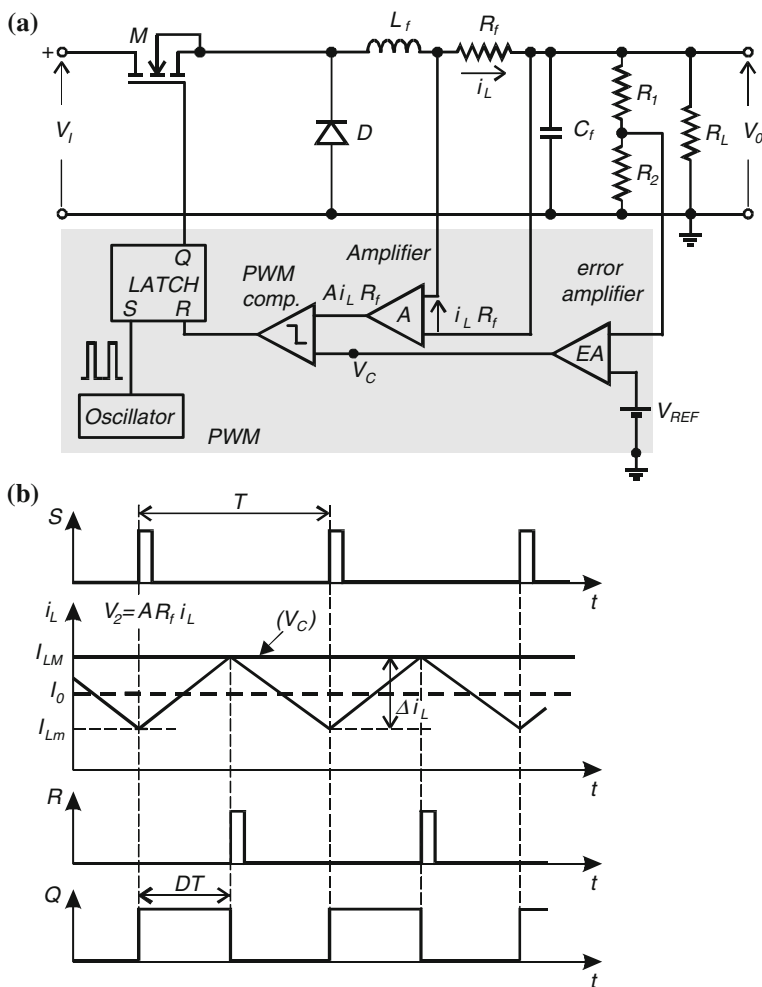


Fig. 5.10 Block diagram of a current-controlled forward converter (a) and the characteristic waveforms (b)

hundreds of $m\Omega$) resistor R_f used as a current sense and a voltage amplifier A . With respect to the voltage PWM control, the amplifier A and the resistor R_f are an equivalent of a generator of auxiliary signals. Consequently, the auxiliary signal is defined as

$$V_2 = AR_f i_L. \quad (5.46)$$

Since the changes of the current i_L are approximately linear, this auxiliary signal is also of a triangular form. An RS latch set by the pulses from a constant frequency ($f = 1/T$) oscillator of rectangular pulses and reset by the output of the PWM

comparator is introduced in order to ensure a constant frequency of control pulses. At the output of the RS latch, the pulses with a cycle T and a width DT , dependent on the output current I_0 , are obtained.

The principle of operation is illustrated by the waveforms of the current through the coil and the characteristic voltages (Fig. 5.10b). A pulse at the S input of the RS latch sets its output to the high level, i.e., $Q = 1$. The transistor M is now on and the diode D is off. With the assumption that the output voltage is constant, the current through the choke L_f will be linear

$$i_L(t) = I_{Lm} + \frac{V_I - V_0}{L_f} t = I_c + m_1 t, \quad (5.47)$$

where

$$m_1 = \frac{di_L}{dt} = \frac{V_I - V_0}{L_f} \quad (5.48)$$

is the slope of the increase in the current i_L , and $I_{Lm} = I_c$ is the minimum current through the choke equal to the minimum control current I_c . As long as $V_2 < V_C$, the output of the PWM comparator is low. When these two voltages become equal, i.e.

$$V_2 = AR_f I_{LM} = AR_f I_c = V_c, \quad (5.49)$$

the output of the PWM comparator becomes high and resets the RS latch. Since $Q = 0$, the transistor M is off and the diode D is on. The current through the choke decreases

$$i_L(t) = I_c - \frac{V_0}{L_f} t = I_c - m_2 t, \quad (5.50)$$

where

$$m_2 = \left| \frac{di_L}{dt} \right| = \frac{V_0}{L_f} \quad (5.51)$$

is the decreasing slope of the current i_L and

$$I_c = I_{LM} = \frac{V_c}{(AR_f)}, \quad (5.52)$$

is the maximum of the control current of the choke. The current i_L will continue decreasing until the next setting pulse. The output current is equal to the mean value of the maximum choke current, i.e.

$$I_o = \frac{I_{LM} + I_{Lm}}{2} = I_c - \frac{\Delta i_L}{2}. \quad (5.53)$$

According to (5.39), (5.52), and (5.53), it can be written that

$$I_o = \frac{V_c}{AR_f} - \frac{1}{2} \frac{V_0}{L_f} (1 - D)T, \quad (5.54)$$

where D is the duty cycle of the control pulses. Therefore, the output current depends on the control voltage V_c . The feedback system controls the output current, so the output could be looked at as a source of controlled current.

The output voltage of the forward DC/DC converter is

$$V_0 = DV_I = I_o R_L \quad (5.55)$$

The second terms in (5.53) and (5.54) are usually negligible, so by combining (5.55), (5.34), and (5.41) one obtains

$$V_0 \approx \frac{V_{REF}}{k_o} = \left(1 + \frac{R_1}{R_2}\right) V_{REF}. \quad (5.56)$$

The result of this brief analysis, expressed by (5.54) and (5.56) shows that in the current-controlled converters, the current feedback controls the output current and the voltage feedback controls the output voltage. The output current and the maximum current through the switch are limited by the current loop and no additional current protection is required. This is one of the advantages of the current-controlled converters over the voltage-controlled ones. It can be shown that the output circuit of a current-controlled converter is a first-order system containing one pole. The maximum phase shift between the control voltage and the output voltage is -90° . The circuit of the feedback loop is very stable and allows simple compensation of the error amplifier. The response to variations of the input voltage and load current is very fast.

A shortcoming of the basic current-controlled PWM is a high sensitivity to noise at duty cycles in excess to 0.5. For this reason, additional compensation is introduced.

5.3.1 Compensated PWM

The problem of instability is solved by introducing a compensation signal V_k which is added to the control voltage (Fig. 5.11). The compensation signal is a negative sawtooth voltage generated by an oscillator and synchronous with the pulses setting the latch. In this way, a linearly decreasing control signal is obtained at the input of the PWM comparator

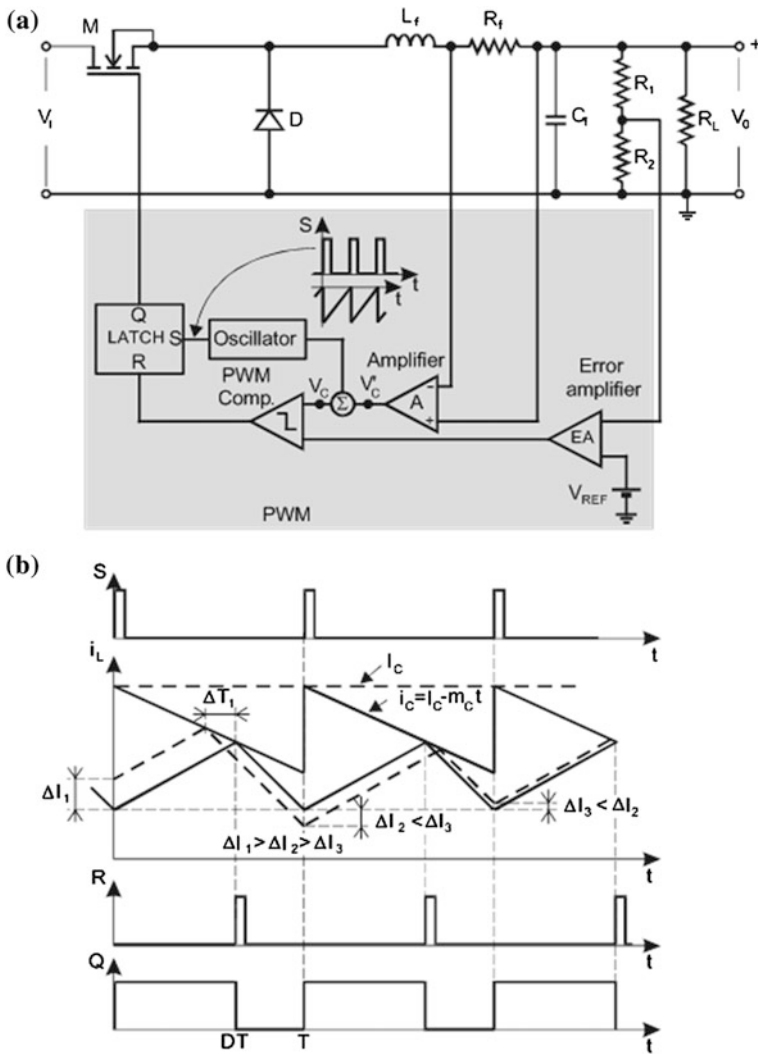


Fig. 5.11 Compensated PWM (a) and the characteristic waveforms (b)

$$v_c = v'_c + v_k = AR_f i_L - \left(\frac{dv_k}{dt} \right) t = V_c - \left(\frac{dv_k}{dt} \right) t \quad (5.57)$$

or

$$i_c = I_c - m_c t, \quad (5.58)$$

where $m_c = (dv_k/dt)/(AR_f)$ is the slope of the control current change.

The characteristic waveforms for $D > 0.5$ are shown in Fig. 5.11. The disturbance ΔI_1 will be suppressed within several cycles. Of course, several conditions have to be satisfied.

From the condition $i_L(DT - \Delta T_1) = i_c(DT - \Delta T_1)$ and using (5.47) and (5.58), it turns out that

$$\Delta T_1 = \frac{\Delta I_1}{m_1 + m_c}. \quad (5.59)$$

On the other hand, ΔI_2 is by $m_c \Delta T_1$ lower compared to the case of an undisturbed control signal, i.e.

$$\Delta I_2 = m_2 \Delta T_1 - m_c \Delta T_1 \quad (5.60)$$

By combining (5.59) and (5.60), one obtains

$$\frac{\Delta I_2}{\Delta I_1} = \frac{m_2 - m_c}{m_1 + m_c}. \quad (5.61)$$

The system will be stable if $\Delta I_2 < \Delta I_1$, thus the stability condition is

$$\frac{m_2 - m_c}{m_1 + m_c} < 1, \quad (5.62)$$

or

$$m_c > (m_2 - m_1)/2. \quad (5.63)$$

For the worst case, when $m_1 = 0$, the stability condition reduces to

$$m_c > \frac{m_2}{2} = \frac{V_0}{2L}. \quad (5.64)$$

With $m_c > m_2/2$, the converter will operate with good stability for any value of the duty cycle within the range $0 < D < 1$.

The preceding analysis of control and stability is valid for the forward DC/DC converters. The mode of control of other converters is the same, and the solution for the stability problem is very similar.

In addition to the already mentioned advantages of the current control compared to the voltage control of DC/DC converters, one should also mention the simple and reliable paralleling of the outputs. Parallel operation is employed when a load current higher than the output current of a single converter is required. Parallel operation of current-controlled converters can be accomplished by using only one error amplifier (Fig. 5.12). The control voltage V_c is common. Independent adjustment of parameters G_1 , G_2 , and G_3 in each of the converters ensures a correct distribution of the load current.

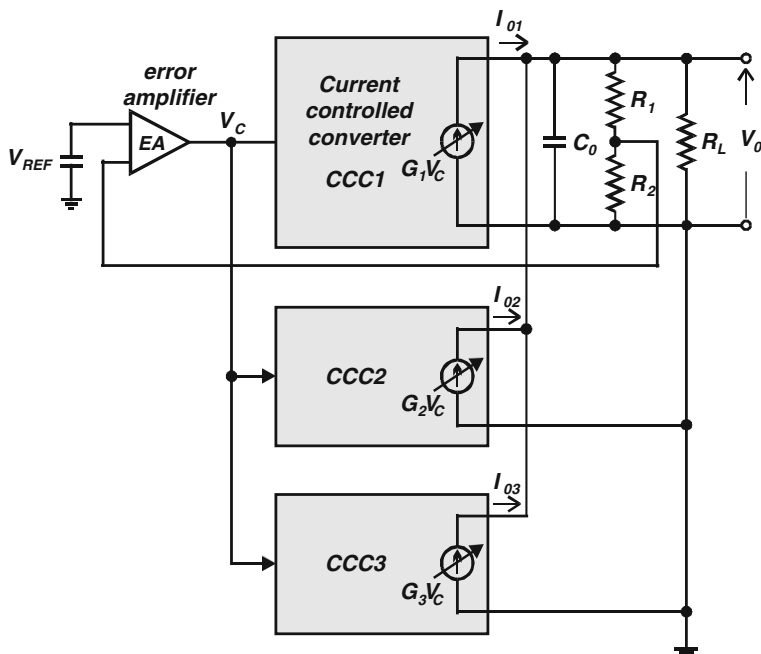


Fig. 5.12 Parallel connection of three current-controlled DC/DC converters

5.4 IC Control Modules

At present, the realization of control modules in the form of integrated circuits is simplified considerably. Several well-recognized families of the monolithic integrated circuits have been produced performing pulse-width modulation which, with addition of several discrete components, achieve very reliable control of DC/DC converters. These circuits differ among themselves in the number of functions they can perform. As a standard, however, they all comprise a PWM comparator, an auxiliary voltage generator (triangular or sawtooth), an error amplifier, a reference voltage source, and one or two outputs. Individually, some include a pulse diode, some current and/or voltage protection, duty cycle limitation, “soft start,” the possibility of shutdown, etc.

Figure 5.13 shows a block diagram of a control module comprising the elements met in the majority of the monolithic circuits of this type.

The aim is to use the model of a hypothetical control module in order to explain the functions of individual sub-modules and the mode of use of the corresponding input terminals. The model is universal and covers all significant sub-modules and functions of the present-day integrated circuits performing control functions. On the basis of this, it is expected that each designer should be able to very quickly understand the possibilities of any IC control module.

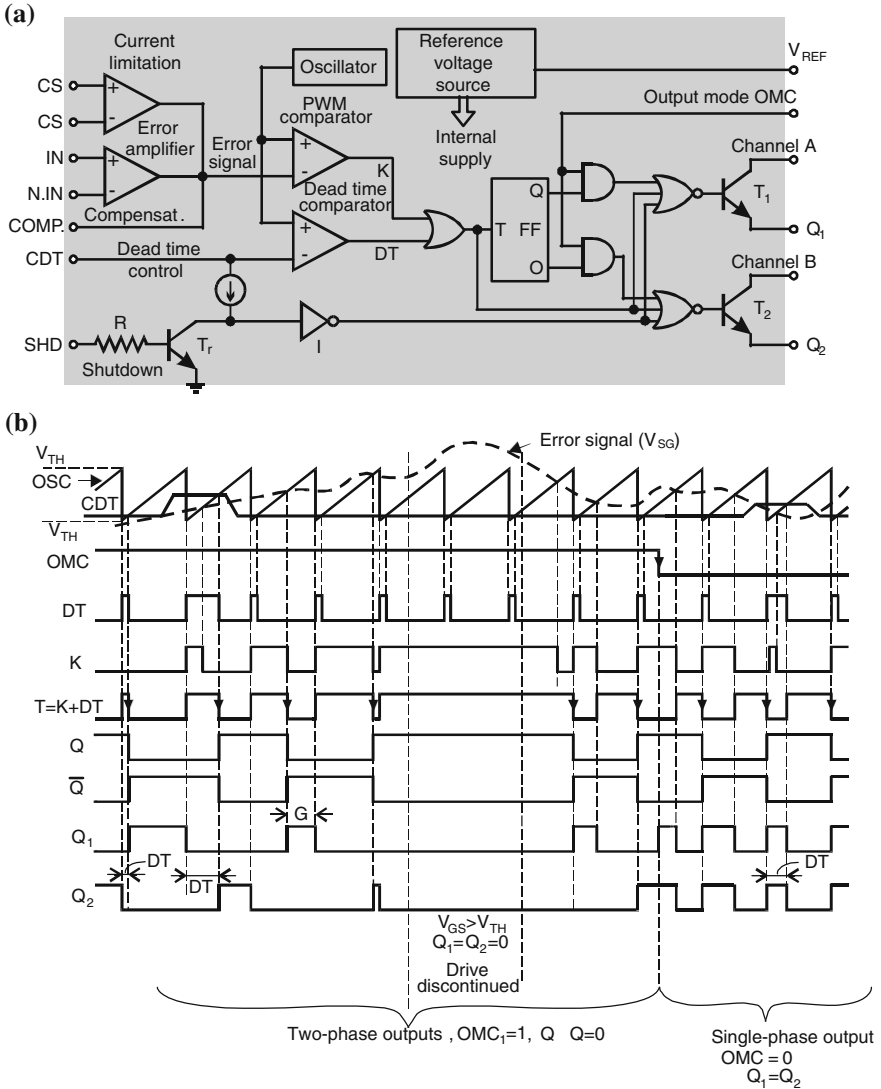


Fig. 5.13 General block diagram of a PWM control module (a) and the voltage waveforms (b)

The PWM comparator and the oscillator (auxiliary signal generator) are the basic parts of a pulse-width modulator. They have been described in the preceding paragraphs.

Phase shifter When two output channels are used individually, like in the push-pull and bridge converters, the output pulses have to be phase shifted so that the power pulse transistors would not be on simultaneously. A phase shifter consists of a *T* flip-flop and two *NOR* logic circuits. When *OMC* = 1, *AND* circuits are

enabled to pass the outputs Q and $\bar{Q}$. The T flip-flop divides by two the PWM frequency. The $NILI$ circuits are enabled by the outputs Q and $\bar{Q}$. During the output pulse at the PWM comparator when $Q = 1$ ($\bar{Q} = 0$), the upper NOR circuit is disabled ($Q_1 = 0 - T_{r1}$ off), and the lower is enabled and the transistor T_{r2} is on until $T = 0$. Within the next cycle, the situation is reversed. Therefore, the cycle of the pulses at the output channels A and B is $T_A = T_B = 2T_0$, and their widths are equal to the duration of the modulated pulses at the output of the OR circuit, i.e., $\tau_{A,B} = \tau$ (see Fig. 5.13b). Since $\tau_{A,B} = T_0$, the maximum duty cycle per channel is $D_{\max} = 50\%$.

Output Mode Control (OMC) The outputs Q_1 and Q_2 could be of the same phase ($Q_1 = Q_2$) as it is required by the converters having only one switching transistor. The output mode (single- or two-phase) is selected through OMC input. If $OMC = 0$, the AND circuits are disabled and they “isolate” the flip-flop from the NOR circuits. The NOR circuits are then acting within the inverter having a common input T so that $Q_1 = Q_2 = T$, and the cycle is $T_A = T_B = T_0$ (Fig. 5.13b). In principle, the maximum duty cycle can be $D_{\max} = 100\%$. In this mode, the emitters and the collectors of the transistors T_{r1} and T_{r2} are connected in parallel. This doubles the output current.

Dead-Time Comparator (DTC) limits the maximum duty cycle so that always $D_{\max} < 100\%$. In the single-phase mode, it limits the minimum off time of the transistors T_{r1} and T_{r2} to a value higher than the maximum off time of the switching transistors of the pulse voltage converters. It is usually assumed that $t_{DT} = 4\% T_0$ meaning that the maximum duty cycle is $D_{\max} = 96\%$. In the two-phase mode, DTC determines the maximum phase shift. This is necessary in order to avoid, for example, that the power switching transistors in a push–pull circuit are on simultaneously. The dead time t_{DT} is adjusted by the voltage V_{DT} at the “+” input of DTC . This voltage has to be within limits

$$V_{TL} < V_{DT} < V_{TH}, \quad (5.65)$$

where V_{TL} and V_{TH} are the minimum and maximum sawtooth (triangular) voltages of the oscillator. If I is the current charging the timing capacitor C_t of the oscillator, then

$$t_{DT} = C_t \frac{V_{DT} - V_{TL}}{I}. \quad (5.66)$$

For $t_{DT}/T = 0.04$, from (5.29) and (5.66) one obtains

$$V_{DT} = V_{TL} + 0.04 V_H. \quad (5.67)$$

The voltage V_{DT} is fed to DTC input from the output of the reference voltage generator via a resistive divider. New generation ICs , however, have a built-in V_{DT} source as the voltage offset of the dead-time comparator. This voltage determines the minimum dead time (maximum duty cycle) and the additional control

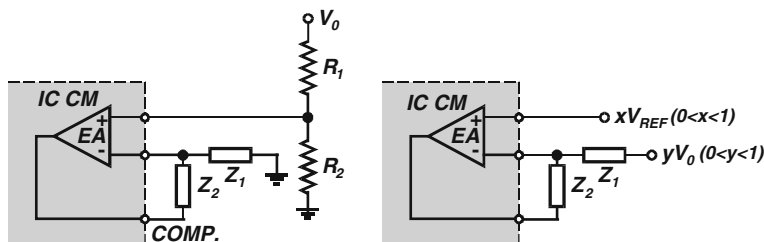


Fig. 5.14 Possible connections of the error amplifier

(amplification) is accomplished by the external elements at *DTC* input (usually a resistive divider supplied by V_{REF}).

Error amplifier (EA) serves to amplify the output voltage variation. Depending on the specific application (type of the pulse converter), *EA* can be inverting or non-inverting. In the inverting connection (Fig. 5.14), a part of the output voltage is fed to the + input of the amplifier. The impedances Z_1 and Z_2 in the feedback loop define the gain and stability of the amplifier. Z_1 and Z_2 are usually of resistive—capacitive type.

The currents of power converters are very high. Their pulse character is the source of both inductive and capacitive disturbances. For this reason, it is often required that the output part of the converter is galvanically separated from the control part. Without this, it would be difficult to realize a stable feedback system including the control module. The galvanic separation is accomplished either by a transformer or by an opto-coupler. In the case of an opto-coupler, care should be taken of the breakdown voltages of the diode and the transistor of the opto-coupler and of the thermal instability of the photo-current. The opto-coupler operates in the linear mode. Figure 5.15 shows an example of galvanic separation by an opto-coupler. The temperature stabilization is realized by a current generator comprising the transistor T_{r1} , the Zener diode Z_1 , and the resistor R_3 . The transistor also serves as an amplifier. The low-pass filter R_1 — C_1 increases the stability. The potentiometer R_0 adjusts the operating point in order to obtain an optimum intensity of the diode light.

A simpler but more expensive solution (Fig. 5.16) includes feeding of the photo-diode by a special shunt controller *TL431* (Fig. 5.17). The controller comprises an internal 2.5 V voltage reference. It could be supplied by a 5-V source, and the output voltage can be programmed externally up to 36 V. Its temperature coefficient is very small (50 ppm/°C). The resistor R_6 and the capacitor C_2 (Fig. 5.16) allow frequency compensation.

Current Limit (CL) Over-current protection is accomplished by a CL comparator connected as shown in Fig. 5.18. The threshold voltage of the comparator, V_t , is typically between 100 and 200 mV. Let I_p be the maximum permitted current of the pulse transistor T_{r1} . With $R_s I_p < V_t$, the output of the comparator is passive. If $R_s I_p > V_t$, the output of the comparator CL is changed. It blocks the output stage of the control module (T_1 and T_2 in Fig. 5.13a) through the PWM comparator. The resistance R_s which initiates the protection action is therefore $R_s = V_t / I_p$.

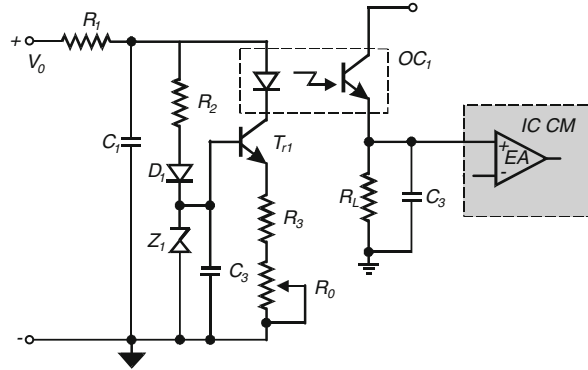


Fig. 5.15 Separation by an opto-coupler

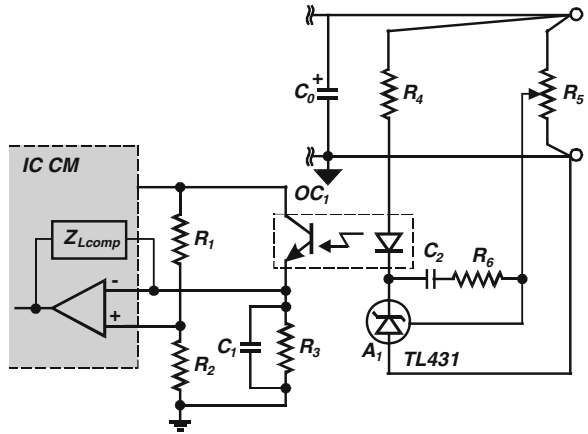


Fig. 5.16 Galvanic isolation having LED driven by shunt controller TL431

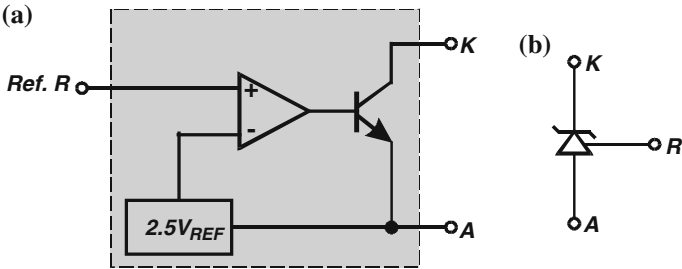


Fig. 5.17 Block diagram (a) and symbol of programmable controller TL431 (b)

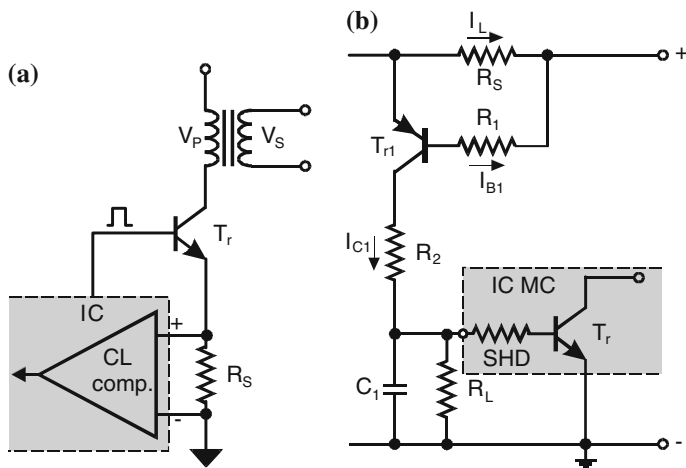


Fig. 5.18 The circuit of the current protection comparator (a) and the additional protection of the output (b). SHD is the shutdown input

Let $V_t = 200$ mV and $I_p = 5$ A. Then $R_s = 0.04$ Ω . The comparator CL can operate in the linear mode if a resistor is connected between its input and output. In this way, the converter can be controlled by using the so-called current programming technique. The current sense R_s (Fig. 5.18) is placed in the circuit of the switching transistor and controls its current. However, the input and the output parts are often galvanically separated. The output ground is then separated from the ground of the control circuit. Then the current limit sense can be connected directly to the output (Fig. 5.18b). In the normal operating mode, the current I_L is lower than the maximum permitted current, the transistor T_{r1} is off, and the protection circuit is passive. The protection is activated at the current $I_{L\max}$ when

$$I_{L\max} R_s = V_{BE1} + I_{B1} R_1. \quad (5.68)$$

The transistor T_{r1} is turned on, which leads to turning on of the transistor T_r at the input of the shutdown. The capacitor C_1 serves for filtering out random shutdowns caused by pulse disturbances. When T_r is off, C_1 is discharged through the resistor R_1 . The output is in this way protected against over-current and short circuit. It should be stressed that both protection techniques shown in Fig. 5.18 may be used in a single converter.

As a rule, R_s is inserted in a high-current branch. Therefore, the resistors of this type have to be very powerful. This may cause problems in powerful converters where a transistor is used as the comparator (Fig. 5.18b), because the threshold voltage $V_t = V_{BE} \approx (0.6 - 0.7)$ V is quite high. If there are problems with the resistor R_s , the use of a pulse transformer as the current sense is recommended (Fig. 5.19). The current transformer T_1 detects the over-current conditions. Since only the primary windings of the current transformer are in the high-current branch, where

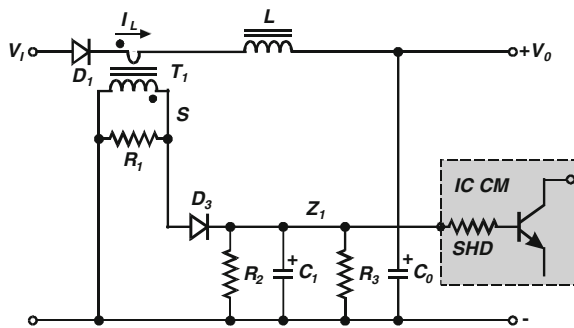


Fig. 5.19 Over-current protection circuit using current transformer T_1

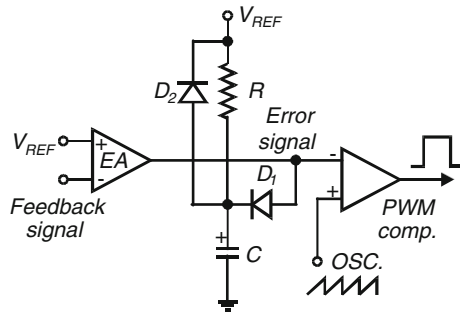
the power losses are negligible, this type of protection is often called non-dissipative. Across the resistor R_1 in the secondary winding of the transformer, a voltage $V_s = I_s R_1$ is developed (I_s is the secondary current). The diode D_3 , the resistor R_2 , and the capacitor C_1 rectify and filter-out the voltage V_s . When the rectified voltage becomes $V_s = V_z + V_{BE}$, the Zener diode Z_1 and the transistor T_r are turned on. Since the transistor T_r is in the shutdown circuit, the converter will be turned off.

If n_p and n_s are the numbers of turns of the primary and secondary windings, respectively, then $n_p/n_s = I_s/I_p$, which allows the determination of the number of turns of the secondary winding so that current protection is activated at the primary current I_{pmax}

$$n_s = n_p \frac{R_1 I_{pmax}}{V_{z1} + V_{D3} + V_{BE}} a_f, \quad (5.69)$$

where a_f is the correction factor of the $R_2 C_1$ filter. Of course it is possible that $n = 1$.

Soft-Start Circuit It is often required, particularly for powerful converters, to introduce a certain delay in entering the steady-state operation mode in order to avoid instantaneous current and/or voltage strikes and the transformer saturation problems at turn-on. A standard circuit for the soft-start consists of an RC net which gradually introduces the control module to the operation mode (Fig. 5.20). When the power supply is turned on, the capacitor C is empty, and the PWM comparator is blocked. The input voltage of the comparator increases exponentially, and the pulses at its output gradually increase. When the capacitor is charged, the diode D_1 separates the output of the error amplifier from the capacitor. In case of a temporary turning off of the converter, the diode D_2 allows a quick discharge of the capacitor. In this way, the capacitor is prepared so that after a brief interruption it can gradually introduce the converter to the normal mode of operation. New IC families of control modules have the resistor R replaced by an internal current source. Then, the soft-start function is accomplished by the capacitor as the only external circuit element.

Fig. 5.20 Soft-start circuit

Shutdown Through this input, the converter is forcibly turned off by discontinuing the drive generated by the control module. Practically, this function is accomplished by the transistor T_r . Normally, T_r is off and the output of the inverter I is low and does not have any influence on the outputs Q_1 and Q_2 . If the base of T_r is turned on, the transistor will go into saturation. The output of I is now high, so the transistors T_1 and T_2 are off ($Q_1 = Q_2 = 0$) irrespective of the DT, K, and OMC. In this way, the drive provided by the control module is discontinued.

Example 5.4 Determine the current I_L of the protection circuit in Fig. 5.18b at which the shutdown circuit is activated if $R_s = 0.2 \Omega$, $R_1 = 200 \Omega$, $V_{EB1} = 0.7 \text{ V}$, $\beta_1 = 50$ and $V_{BEt} = 0.7 \text{ V}$.

The shutdown circuit is activated when the transistor T_r starts to lead, i.e., at

$$I_{C1}R_L = \beta_1 I_{B1}R_L = V_{BEt} = 0.6 \text{ V}. \quad (5.70)$$

The transistor T_{r1} starts to lead before the transistor T_r , so from (Eq. 5.68) it follows that

$$I_{B1} = \frac{I_{L\max}R_s - V_{EB1}}{R_1}. \quad (5.71)$$

From (5.68) and (5.69) it follows that

$$I_{L\max} = \frac{1}{R_s} \left(V_{EB1} + \frac{R_1}{\beta_1 R_L} V_{BEt} \right) \approx \frac{V_{EB1}}{R_s} = \frac{0.7 \text{ V}}{0.2 \Omega} = 3.5 \text{ A}$$

5.4.1 Control Module TL494

A typical example of a PWM constant frequency control module is IC TL494 whose block diagram is shown in Fig. 5.21. Since this block diagram is very similar to the general block diagram (Fig. 5.13), only the peculiarities of IC TL494 will be mentioned.

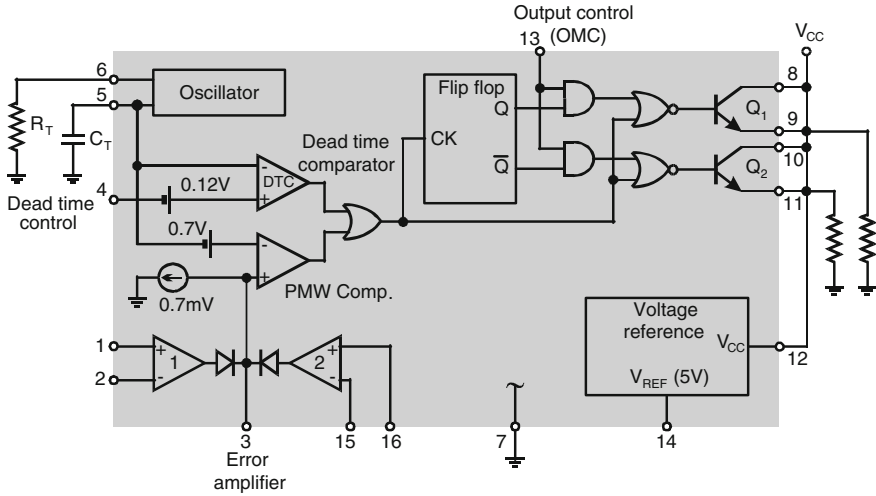


Fig. 5.21 Block diagram of control module TL494

The oscillator generates the auxiliary sawtooth voltage when the timing elements, the capacitor C_T and the resistor R_T , are connected to the terminals 5 and 6. The oscillator frequency is determined by

$$f_o = 1.1/(R_T C_T). \quad (5.72)$$

The internal offset of the dead-time comparator is 0.12 V, which determines the minimum dead time to 4 % of the cycle of the oscillator. This means that the maximum duty cycle for the single-phase output (OMC = 0, i.e., $V_{13} = 0$) is 96 and 48 % for the two-phase mode (OMC = 1). Then, the input 4 is connected to the negative pole of the input voltage by a several k Ω to 10 k Ω resistor. When the dead time should be increased, the input 4 is connected to a resistive divider fed by the output of the voltage reference. The voltage V_4 can be varied from 0 to 3.3 V.

The PWM comparator contains a built-in 0.7-mA current source, which provides a soft start. The non-inverting input of this comparator is driven by the outputs of two error amplifiers. One of the amplifiers brings the error signal to the output of the DC/DC converter and the other may serve as the current limit. Figure 5.22 shows one of the possible ways of setting (“programming”) the output voltage. The resistors R_1 and R_2 set the quiescent operating point of the error amplifier. By equating the currents through these two resistors, since $V_1 = V_2$, the positive output voltage (Fig. 5.22a) is determined by

$$V_0 = \left(1 + \frac{R_1}{R_2}\right) V_{\text{REF}}, \quad (5.73)$$

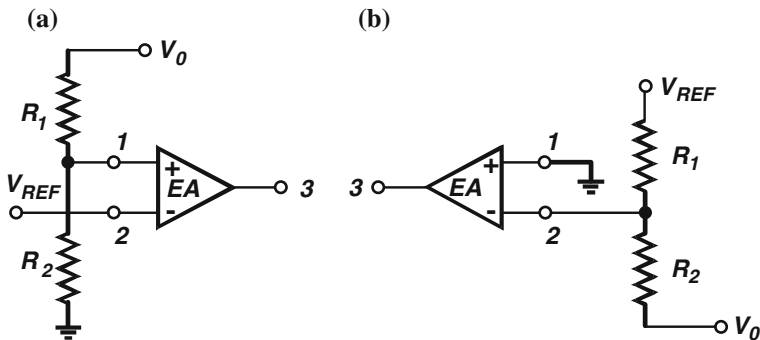


Fig. 5.22 Setting the output voltage: positive (a) and negative (b)

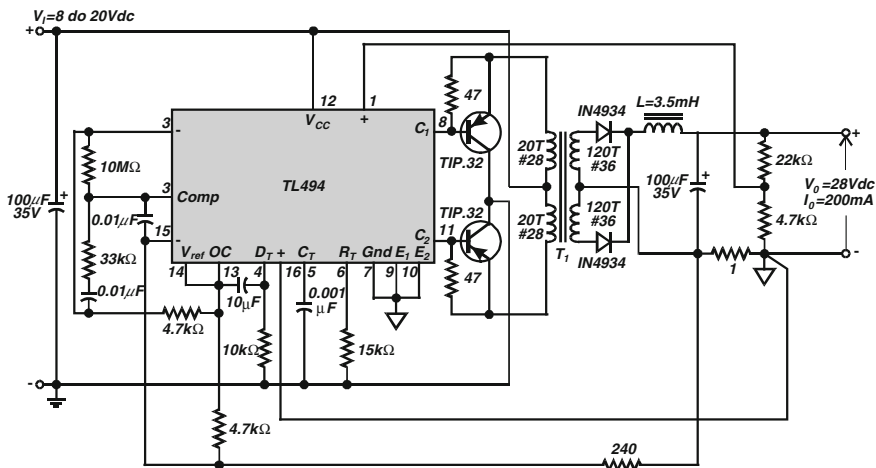


Fig. 5.23 Typical application of IC TL494 in a push-pull voltage converter [1]

and the negative (Fig. 5.22b) by

$$V_0 = -\frac{R_1}{R_2} V_{REF}. \quad (5.74)$$

The dynamics of the error signal is determined by the elements of the negative feedback circuit (between terminals 2 and 3) which determine the gain and stability of the error amplifier.

An example of a push-pull pulse voltage converter illustrating the method of connecting IC TL494 is shown in Fig. 5.23.

On the basis of TL494, a whole family of the control module integrated circuits has been developed. For example, Unitrode is manufacturing the family UC493A,

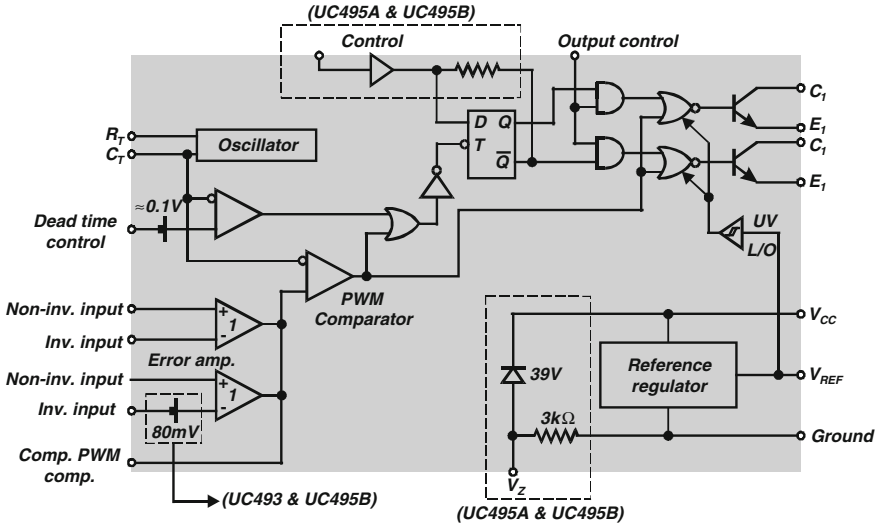


Fig. 5.24 General circuit diagram of the family UC493, UC494, and UC495

UC493AC, UC494A, UC494AC, UC495A, UC495AC, UC495B, UC495BC, which is an advanced version of the basic circuit TL494. Additional letters A and B denote the extended temperature range (-55 up to $+125$ °C) and AC and BC the industrial temperature range (0 up to $+70$ °C).

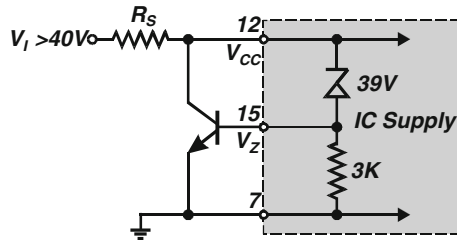
In the general block diagram of the circuits UC493, UC494, and UC495 (Fig. 5.24), the parts specific only for some of the circuits are clearly marked. For instance, UC493 and UC495B at the input of one of the error amplifiers have an 80-mV built-in voltage offset. When this amplifier is used as the over-current protection comparator, the resistance of the current sense $R_s = 0.08/I_M$ [Ω] (I_M is the maximum current in the controlling branch) is seven to eight times lower compared to the situation when R_s is connected between the base and the emitter of the transistor. Only the control modules UC495A and UC495B have additional output control and over-voltage protection. The additional output control at the input is as follows.

Steering Control (SC) is via a synchronized D flip-flop when SC exists and via a non-synchronized T flip-flop ($D = Q$) when SC does not exist. For instance, when $OC = 1$, for $SC = 0$ only the output transistor T_{r1} is enabled, whereas for $SC = 1$ only T_{r2} is enabled.

Example 5.5 For the push–pull converter shown in Fig. 5.23 it is necessary to:

- Determine the oscillator frequency of the control module TL494.
- Determine the minimum dead time that the controller can generate.
- If the reference voltage is $V_{REF} = 5\text{ V}$ and the resistor $R_1 = 20\text{ k}\Omega$, determine the resistance of resistor R_2 so the output voltage is 24 V .

Fig. 5.25 IC supply when $V_I > 40$ V



- (a) The oscillator frequency is determined by $f_o = 1.1/R_T C_T$. Since $R_T = 1\text{ nF}$ and $R_T = 15\text{ k}\Omega$, it follows $f_o = \frac{1.1}{15 \times 10^3 \times 10^{-9}} = 73.3\text{ kHz}$.
- (b) The minimum dead time is 4 % of the oscillator cycle, so

$$T_{\text{TD}} = 0.04/f_o = 0.545\text{ }\mu\text{s}.$$

- (c) The positive output voltage (Fig. 5.22a) is determined by $V_0 = \left(1 + \frac{R_1}{R_2}\right) V_{\text{REF}}$.
So, $R_2 = \frac{R_1}{\frac{V_0}{V_{\text{REF}}} - 1} = 5.26\text{ k}\Omega$.

The over-voltage protection is used in high-voltage applications ($V_I > 40$ V) (Fig. 5.25). When $V_I > 40$ V, the Zener diode is operating and the IC supply voltage is $V_{\text{CC}} = V_Z + V_{\text{BE}} \approx 39.7$ V.

All circuits shown in Fig. 5.24 are provided with the under-voltage lockout (UV L/O) shutdown. When the input voltage is below the upper threshold of the Schmitt trigger, the IC is off. The upper threshold is 3.5 V minimum, usually 6.5 V. The voltage hysteresis is about 300 mV.

5.4.2 Control Module SG1524/2524/3524

When it had been manufactured, IC SG1524 (Fig. 5.26) became the standard in this area. Currently, it is being manufactured by several integrated circuits manufacturers. It comprises almost all the elements (blocks) required for an efficient control of the pulse converters.

The dead time of IC SG1524 is determined by the duration of the pulses at the oscillator output (Fig. 5.26b). In principle, the oscillator is realized as shown in Fig. 5.5, thus the duration of the positive pulse is determined by the discharging time of the capacitor C_T , approximately given by (5.32). Within that time, both NOR circuits at the output are disabled (their outputs are low irrespective of other inputs) so that the output transistors have no drive. This is, therefore, the dead time t_{DT} . Its dependence on C_T (Fig. 5.27c) ranges from 0.5 up to 3 μs .

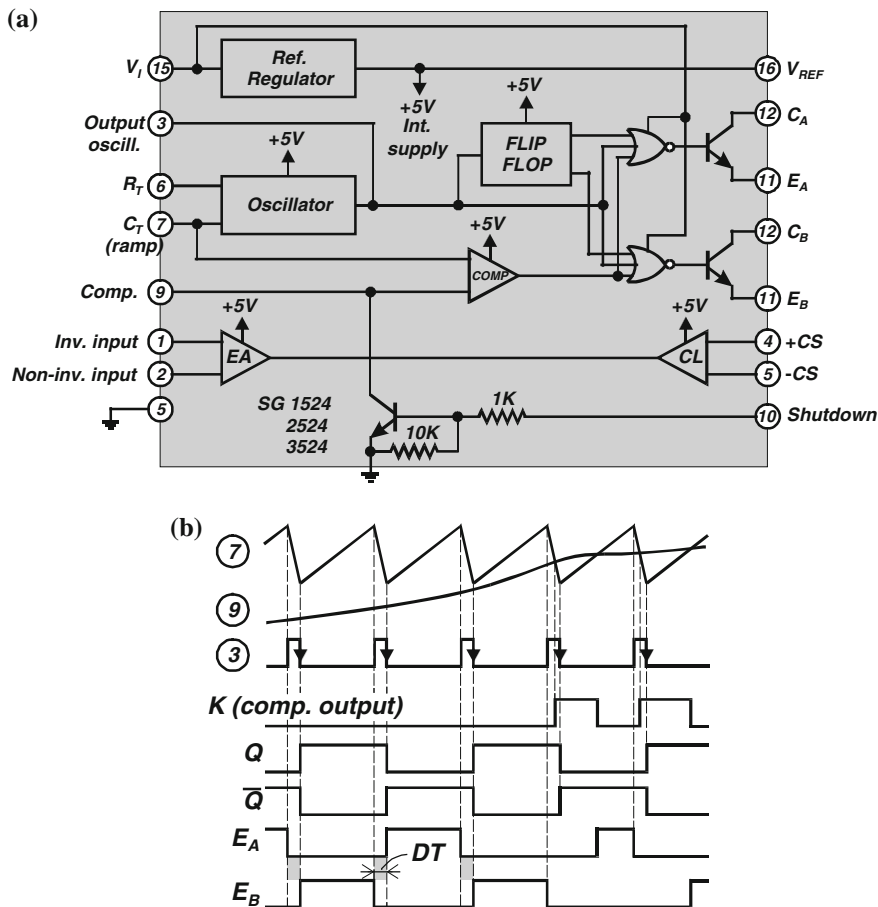


Fig. 5.26 Block diagram of control module SG1524 (temperature range -55 up to $+125$ °C), SG2524 (-25 up to 85 °C), and SG3524 (0 up to 70 °C) (a) and the characteristic waveforms illustrating dead-time appearance (b)

The maximum duty cycle per output is 45 %. If t_{DT} should be increased, connecting a 100-pF capacitor between the terminal 3 and ground is recommended. If this is not sufficient, the limitation of the maximum duty cycle (increase of t_{DT}) can be accomplished by limiting the voltage at the output of the error amplifier (Fig. 5.27d).

The oscillator frequency is approximately given by

$$f \approx \frac{1.18}{R_T [\text{k}\Omega] C_T [\mu\text{F}]} [\text{kHz}], \quad (5.75)$$

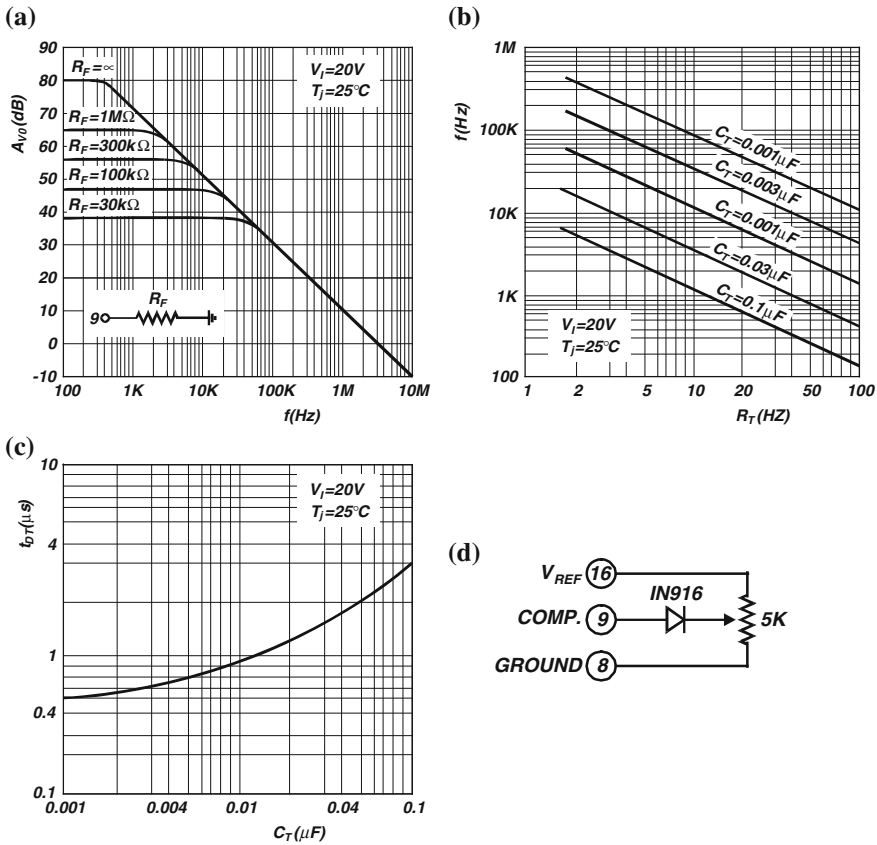


Fig. 5.27 Frequency characteristic of the error amplifier (a), oscillator frequency as function of timing elements C_T and R_T (b), dead time as function of C_T (c), and a possibility of increasing t_{DT} (d)

and its dependence on the timing elements is shown in Fig. 5.27b. The practical values of the capacitance C_T are within limits $0.001 \mu F < C_T < 0.1 \mu F$ and resistance $1.8 k\Omega < R_T < 100 k\Omega$. This provides a frequency range from 120 Hz up to 500 kHz. An external synchronization of pulses by approximately 3 V can be realized via the terminal 3. The resistance of this terminal with respect to ground is approximately 2 k Ω . The time constant $C_T R_T$ has to be chosen so that the internal cycle is somewhat longer than the cycle of the synchronizing pulses.

When synchronous operation of several modules SG1524 is required, the outputs of all oscillators have to be connected together, all terminals for C_T have to be connected together with one timing capacitor connected to the common terminal, and one timing resistor connected to one of the R_T terminals. The remaining R_T terminals may be left open or connected to V_{REF} .

The frequency characteristic of the error amplifier (Fig. 5.27a) depends on the value of the resistor R_F connected between the terminal 9 and ground. When

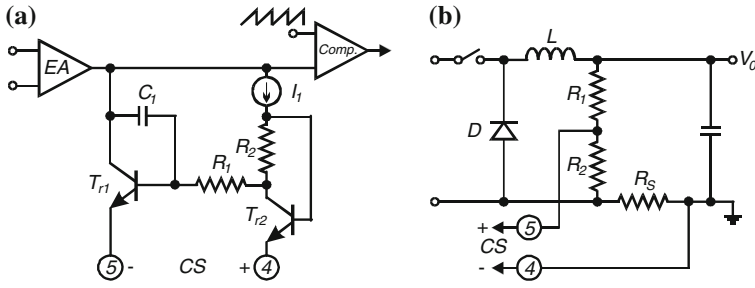


Fig. 5.28 Current limiting circuit (a) and current limitation having a foldback characteristic (b)

$R_F < 30 \text{ k}\Omega$, the limitations on the maximum value of duty cycle arise (increased t_{DT}). The unity gain is at frequency $f_T = 2 \text{ MHz}$.

The current sense R_s of the circuit for current limitation (Fig. 5.28a) is inserted between the terminals 4 and 5. The current limitation arises when the transistor T_{r1} is turned on. If the voltage drop across R_1 is neglected ($I_{B1} \ll I_{C2}$) and because $I_{B2} \ll I_{C2}$, the threshold voltage (initiation of the current protection) is

$$V_{45t} = V_{OS} = -V_{BE2} + R_2 I_1 + V_{BE1} = R_2 I_1 = 200 \text{ mV}.$$

R_1 and C_1 are the compensating elements. One of the terminals for the current limitation may be grounded. For instance, if the terminal 5 is grounded, the terminal 4 is used as an additional terminal for the shutdown. Namely, if the terminal 4 is left open, then the output will be shutdown ($I_{B1} = I_1$ and T_{r1} is in saturation) and when it is grounded, the output is enabled since T_{r1} is off ($V_{BE1} = -I_1 R_2 + V_{BE} \approx -0.2 \text{ V} + 0.4 \text{ V} = 0.4 \text{ V} < V_{BE1}$). For the current limiting circuit having a foldback characteristic (Fig. 5.28b)

$$V_{BE1} = -V_{OS} + V_{BE2} - \frac{R_2}{R_1 + R_2} V_0 + I_m R_s, \quad (5.76)$$

where I_m is the current through R_s when T_{r1} is turned on and $V_{OS} = 0.2 \text{ V}$. Since $V_{BE1} \approx V_{BE2}$, then

$$I_m = \frac{1}{R_s} \left(V_{OS} + \frac{R_2}{R_1 + R_2} V_0 \right). \quad (5.77)$$

In this way, the short-circuit current is

$$\frac{I_m}{3} < I_{sc} = \frac{V_{OS}}{R_s} < I_m \quad (5.78)$$

Figure 5.29 shows a typical application of IC SG3524 in a push–pull DC/DC converter 160 V/+50 V, 100 W. The soft-start elements are separately shown.

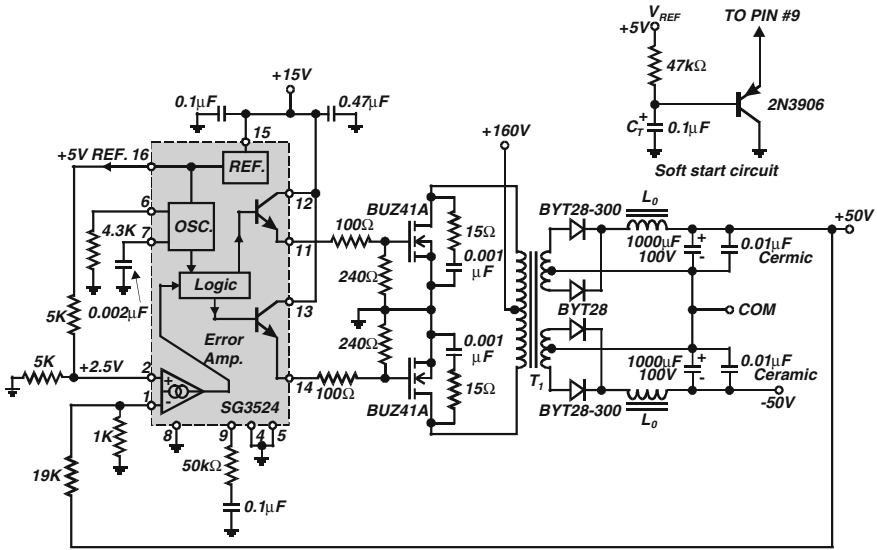


Fig. 5.29 Push-pull converter using IC SG3524

Terminals 4 and 5 for current limitation have not been used here. The switching transistors are MOS power transistors BUZ41A. The driving pulse frequency is 50 kHz and the oscillator frequency 100 kHz.

The input and output stages of a specific Čuk converter using SG1524 (IC₁) are separated by the transformer T and the opto-coupler IC₂.

The peculiarity of this converter (Fig. 5.30) is that the output voltage could be higher, lower, or equal to the input voltage. Namely, $V_0 = 12$ V, while the input voltage varies from 10 to 40 V. This has been achieved owing to the fact that the control module operates as a pulse-width and a pulse-frequency modulator simultaneously. This is accomplished by replacing the resistor at terminal 6 by a voltage-to-current converter (T_{I6} , R_{11} , R_{12} , and R_{13}). The charging current of the timing capacitor $C_T = C_6$ is now

$$I_{C6} = \frac{V_I - (1 + R_{13}/R_{12})V_{BE}}{R_{13} + R_{11}(1 + R_{13}/R_{12})}, \quad (5.79)$$

and according to (5.29) the oscillator frequency is

$$f_o \approx \frac{I_{C6}}{C_9 V_H} \quad (5.80)$$

a linear function of the input voltage. $V_H = 3$ V is the swing of the sawtooth voltage. By varying the input voltage from 10 to 40 V, the frequency varies from 25 to 160 kHz. The resistor R_{11} should be $R_{11} > 3$ kΩ to ensure a reliable start of the

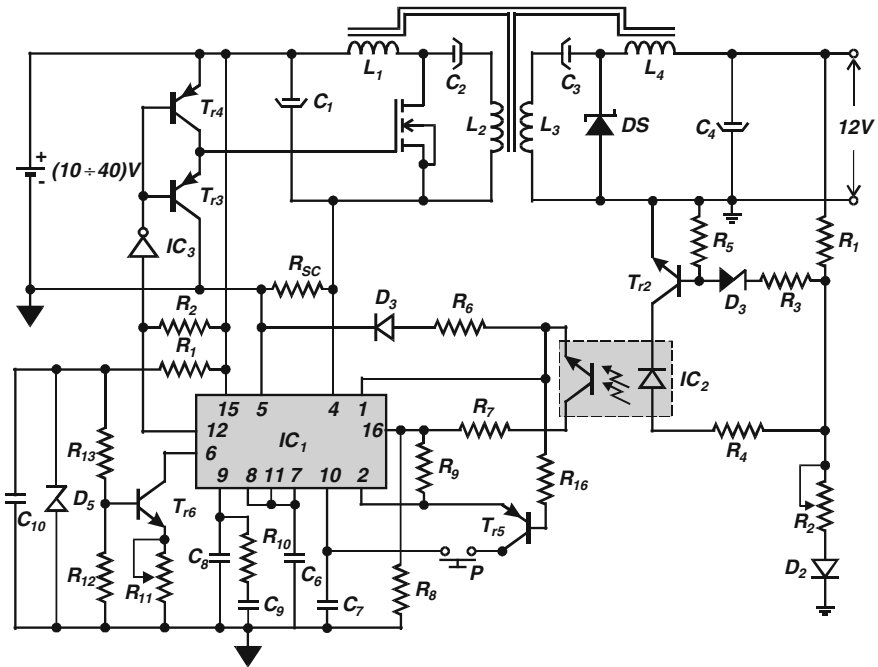


Fig. 5.30 Čuk converter 10–40 V/12 V, 1.5 A having separated input from output

oscillator. The current sense, $R_{sc} = 0.06 \Omega$, is placed in the input circuit, so the base current is limited to $I_{sc} = 200 \text{ mV}/R_{sc} = 3 \text{ A}$. For the purpose of avoiding source overload due to output short circuit, the shutdown input (terminal 10) is used. Namely, when $V_0 = 0$, the transistor T_{r5} is turned on which turns off the control module so the source is not loaded. The restart, after removing the short circuit, is accomplished by the push button P.

The grounds of the output and control parts are galvanically separated by the opto-coupler IC_2 . The LED of the opto-coupler is in the collector circuit of T_{r2} which together with the resistors R_3 and R_5 and the diode D_3 constitutes a current source.

The variations of temperature from -30 up to $+55^\circ \text{C}$, the input voltage from 10 to 40 V, and the load current up to 1.5 A will cause the output voltage variations to be less than 100 mV.

The coefficient of efficiency over the entire operating range is no less than 70 %. The converter in Fig. 5.30 is specifically developed for battery supplied equipment when a stable 12-V voltage is required. The battery voltage is $12 \text{ V} \pm 10 \%$.

Example 5.6 For the push–pull converter with IC SG3524 control module shown in Fig. 5.29 determine

- (a) the oscillator frequency of the control module SG3524,
 - (b) the resistors in the feedback branch so the output voltage is 25 V, and
 - (c) the resistance of the resistor R_S , so the short-circuit current is 2 A. Define the maximum value of the load current.
- (a) The oscillator frequency is determined by $f_o = 1.18/R_T C_T$. Since $R_T = 2 \text{ nF}$ and $R_T = 4.3 \text{ k}\Omega$, it follows

$$f_o = \frac{1.18}{4.3 \times 10^3 \times 2 \times 10^{-9}} = 137 \text{ kHz}.$$

- (b) Input voltages on the connectors 1 and 2 should be equal. The voltage $V_2 = 2.5 \text{ V}$ and $V_1 = \frac{V_0 R_2}{R_1 + R_2}$ (Fig. 5.29). If we put $R_2 = 1 \text{ k}\Omega$, then $R_1 = R_2 \left(\frac{V_0}{V_2} - 1 \right) = 24 \text{ k}\Omega$.
- (c) The short-circuit current can be calculated from the protection circuit as $I_{SC} = \frac{V_{OS}}{R_S}$. The voltage V_{OS} is equal to 0.2 V, so $R_S = \frac{V_{OS}}{I_{SC}} = \frac{0.2}{2} = 0.1 \Omega$. The maximum load current and the short-circuit current are related by the following inequality

$$\frac{I_m}{3} < I_{sc} = \frac{V_{os}}{R_s} < I_m,$$

so $I_m < 6 \text{ A}$.

5.4.2.1 Advanced Circuits

The second generation of modules SG1524 is the advanced module UC1524A (Fig. 5.31) pin-to-pin compatible with the basic module 1524 not “A” suffixed. The internal structure has been improved, resulting in an increased functionality and simplified application. Only these improvements will be described here.

This module has a block for the under-voltage shutdown (Fig. 5.32a). The current transfer characteristic of this block is shown in Fig. 5.32b. Through the open-collector transistor, which constitutes current mirrors together with the transistors T_{r4} and T_{r5} , the supply is provided for the output stage, oscillator, amplifiers, and PWM comparator. The current mirrors are driven by the output of the Schmitt trigger whose basic element are the transistors T_{r2} and T_{r3} and the resistors R_2 , R_3 , and R_4 . When the input voltage is below the upper threshold voltage of the Schmitt trigger, determined by

$$V_{TH} = V_{Z1} + V_{BE2} + R_3 \frac{(R_2 + R_u)V_{REF} - R_2 V_{CES3} - R_4 V_{BES3}}{R_2 R_4 + R_3(R_2 + R_4)} \approx 8 \text{ V}, \quad (5.81)$$

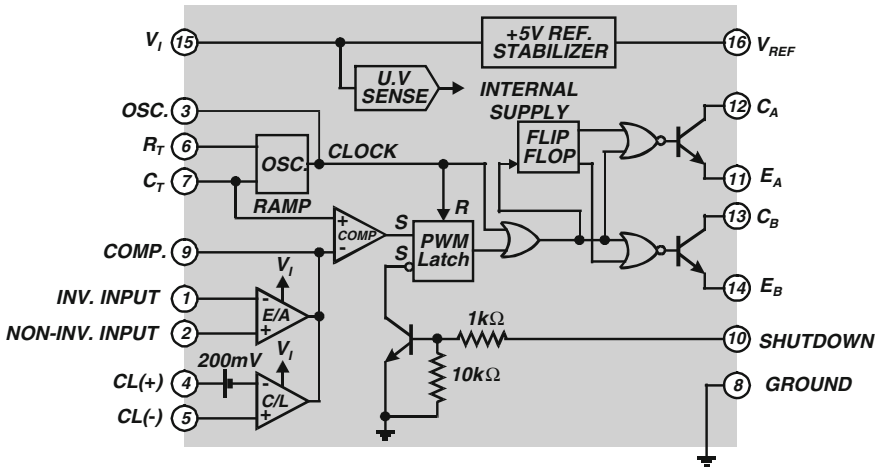


Fig. 5.31 Block diagram of control module UC1524A

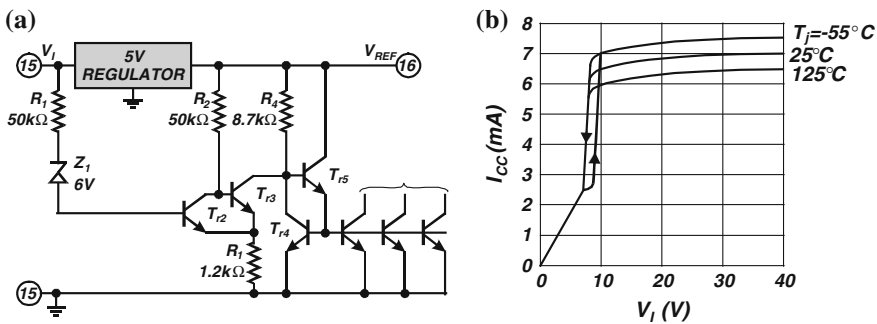


Fig. 5.32 Under-voltage shutdown block (UV SENSE or UV L/O) (a) and its current transfer characteristic (b)

T_{r3} is in saturation, the transistors of the current mirrors are off and so is the supply of the blocks feeding the current mirrors. Therefore, only for $V_I > 8$ V the supply for all blocks is provided. Then T_{r2} is in saturation and T_{r3} is off. During decreasing of the input voltage the current mirrors will be turned off when the input voltage becomes equal to the lower threshold of the Schmitt trigger. Then, T_{r3} is turned on and goes to saturation, whereas T_{r2} is turned off. Since at $V_I = V_{TL}$ T_{r2} is in the active region, it follows that

$$V_{TL} = V_{Z1} + V_{BE2} + \frac{R_3 + R_1/(1 + \beta_2)}{R_3 + \alpha_2 R_2} (V_{CC} - V_{BE13}) \approx 7.4 \text{ V}, \quad (5.82)$$

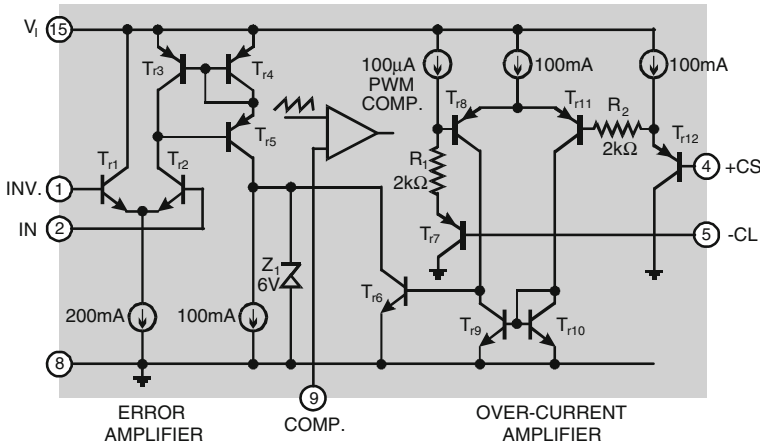


Fig. 5.33 Basic scheme of error amplifier and over-current limiter

where α_2 is the common-base current gain of T_{r2} . The voltage hysteresis is $V_H = V_{TH} - V_{TL} = 60$ mV.

The error amplifier (Fig. 5.33) is almost the same as in the earlier version of 1524. The difference is only that it is now supplied by V_I instead of by V_{REF} . In this way, the range of the input voltage of the amplifier is extended to $V_I - 2$ V. The output voltage of the amplifier is limited by the Zener diode Z_1 to the value $V_9 \leq 6$ V. The over-current amplifier (Fig. 5.33) through R_1 has a built-in voltage offset $V_{OS} = R_1(100 \mu A) = 200$ mV. As long as the voltage between the terminals 4 and 5 $V_{45} < 200$ mV, T_{r8} is off and so is T_{r6} . The PWM comparator is then controlled only by the outputs of the oscillator and error amplifier. When $V_{45} > 200$ mV, T_{r11} will be off and T_{r8} on. Since via the current mirror $T_{r9} - T_{r10}$, $I_{C9} = 0$, $I_{CS} = I_{bb}$, so T_{r6} is on and reduces the voltage at the input of the PWM comparator. The duty cycle of output pulses is reduced or the output is turned off.

The resistance of the current sense, which is inserted between 4 and 5, therefore, is

$$R_s = \frac{0.2}{I_m[A]} [\Omega]. \quad (5.83)$$

In addition to operating as a comparator, the over-current amplifier can also operate in the linear mode. Its open-loop gain is about 80 dB. The circuit corresponding to the linear mode (Fig. 5.34) is similar to that of the error amplifier. The impedances in the feedback loop determine the voltage and frequency characteristics.

The over-current amplifier can be used for additional control of the dead time (Fig. 5.34b). The maximum duty cycle is

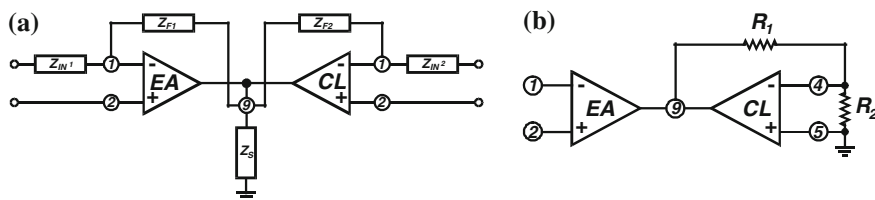


Fig. 5.34 Over-current amplifier circuits corresponding to the linear mode (a) and to the mode of maximum duty cycle limitation (b)

$$D_{\max} [\%] \approx 40 \left[0.2 \left(\frac{R_1}{R_2} + 1 \right) - 1 \right]. \quad (5.84)$$

The resistance R_1 should be higher than 100 k Ω . Then, its influence on the gain of the error amplifier is negligible.

In addition to the PWM comparator, the UC1524A circuit also comprises a PWM latch. The latch has two write inputs (S) and one erase input (R). With each positive pulse at the oscillator output, determining the minimum dead time, the

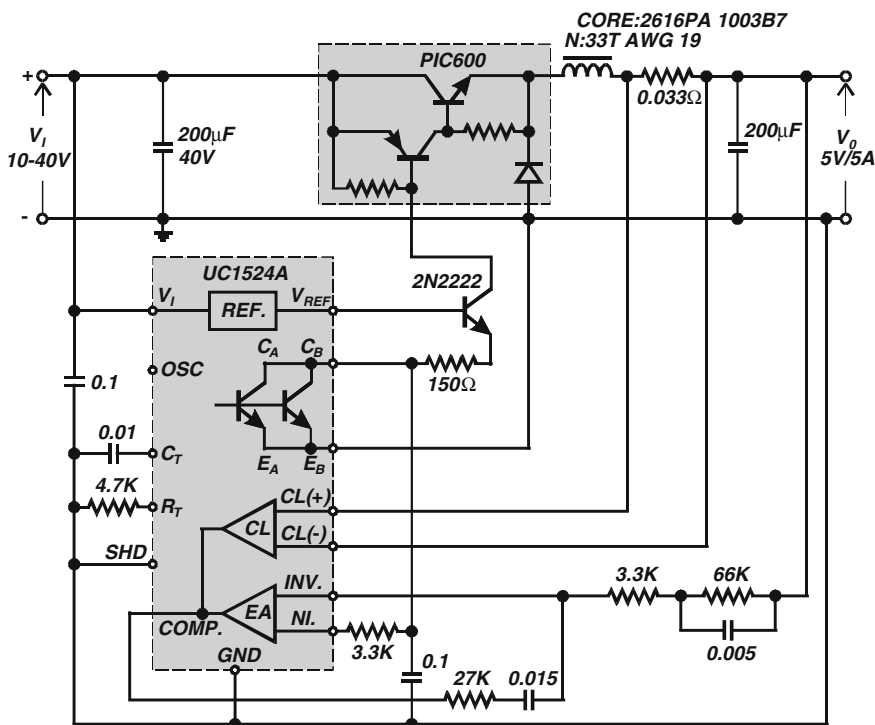


Fig. 5.35 Forward converter (10–40) V/5 V, 5 A based on UC1524A

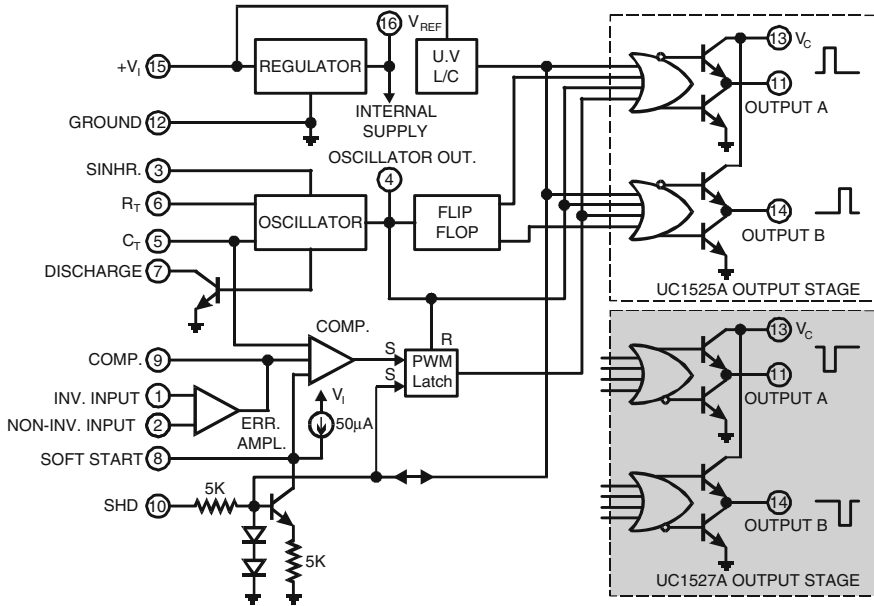


Fig. 5.36 Block diagrams of control modules UC1525A and UC1527A

latch is erased. Each pulse at the PWM comparator output writes the latch. Additional writing is performed via the shutdown input.

As long as this input exists ($V_{SHD} > 2.4\text{ V}$), the latch is written so that the output of the OR circuit is high and the output transistors are off. The latch increases the stability of PWM. It filters out the disturbances that may appear at the output of the PWM comparator as a consequence of the fast disturbances at the outputs of the error and over-current amplifiers. In addition, the latch enables a very fast response to the shutdown.

Figure 5.35 shows a typical example of IC UC1524A application in a forward converter. The function of switching is performed by the hybrid switching circuit PIC 600.

There are several types of control modules which are only improvements of the basic circuit 1524. For instance, the circuit UC1525A (Fig. 5.36) comprises a soft start. The outputs have low impedances and could sink or deliver currents up to 500 mA. The UC1527A circuit is identical to 1525 except for the output stage which is the complement of the 1525 output (Fig. 5.36). Within this set is also UC1526A/2525A/3526A which, additionally, comprises a block for temperature protection.

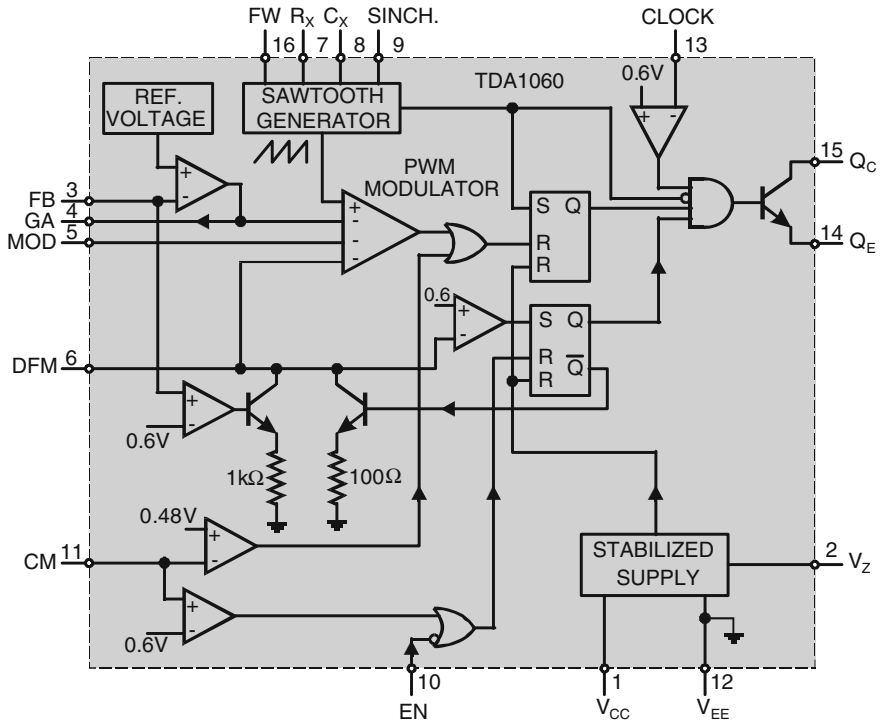


Fig. 5.37 Block diagram of TDA 1060; A; B; T (suffix A is for temperature range 0 up to 70 °C, B is for –55 up to +150 °C, and T for –25 up to +125 °C)

5.4.3 Control Module TDA 1060

The structure of the control module TDA 1060 (Fig. 5.37) is in no way specific. For this reason only the specifications of terminals and functions of individual parameters will be presented here.

In addition to the reference voltage source with the typical value $V_{REF} = 3.72$ V, this circuit contains an internal voltage source $V_Z = 8.4$ V at the pin 2. The frequency of the sawtooth generator is determined by external elements C_x and R_x and can be adjusted within limits 50/100 kHz. Typical values of the timing elements are within limits $5\text{ k}\Omega < R_x < 40\text{ k}\Omega$ and $1\text{ nF} < C_x < 100\text{ nF}$. The frequency dependence on the values of the timing elements $R_x = R_7$ and $C_x = C_8$ is shown in Fig. 5.38a. The input 9 SYN serves for external synchronization of the generator. The frequency of the synchronizing oscillator has to be lower than that of the basic oscillator. If external synchronization is not used, the pin 9 should be connected to the pin 2. The FW input FW (feed-forward) (pin 16) is connected to an external resistive divider connected between the input and the common pin 12. When $V_{16} > V_Z$, the additional control of the duty cycle is accomplished by varying the

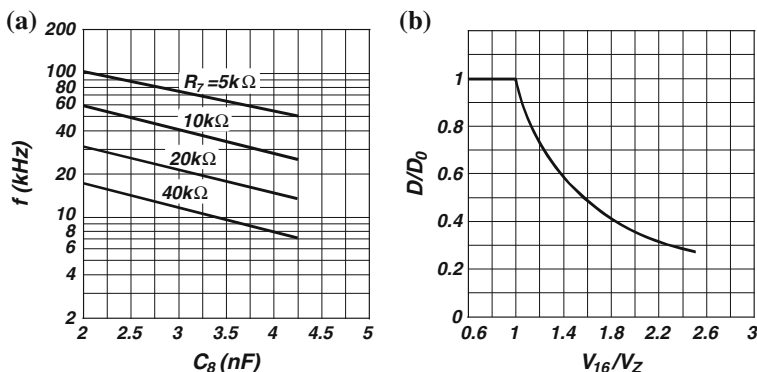


Fig. 5.38 Frequency as function of the timing elements (a) and relative duty cycle as function of ratio V_{16}/V_Z (b)

input voltage. D_0 denotes the duty cycle for $V_{16} \leq V_Z$. If this additional control is not used, the input FW should be connected to the pin 12.

The input DFM (pin 6) serves to program the maximum duty cycle and the realization of the soft start. The minimum dead time, similar to the 1524 circuit, is determined by the duration of the short pulse (discharging time of C) at the oscillator output. Then $t_{DTmin}/T_{osc} \approx 5\%$ (T_{osc} is the oscillator cycle), and the maximum duty cycle is $D_{max} \approx 95\%$. A decrease of the maximum duty cycle is obtained by a decrease of the voltage at the input 6 when $V_6 < 0.6 V_Z$ (Fig. 5.39a). This is accomplished by connecting the input DFM to the resistive divider fed by the output V_Z of the voltage stabilizer.

The time constant of the soft start is determined by the capacitor connected between the pins 6 and 12 and the resistors R_{6-2} and R_{6-12} . Figure 5.39b shows the dependence of the minimum duty cycle of the soft start on the sum of resistances $R_{6-2} + R_{6-12}$ with the maximum duty cycle as a parameter. If the input DFM is not used, it should be connected to V_Z by a resistor of approximately $5 k\Omega$. The operating conditions of the error amplifier are established via the inputs FB (feedback) and GA (gain adjustment), similarly to other control modules.

CM (pin 11) is the current protection input. The peculiarity of this circuit is that it comprises two comparators for over-current protection having thresholds $V_{T1} = 480$ mV and $V_{T2} = 600$ mV. As soon as $V_{11} = V_{T1}$, the upper RS latch is erased and the output is disabled. Then the transistor with 100Ω in the emitter is turned on through $\overline{Q}$. The capacitor C_6 at DFM input is discharged through this transistor. After that, the soft-start procedure is initiated. If the CM input is not used, it should be connected to the pin 12. The over-voltage protection and the output transformer core saturation protection are controlled by the SAT input (pin 13). The core saturation signal obtained during transient processes is generated by a separate winding used as a current sensor. When $V_{SAT} > 600$ mV, the output transistor is off. If the V_{SAT} input is not used, it should be connected to pin 12.

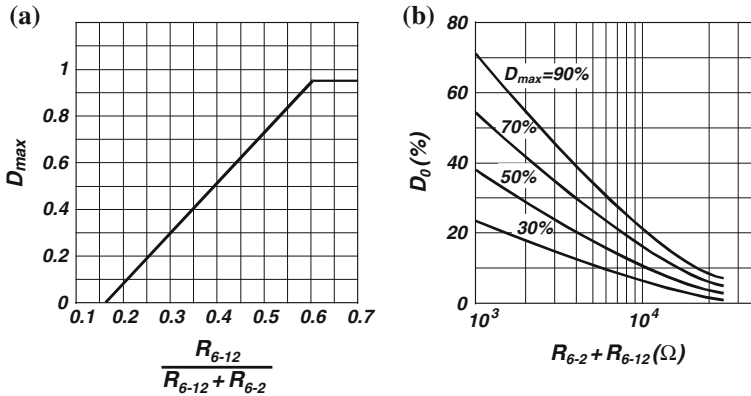


Fig. 5.39 Maximum duty cycle (a) and minimum duty cycle of the soft start (b) as functions of the external resistors between pins 6 and 2 (R_{6-2}) and 6 and 12 (R_{6-12})

EN (Enable)—pin 10 is the enable input, TTL compatible. If $EN = 0$, the output is blocked. Therefore, shutdown is accomplished through EN. When subsequently a high level ($V_{EN} > 2.4$ V) is fed, the converter goes to the soft-start mode. Normally, EN is high. If it is not used, it should be connected to V_Z (pin 2).

The MOD (5) input is used for additional control of the maximum duty cycle or of the voltage gain of the error amplifier. It can also be used in the current control loop, specifically the one with fold back characteristic. If the input MOD is not used, it should be connected to the pin 2.

Figure 5.40 shows the scheme of a DC/DC converter 20–30 V/12 V, 10 A illustrating the connection of IC TDA 1060. The input and output power parts are standard.

The mains converter and stabilizer 220 V/12 V, 10 A based on TDA 1060 (Fig. 5.41) is a forward pulse converter having the input and the output separated. At the maximum output load, the efficiency coefficient is higher than 80 %.

The mains voltage 220 V $\pm$ 10 % is rectified by a bridge rectifier and filtered by a 500 μ F/350 V capacitor. The resistor 100 k Ω , connected in parallel with the capacitor, serves for its discharging after the converter is switched off. At the same time, the mains voltage is fed to the primary winding of the transformer T_4 , which together with the bridge rectifier BY164 and a 680- μ F capacitor ensures the initiation of the operation of the control part of the converter at the switch-on. The capacitor 100 μ F, connected to the pin 6 of IC TDA 1060, is charged through a resistive divider 4.7/10 k Ω . Upon charging of this capacitor, lasting about 0.8 s, the duty cycle changes from 0.1 to 0.5. In this way the so-called “soft start” is provided, i.e., the switching transistor is protected against burn-up during the switch-on process. The driving circuit is made of the transistor BD 230, the transformer T_3 , and the associated elements.

While the transistor BVX 80 is open, the diode BYW 30150, connected in series with the secondary winding of the transformer T_1 , is conducting and energy is

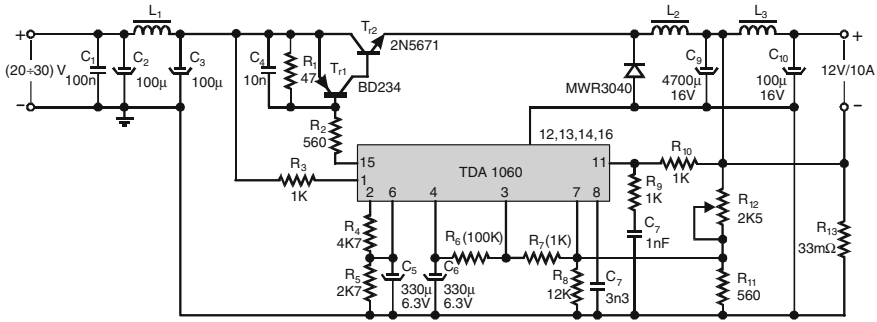


Fig. 5.40 Forward DC/DC converter 20–30 V/12 V, 10 A based on control module TDA 1060

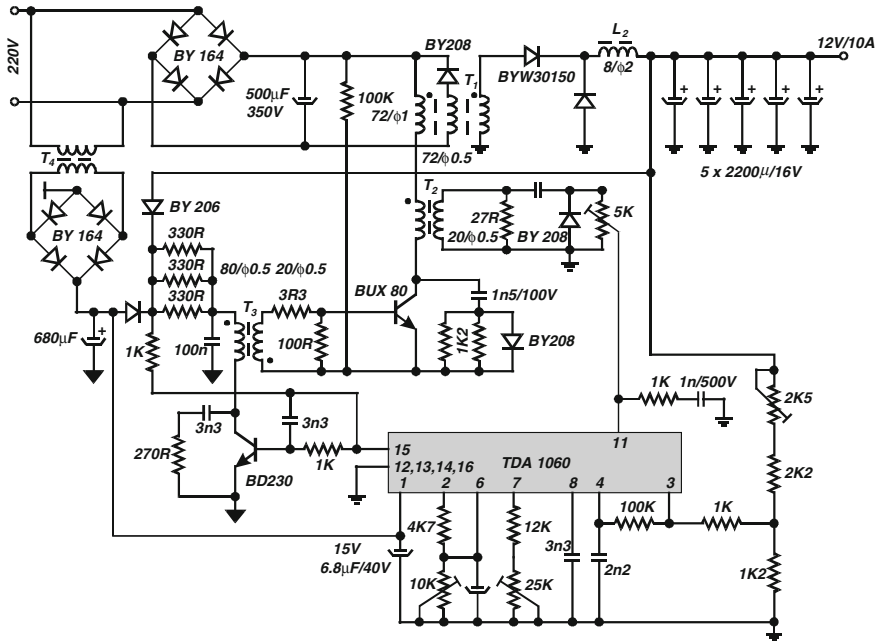


Fig. 5.41 Forward pulse converter 220 V/12 V, 10 A using TDA 1060

accumulated in the choke L_1 . When the transistor is off, this diode stops conducting, and another diode connected to the ground opens enabling the transfer of energy to the load. A part of the DC voltage obtained in this way, via a divider 2.5/2.2/1.2 k Ω , is fed to the DC amplifier in TDA 1060 and from there to the comparator (also within TDA 1060), which at its second input obtains a sawtooth voltage with a constant frequency and amplitude. At the output of this comparator, one obtains a signal whose signal/pause ratio is proportional to the output voltage of the converter.

Upon the switch-on of the converter, the control and driving circuits are supplied by its output, relieving in this way the transformer T_4 . The transformer T_2 , together with the associated elements, serves for current protection of the converter. The threshold of the current protection is adjustable.

The basic technical specifications are as follows: input voltage $220\text{ V} \pm 10\%$, 50 Hz, output voltage 12 V, maximum output current 10 A, operating frequency approximately 20 kHz, output voltage regulation 0.01 V/A, and output ripple approximately 100 mV.

Problems

- 5.1 (a) A PWM controller has a sawtooth pulse oscillator frequency of $f = 20\text{ kHz}$. Determine the RC time constant of the soft-start circuit (Fig. 5.20) if the converter enters the operation mode after a time interval of $t = 10 T = 10/f$ when power supply is switched on. The reference voltage is $V_{\text{REF}} = 10\text{ V}$.
 (b) Draw the waveforms of the voltage on capacitor and the output voltage of the PWM comparator from the moment when power supply is switched on to the moment when the converter enters its operation mode. Sawtooth voltage changes from $V_{\text{TL}} = 2\text{ V}$ to $V_{\text{TH}} = 6\text{ V}$.
- 5.2 Explain the difference between PWM with voltage and with current control
- 5.3 Draw the waveforms of pulse voltage at the output of NOR circuits of the PWM controller (Fig. 5.13a) in the time interval of $5 T_{\text{OSC}}$, where T_{OSC} is the period of sawtooth oscillator voltage. In this interval the error signal increases linearly from 2 to 3.5 V, if the sawtooth oscillator voltage changes from 0 to 4 V. Discuss two cases:
 - (a) $\text{OMC} = 1$ and
 - (b) $\text{OMC} = 0$.

In both cases determine the maximum duty factor if the DC voltage at the input of the dead-time comparator is $V_{\text{DT}} = 0.12\text{ V}$.
- 5.4 Determine the maximum current of forward converters with controller UC1524A (Fig. 5.35) if the current sense monitor $R_S = 0.02\ \Omega$ is connected in series between the inductor and the converter output. Using the circuit from Fig. 5.34 explain how to implement over-current control.
- 5.5 Draw the scheme of the boost rectifier with controller SG1524 (Fig. 5.26a) and calculate the elements of the control circuit if switching frequency is 50 kHz, the maximum transistor current $I_M = 5\text{ A}$, the input voltage $V_I = 12 \pm 10\%$, the output voltage $V_0 = 15\text{ V}$ and the dead time $t_{\text{DT}} = 0.9\ \mu\text{s}$.

- 5.6 Draw the scheme and calculate the elements of the controller UC1527 (Fig. 5.36) in a push–pull converter with the following parameters: $V_I = 12\text{ V} \pm 10\%$, $V_0 = 5\text{ V}$, and $I_{\text{OM}} = 5\text{ A}$. The switching frequency of the power MOS transistor is 60 kHz. Explain the function of each element connected to IC UC1527. Determine the maximum duty factor.
- 5.7 For the control module of the forward converter with UC1524A (Fig. 5.35)
- Determine the maximum converter current I_m
 - Determine the ratio R_1/R_2 (Fig. 5.34b) so that the maximum duty factor is 0.9.
- 5.8 Determine the elements R_X and C_X of the PWM circuit TDA 1060 (Fig. 5.38), so it runs at a frequency of $f = 100\text{ kHz}$. On this basis, determine the minimum dead time and the maximum duty factor of the control signals. Explain how the soft-start circuit is realized.

Reference

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Chapter 6

DC/AC Converters–Inverters

DC/AC converters are used in situations when the primary source is DC (battery, DC motor-generator, solar cells, etc.) and the loads require an AC supply. Since a DC source is inverted to an AC source of energy, DC/AC converters are often called the inverters. This is not quite correct since the inverter is only one, although basic, part of a DC/AC converter (Fig. 6.1). The inverter alone cannot meet the relatively strict technical requirements, such as the accuracy of maintaining the output voltage or current, low harmonic content, high coefficient of efficiency, and small size. For this reason the DC/AC converters consist of the following functional blocks:

- DC current or voltage source,
- control module,
- inverter,
- output filter, and
- current or voltage regulator.

The control module provides driving signals for the switching elements (transistors or thyristors) of the inverter. It consists of an oscillator of monophasic pulses or a generator of multiphase pulses.

In fact, the generator of multiphase pulses is made of logic circuits, which at their outputs give square pulses shifted by a certain phase angle π/n (n is the number of phases of the converter).

The basic function of the converter is to convert a DC voltage to a sequence of square AC pulses. For this reason an output filter is inserted between the load and the inverter with the task of extracting the fundamental harmonic from the sequence of the square pulses so that the voltage across the load would differ as little as possible from the sinusoidal form.

The current and voltage regulator maintains a preassigned value of the AC output voltage and limits the output current to avoid overloading the converter.

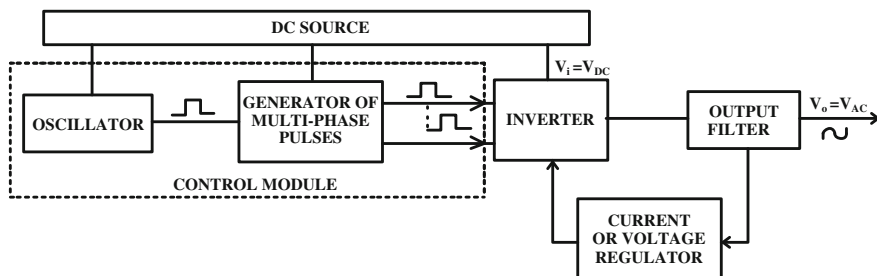


Fig. 6.1 Block diagram of a DC/AC converter

6.1 Single-Phase Voltage Inverters

The bridge voltage inverter (Fig. 6.2a) is the basic circuit of DC/AC converters. The DC power source operates in the voltage generator mode. If the inverter is fed from a rectifier, a sufficiently large capacitor C_g is connected in parallel with its input in order to filter out higher harmonics of the voltage. The voltage inverters create a voltage $+V_{DC}$ across the load (Fig. 6.2b). This is accomplished by the operation of two pairs of switches (S_1, S_2) and (S_3, S_4). While one pair is on, the other is off. Assuming that the switches are ideal, when the first pair (S_1, S_2) is on, the point A is on the $+$, the point B is on the $-$ pole of the power source and $v_0 = V_{AB} = V_{DC}$. In the second half-cycle the pair (S_3, S_4) is on, the point A is on the $(-)$ pole and the point B is on the $(+)$ pole of the power source so that $v_0 = -V_{DC}$.

The switches (S_1, S_4), or (S_3, S_2), must not be on simultaneously because the DC power source would be short circuited.

If the load were resistive, the current i_0 would also have the form of square pulses having amplitudes $+V_{DC}/R_L$ while S_1 and S_2 are on and $-V_{DC}/R_L$ while S_3

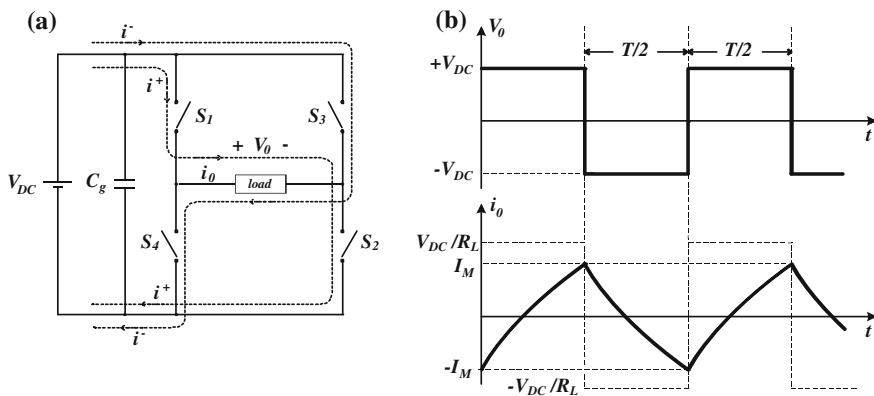
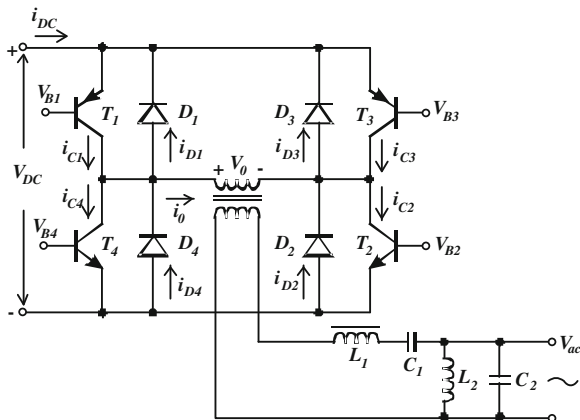


Fig. 6.2 Basic scheme of an inverter (a) and the timing diagram of the voltage and load current (b)

Fig. 6.3 Voltage inverter based on bipolar transistors



and S_4 are on (dashed lines in Fig. 6.2b). In practice, however, the load is usually resistive-inductive or mainly inductive. For this reason Fig. 6.2b shows the form of the current corresponding to an inductive load. In this case, the load current in one half-cycle has both positive and negative values. This means that the switches should be able to conduct in both directions.

For the switches transistors (bipolar or MOS) or thyristors are used. Two-directional conduction of the switches is provided by the anti-parallel connection of a thyristor/transistor and a diode (Fig. 6.3). Figure 6.3 shows an inverter based on bipolar transistors and the output filter for extracting the fundamental harmonic. The transformer T separates galvanically the inverter from the load and output filter. Thus, the equivalent load of the inverter is mainly inductive.

Let the equivalent load of the inverter be a series connection of a resistor R and an inductor L , with the condition $\omega L \gg R$. Then the load current is determined by the differential equation where the saturation voltages V_{CES} of the transistors conducting in saturation are neglected. Then, the next differential equation can be written

$$L \frac{di_0}{dt} + Ri_0 = V_{DC}. \quad (6.1)$$

The initial conditions depend upon the interval of observation. Within the interval $0 \leq t \leq T/2$ the load current increases from its minimum to its maximum value, whereas within the interval $T/2 \leq t \leq T$ the current i_0 decreases from its maximum to its minimum value. Since the pulses are symmetric, the absolute values of the maximum, I_M , and the minimum, I_m , current are equal, i.e. $I_m = -I_M$ so the initial conditions are:

$$i_0(0) = -I_M, \quad i_0(T/2) = I_M. \quad (6.2)$$

After solving Eq. (6.1) and combining the solution with (6.2), it turns out that

$$i_0 = \begin{cases} \frac{V_{DC}}{R} - \left(I_M + \frac{V_{DC}}{R}\right)e^{-t/\tau}, & 0 \leq t \leq T/2, \quad (a) \\ -\frac{V_{DC}}{R} + \left(I_M + \frac{V_{DC}}{R}\right)e^{-(t-T/2)/\tau}, & T/2 \leq t \leq T \quad (b) \end{cases} \quad (6.3)$$

where the time constant is $\tau = L/R$. Therefore, in the interval $0 \leq t \leq T/2$ the load current increases, whereas in the interval $T/2 \leq t \leq T$ it decreases. Since $i_0(T/2) = I_M$, from (6.3) it follows that

$$I_M = \frac{V_{DC}}{R} \frac{1 - e^{-T/(2\tau)}}{1 + e^{-T/(2\tau)}}. \quad (6.4)$$

For instance, if $V_{DC} = 10$ V, $L = 1$ mH, $R = 0.4$ Ω , and $f = 100$ Hz, then from (6.4) $I_M = 19$ mA. If the load were purely resistive $R = 0.4$ Ω , the maximum current would be $I_M = V_{DC}/R = 25$ A.

The current waveforms are shown in Fig. 6.4. Each half-cycle $T/2$ consists of two intervals. For instance, in interval $0 \leq t \leq t_1$ the diodes D_1 and D_2 are conducting, whereas in $t_1 \leq t \leq T/2$ the diodes D_1 and D_2 are off and the transistors T_1 and T_2 are on. From the condition $i_0(t_1) = 0$, and Eq. (6.3) it follows that

$$t_1 = \tau \ln \left(1 + \frac{I_M R}{V_{DC}} \right). \quad (6.5)$$

This time is equal to t_2 , the time when the load current is conducted by D_3 and D_4 .

The thermal losses in the resistor R are determined by I_{rms}^2 , where the root mean square value of the load current is

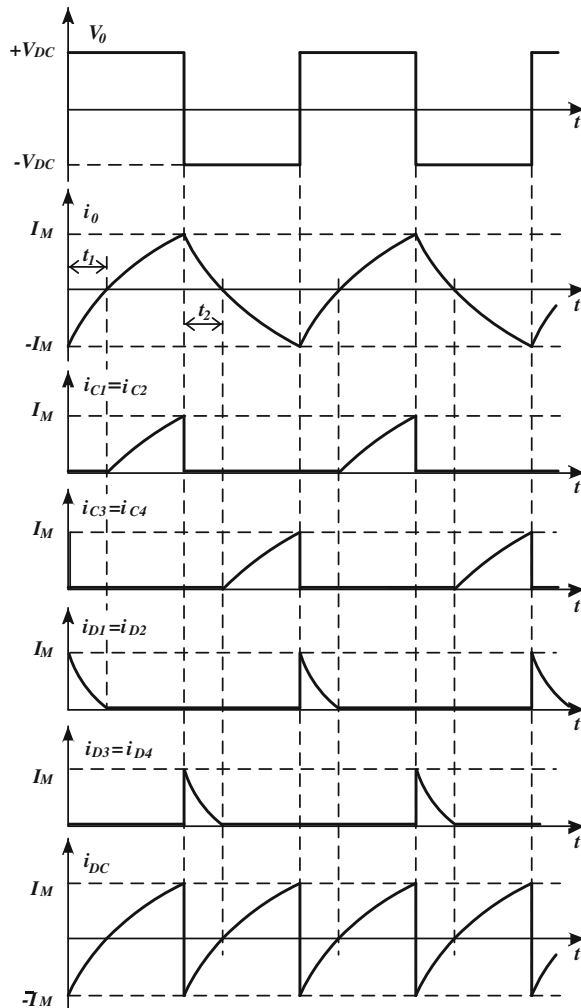
$$I_{rms} = \sqrt{\frac{1}{T} \int_0^T i_o^2(t) dt} = \sqrt{\frac{2}{T} \int_0^{T/2} \left[\frac{V_{DC}}{R} - \left(I_M + \frac{V_{DC}}{R} \right) e^{-t/\tau} \right]^2 dt}. \quad (6.6)$$

The average currents of transistors and diodes are determined by (6.7) and (6.8), respectively

$$I_{Cav} = \frac{1}{T} \int_0^{T/2} i_0(t) dt = \frac{V_{DC}}{R} \left(\frac{T}{2} - t_1 \right) \frac{1}{T} + \left(I_M + \frac{V_{DC}}{R} \right) \frac{\tau}{T} (e^{-(T/2)/\tau} - e^{-t_1/\tau}), \quad (6.7)$$

$$I_{Dav} = \frac{1}{T} \int_0^{t_1} i_0(t) dt = -\frac{V_{DC}}{R} \frac{t_1}{T} + \left(I_M + \frac{V_{DC}}{R} \right) \frac{\tau}{T} (1 - e^{-t_1/\tau}). \quad (6.8)$$

Fig. 6.4 Waveforms of the voltage across the load and currents through: load, transistors, diodes, and power supply



Example 6.1 A single-phase inverter based on thyristors (Fig. 6.5a) has a purely inductive load $L = 1 \text{ mH}$. Draw the timing diagrams and calculate the average values of the currents through the thyristors and the diodes if $V_{DC} = 10 \text{ V}$ and $f = 50 \text{ Hz}$. The thyristors and the diodes can be considered ideal.

When the thyristors Th_1 and Th_2 are on, the voltage across the load is $v_0 = +V_{DC}$, and when Th_3 and Th_4 are on then $v_0 = -V_{DC}$. For this reason the current through the coil will be linear since $L di_0/dt$ is equal either $+V_{DC}$ or $-V_{DC}$. Taking into account the initial conditions it follows that

$$i_0(t) = \begin{cases} -I_M + \frac{V_{DC}}{L}t, & 0 \leq t \leq T/2, \\ I_M - \frac{V_{DC}}{L}t, & T/2 \leq t \leq T. \end{cases}$$

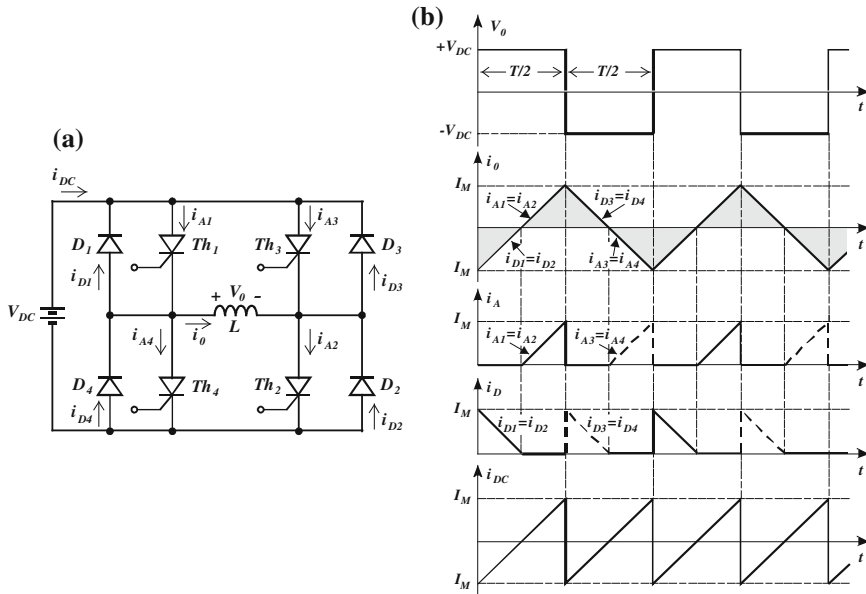


Fig. 6.5 Thyristor single-phase inverter (a) and waveforms of the voltage v_0 and the characteristic currents (b)

The diodes D_1 and D_2 are on within interval $0 < t < T/2$ up to t_1 , or $i_0(t_1) = 0$ wherefrom it follows

$$t_1 = \frac{L I_M}{V_{DC}} = \frac{T}{4}, \text{ since } i_0(T/2) = I_M = \frac{V_{DC}}{4L} T = 25 \text{ A.}$$

Therefore, the diodes and the thyristors are conducting during intervals of $T/4$, thus their average values are equal and amount to

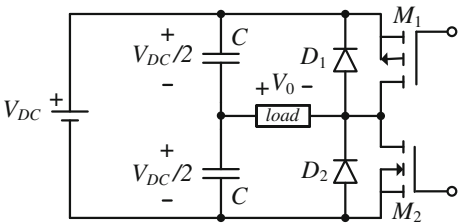
$$I_{Aav} = I_{Dav} = \frac{1}{T} \left(\frac{1}{2} \frac{T}{4} I_M \right) = \frac{I_M}{8} = 3.125 \text{ A.}$$

The waveforms of the voltage v_0 and of the characteristic currents are shown in Fig. 6.5.

So far only bridge inverters have been considered. The half-bridge inverters (Fig. 6.6) which are also in use consist of two switches and two capacitors.

The capacitors have the same capacitance and each one takes one half of the DC voltage ($V_{DC}/2$). The transistors are alternatively on and off. Since the voltages across the capacitors are always $V_{DC}/2$, the voltage across the load is either $+V_{DC}$ or $-V_{DC}$.

Fig. 6.6 Half-bridge inverter

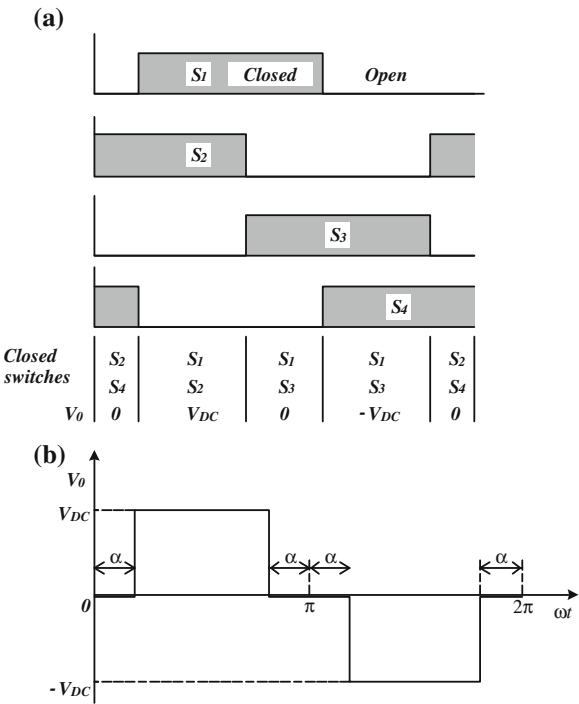


6.1.1 Pulse-Controlled Output Voltage

The control pulses should be phase-shifted so that the switches give zero voltage across the load at the start and at the end of each half-cycle (Fig. 6.7). Thus, one obtains

$$v_0(t) = \begin{cases} +V_{DC}, & \alpha \leq \omega\tau \leq \pi - \alpha, \\ -V_{DC}, & \pi + \alpha \leq \omega\tau \leq 2\pi - \alpha, \\ 0, & 0 \leq \omega\tau \leq \alpha, \pi - \alpha \leq \omega\tau \leq \pi + \alpha, 2\pi - \alpha \leq \omega\tau \leq 2\pi. \end{cases} \quad (6.9)$$

Fig. 6.7 Real states of switches (a) and the corresponding waveform of the output voltage of the inverter from Fig. 6.2a (b)



This is necessary for two reasons. In this way the simultaneous conduction of S_1 and S_4 or of S_2 and S_3 is avoided. Practically, this would be possible during transition if for example S_1 were turning on, S_4 were turning off, and vice versa. During that time the DC power source would be short-circuited. In order to avoid that, the control pulses have to be phase-shifted at least for the maximum duration of the transition process. The sequence of turning on the switches should prevent the formation of a low Ohmic loop in parallel with the DC power source. This is related to the problem of non-overlapping (overlapping) which will be considered in more detail in the chapter dealing with real driving.

In this chapter the phase-shifted control pulses are of interest from another point of view. Namely, it is possible to control the voltage of the fundamental harmonic through the angle of the phase-shift. The mean square value of the voltage in Fig. 6.7 is determined by

$$V_{\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\pi-\alpha} V_{\text{DC}}^2 d(\omega t)} = V_{\text{DC}} \sqrt{1 - \frac{2\alpha}{\pi}}. \quad (6.10)$$

The Fourier series of this signal is

$$v_o(t) = \sum_{k=1}^{\infty} V_n \sin[(2k-1)\omega t] \quad (6.11)$$

and it contains odd harmonics. If the odd harmonics are denoted by $n = 2k - 1$, taking into account the symmetry of the square pulses the amplitudes are

$$V_n = \frac{2}{\pi} \int_{\alpha}^{\pi-\alpha} V_{\text{DC}} \sin(n\omega t) d(\omega t) = \frac{4V_{\text{DC}}}{n\pi} \cos(n\alpha). \quad (6.12)$$

Therefore, the amplitude of each harmonic is a function of the angle α which corresponds to the zero voltage across the load. It is important to emphasize that by an adequate choice of α individual harmonics can be eliminated. Namely, if

$$\alpha = 90^\circ / n, \quad (6.13)$$

the n -th harmonic will be eliminated. If $\alpha = 30^\circ$, then $V_3 = 0$, meaning that the third harmonic is eliminated. Then the amplitude of the fundamental harmonic is $V_1 = (4V_{\text{DC}}/\pi)\cos(30^\circ) = 1.1V_{\text{DC}}$. The fifth harmonic is eliminated if $\alpha = 90^\circ/5 = 18^\circ$, and the amplitude of the first harmonic will be $V_1 = 1.2V_{\text{DC}}$.

Total harmonic distortion can be reduced by reducing individual harmonics (see Example 6.2).

Example 6.2 The load of the inverter from Fig. 6.2 is inductive-resistive with $L = 25$ mH and $R = 10 \Omega$. If $V_{DC} = 100$ V and $f = 50$ Hz determine the total harmonic distortions of the voltage and current at

(a) $\alpha = 0$ and (b) $\alpha = 30^\circ$.

The amplitudes of the harmonics in the Fourier series of the load current are determined by

$$I_n = \frac{V_n}{Z_n} = \frac{V_n}{\sqrt{R^2 + (n\omega L)^2}} = \frac{4 \times 100 / (n\pi) \times \cos(n\alpha)}{\sqrt{10^2 + [n(2\pi \times 50) \times 0.025]^2}},$$

and the amplitudes of the voltage harmonics across the load are given by (6.12). The individual values of V_n and I_n are given in Table 6.1.

Table 6.1 The individual values of V_n and I_n

n	f_n (Hz)	Z_n (Ω)	V_n (V)		I_n (A)	
			$\alpha = 0$	$\alpha = 30^\circ$		
1	50	12.71	127.3	110.2	1	50
3	150	25.59	42.4	0	3	150
5	250	40.52	25.5	22.1	5	250
7	350	55.88	18.2	15.7	7	350
9	450	71.39	14.1	0	9	450

The total harmonic voltage distortion is determined by

$$\text{THD}_v = \frac{\sqrt{V_{\text{rms}}^2 - V_{1,\text{rms}}^2}}{V_{1,\text{rms}}}.$$

(a) $V_{\text{rms}} = V_{DC}$, $V_{1,\text{rms}} = \frac{V_1}{\sqrt{2}} = \frac{4V_{DC}}{\sqrt{2}\pi} = 90.07$ V,

$$\text{THD}_v = \frac{\sqrt{100^2 - 90.07^2}}{90.07} = \frac{43.43}{90.07} = 0.482 = 48.2 \%.$$

(b) On the basis of (6.10), the rms value of the voltage across the load for $\alpha = 30^\circ$ is

$$\begin{aligned} V_{\text{rms}} &= 100 \sqrt{1 - \frac{2 \times 30}{180}} = 81.6 \text{ V}, \\ V_{1,\text{rms}} &= \left(\frac{4V_{DC}}{\pi} \cos \alpha \right) / \sqrt{2} = 110 / \sqrt{2} = 77.92 \text{ V}, \\ \text{THD}_v &= \frac{\sqrt{81.6^2 - 77.92^2}}{77.92} = \frac{24.23}{77.92} = 0.311 = 31.1 \%. \end{aligned}$$

The total harmonic distortion of load current is determined by (1.26), so according to the values given in the Table 6.1 one has

$$\text{THD}_I = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n\text{rms}}^2}}{I_{1\text{rms}}} = \frac{\sqrt{\left(\frac{1.65}{\sqrt{2}}\right)^2 + \left(\frac{0.63}{\sqrt{2}}\right)^2 + \left(\frac{0.32}{\sqrt{2}}\right)^2 + \left(\frac{0.2}{\sqrt{2}}\right)^2}}{10.01/\sqrt{2}} = 0.18 = 18\%,$$

$$\text{(b) THD}_I = \frac{\sqrt{\left(\frac{0.54}{\sqrt{2}}\right)^2 + \left(\frac{0.28}{\sqrt{2}}\right)^2}}{8.67/\sqrt{2}} = 0.07 = 7\%.$$

6.2 Pulse-Width Modulated Inverters

It has been shown in Chap. 4 that the ratio of the output and the input voltage of DC/DC converters is directly proportional to the duty cycle of the control pulses with a constant frequency and a variable duration. Pulse-width modulation is used in inverters for the purpose of regulating the amplitude and the frequency of the output voltage. In the inverter circuits it is even more complex because it is required that one obtains approximately sinusoidal (quasi-sinusoidal) voltage of a preassigned frequency (usually 50 or 60 Hz) at its output.

The pulse-width-modulated (PWM) inverters use a harmonic control (modulating) signal, whereas the carrier signal is triangular, as in DC/DC converters. A PWM module consists of:

- a sinusoidal oscillator with a frequency f_1 (normally 50 or 60 Hz) which generates the control signal,
- a generator of triangular voltage (carrier signal) whose frequency f_s is several times higher than f_1 ,
- a comparator with complementary outputs (Fig. 6.8).

The pulse frequency at the comparator output is equal to the frequency of the carrier signal f_s , and the duration of the pulses depends on the ratio of the instantaneous values of the voltages of the control and carrier signals. Since these pulses control the states of the inverter switches, the switches will also operate at the frequency f_s modulated by the ratio of the turn-on and the turn-off time. Consequently, it follows that

$$v_o = \begin{cases} +V_{\text{DC}}, & V_c > V_{\text{TM}} (S_1 \text{ and } S_2 \text{ are turned on}) \\ -V_{\text{DC}}, & V_c < V_{\text{TM}} (S_3 \text{ and } S_4 \text{ are turned on}) \end{cases} \quad (6.14)$$

which is illustrated in Fig. 6.9. Since the output voltage varies between $+V_{\text{DC}}$ and $-V_{\text{DC}}$, these PWM are bipolar modulators. Because the frequency of the carrier signal is much higher than the frequency of the sinusoidal control signal, i.e., $f_s \gg f_1$,

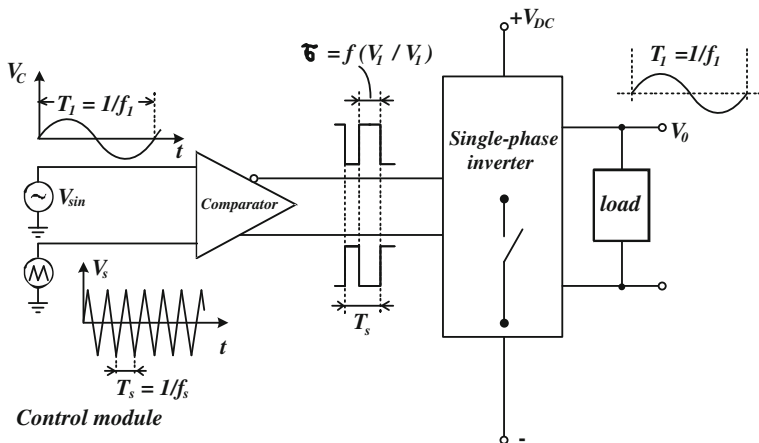
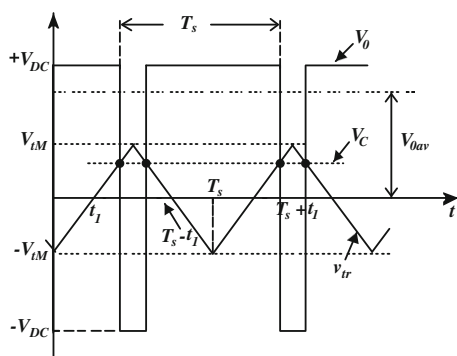


Fig. 6.8 Block diagram of a single-phase PWM inverter

Fig. 6.9 Waveforms of characteristic voltages in one period of the carrier signal



it may be assumed that the control voltage V_c during the cycle T_s is approximately constant (Fig. 6.9). Then, based on Fig. 6.9, the average value of the output voltage is

$$V_{0av} = \frac{1}{T_s} \left[\int_{t_1}^{T_s - t_1} -V_{DC} dt + \int_{T_s - t_1}^{T_s + t_1} V_{DC} dt \right]. \quad (6.15)$$

Because in the interval $0 \leq t \leq T_s$: $V_{tr} = -V_{im} + (4V_{im}/T_s)t$, from the condition $V_{tr}(t_1) = V_c$ it follows that

$$t_1 = \frac{T_s}{4} \left(1 + \frac{V_c}{V_{im}} \right). \quad (6.16)$$

From (6.15) and (6.16) it follows that

$$V_{0av} = \frac{V_c}{V_{tM}} V_{DC}. \quad (6.17)$$

If

$$V_c = V_{cM} \sin(\omega t), \quad (6.18)$$

then

$$V_{0av} = \frac{V_{cM}}{V_{tM}} V_{DC} \sin(\omega t) = m_a V_{DC} \sin(\omega t), \quad (6.19)$$

where

$$m_a = \frac{V_{cM}}{V_{tM}} \quad (6.20)$$

is the factor of amplitude modulation, equal to the ratio of the sinusoidal control signal and the triangular carrier signal. On the basis of (6.19) one can draw a very important conclusion that the average value of the output voltage is a sinusoidal function having the frequency of the control signals f_1 (dashed line in Fig. 6.10b) and the amplitude

$$V_{0M} = m_a V_{DC} \leq V_{DC}, \quad (6.21)$$

because the amplitude modulation factor $m_a \leq 1$.

In addition to the factor of amplitude modulation a definition is also made of the factor of frequency modulation as the ratio of the frequencies of the carrier and the control signals, i.e.,

$$m_f = \frac{f_s}{f_1}. \quad (6.22)$$

Even though $m_f \gg 1$, the control signal is not constant within one cycle T_s . For this reason the output voltage will contain higher harmonics, whereas (6.19) gives its fundamental harmonic. The higher harmonics appear around the carrier frequency (Fig. 6.10c) and its integer multiples, more precisely around the harmonics $m_f, 2m_f, 3m_f, \dots$. For instance, if $m_f = 15$, harmonics 15, 17, 13, ..., 31, 33, 29, etc. will exist.

Table 6.2 presents the normalized Fourier coefficients for individual harmonics versus the factor of amplitude modulation. It should be noted that the coefficients in Table 6.1 are almost independent of m_f if $m_f \geq 9$.

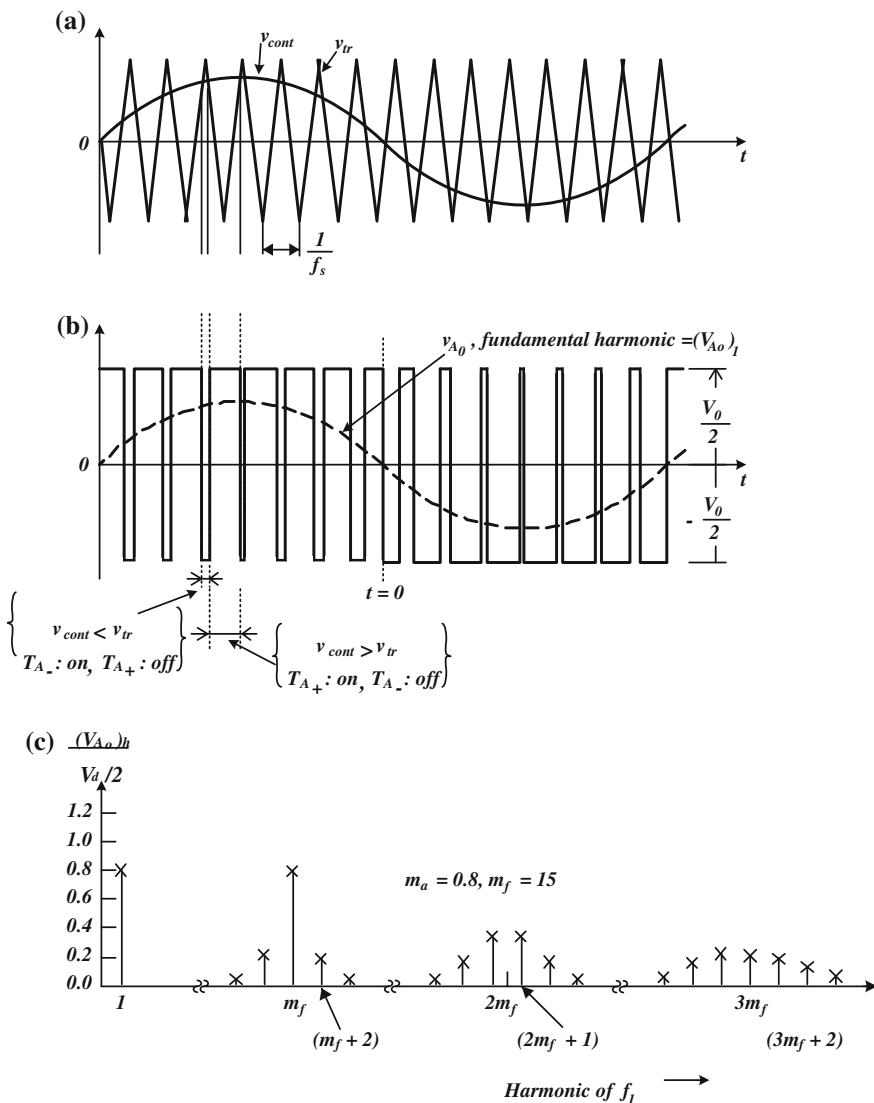


Fig. 6.10 Voltage waveforms (a and b) and frequency spectrum of the inverter based on bipolar PWM (c)

From Table 6.2 it can be noted that the amplitudes of some harmonics may be higher than the amplitude of the fundamental harmonic. A favorable circumstance is that the higher harmonics are at considerably higher frequencies and can readily be filtered out. This is a significant advantage of the inverters based on PWM. The higher the carrier frequency is, the less difficult the problem of filtering will be. The maximum frequency f_s is limited by dynamic losses in semiconductor switches.

Table 6.2 Normalized harmonics of bipolar PWM [1]

Harmonic	0.2	0.4	0.6	0.8	1.0
1 (fundamental)	0.2	0.4	0.6	0.8	1.0
m_f	1.242	1.15	1.006	0.818	0.601
$m_f \pm 2$	0.016	0.061	0.131	0.220	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.190	0.326	0.370	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.113
$3m_f \pm 2$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 4$		0.012	0.047	0.104	0.157
$3m_f \pm 6$				0.016	0.044

Thus, f_{smax} of the inverters based on bipolar transistors is from ten to several tens kHz, whereas for MOS transistors it is about a 100 kHz.

Example 6.3 A bridge PWM inverter should provide alternating voltage at a frequency $f = 50$ Hz across an R-L load ($R = 10 \Omega$, $L = 20$ mH). The amplitude modulation factor is $m_a = 0.8$ and the frequency modulation factor is $m_f = 21$. The input DC voltage is $V_{\text{DC}} = 100$ V. It is required to determine:

- the amplitudes of the fundamental harmonics of the output voltage and load current,
 - THD of the load current, and
 - power dissipation in the resistive component of the load.
- (a) According to (6.19) the amplitude of the fundamental harmonic is

$$V_{01} = m_a V_{\text{DC}} = 0.8 \times 100 = 80 \text{ V}.$$

The amplitudes of the harmonics of the load current are

$$I = \frac{V_{0h}}{Z_h} = \frac{V_{0h}}{\sqrt{R^2 + (h\omega L)^2}}, \quad (6.23)$$

and the amplitude of the fundamental harmonic of the load current is

$$I_{01} = \frac{80 \text{ V}}{\sqrt{10^2 + (1 \times 2 \times \pi \times 50 \times 0.02)^2}} = 6.39 \text{ A}.$$

Table 6.3 The calculated values of harmonics for the voltage, load current and absorbed power

h	$f_h(\text{Hz})$	$V_{0h}(\text{V})$	$Z_{0h}(\Omega)$	$I_{0h}(\text{A})$	$I_{0\text{hrms}}(\text{A})$	$P_h(\text{W})$
1	50	80.0	11.81	6.78	4.79	229.4
19	950	22.0	119.8	0.18	0.13	0.2
21	1,050	81.8	132.3	0.62	0.44	1.9
23	1,150	22.0	144.8	0.15	0.11	0.1

- (b) Since $m_f = 21$, the first higher harmonics are $h = 19$, $h = 21$, and $h = 23$. On the basis of Table 6.1 it follows that

$$V_{021} = 0.818 \times 100 = 81.8 \text{ V},$$

$$V_{19} = V_{023} = 0.22 \times 100 = 22 \text{ V}.$$

The currents of these harmonics are determined by (6.24). The power dissipated by individual harmonics on the resistive component of the load is determined by

$$P_h = I_{0h,\text{rms}}^2 R = \left(\frac{I_{0h}}{\sqrt{2}} \right)^2 R.$$

The calculated values of harmonics for the voltage, load current, and absorbed power are presented in Table 6.3.

THD of the load current is determined by (1.26) and

$$\text{THD}_I = \frac{\sqrt{(0.13)^2 + (0.44)^2 + (0.11)^2}}{4.79} = 0.098 = 9.8 \text{ \%}.$$

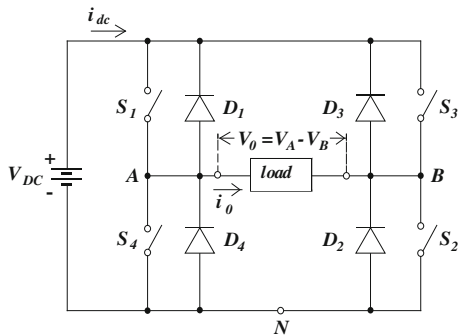
- (c) The dissipation on the resistor R is

$$P = \sum P_h = 229.4 + 0.2 + 1.9 + 0.1 = 231.6 \text{ W}.$$

6.2.1 Unipolar PWM

The output voltage of the inverters based on PWM, described in the preceding sections, varies between $+V_{\text{DC}}$ and $-V_{\text{DC}}$. For this reason these inverters are called the bipolar PWM inverters, or the inverters based on bipolar PWM. Compared to them, the output voltage of the unipolar PWM inverters varies between 0 and $+V_{\text{DC}}$ or between 0 and $-V_{\text{DC}}$. Here, the switches in the branches A and B (Fig. 6.11) do not change the states simultaneously like they do in the inverters based on bipolar PWM. The arms A and B of the bridge are separately controlled by comparing in

Fig. 6.11 Principally scheme of single-phase voltage inverter for which unipolar PWM is applied



turns the triangular voltage of the carrier with the positive (V_c) and negative ($-V_c$) control voltages. For a positive control voltage it follows

$$\begin{aligned} V_c > V_{tr} : S_1 \text{ on, } S_4 \text{ off, } V_{AN} &= +V_{DC}, \\ V_c < V_{tr} : S_4 \text{ on, } S_1 \text{ off, } V_{AN} &= 0. \end{aligned} \quad (6.24)$$

From the comparison of $-V_c$ and the triangular signal (Fig. 6.12) it follows:

$$\begin{aligned} -V_c > V_{tr} : S_3 \text{ on, } S_2 \text{ off, } V_{BN} &= +V_{DC} \\ -V_c < V_{tr} : S_2 \text{ on, } S_3 \text{ off, } V_{BN} &= 0. \end{aligned} \quad (6.25)$$

The voltage levels from Eqs. (6.24) and (6.25) are represented in Fig. 6.12b, c. The output voltage (Fig. 6.12d) is the voltage difference between the points A and B, i.e.,

$$V_o = V_{AN} - V_{BN}. \quad (6.26)$$

In accordance with the previous equations Table 6.4 shows the states of the switches and the levels of characteristic voltages. When both switches in the upper or lower half of the bridge are on, the output voltage is zero. The load current flows in the loop S_1 – D_3 or S_3 – D_1 or S_4 – D_2 or S_2 – D_4 , depending upon the direction of i_o . Within these intervals the current i_{dc} of the primary source is zero.

The output voltage (Fig. 6.12d) consists of the bipolar package of the pulse-width modulated square pulses. Within one cycle of the control voltage these pulses vary between 0 and $+V_{DC}$, whereas in the next cycle they vary between 0 and $-V_{DC}$. Owing to this the first harmonics appear around the frequency $2m_f f_1$, and the second around $4m_f f_1$ (Fig. 6.12e). Therefore, compared to a bipolar PWM, the frequencies of harmonics have doubled, which is a significant advantage of the unipolar PWM. The parameters of the fundamental harmonic are the same as for the bipolar PWM. The amplitude is $V_{0M1} = m_a V_{DC}$ and the frequency is equal to the control signal frequency f_1 .

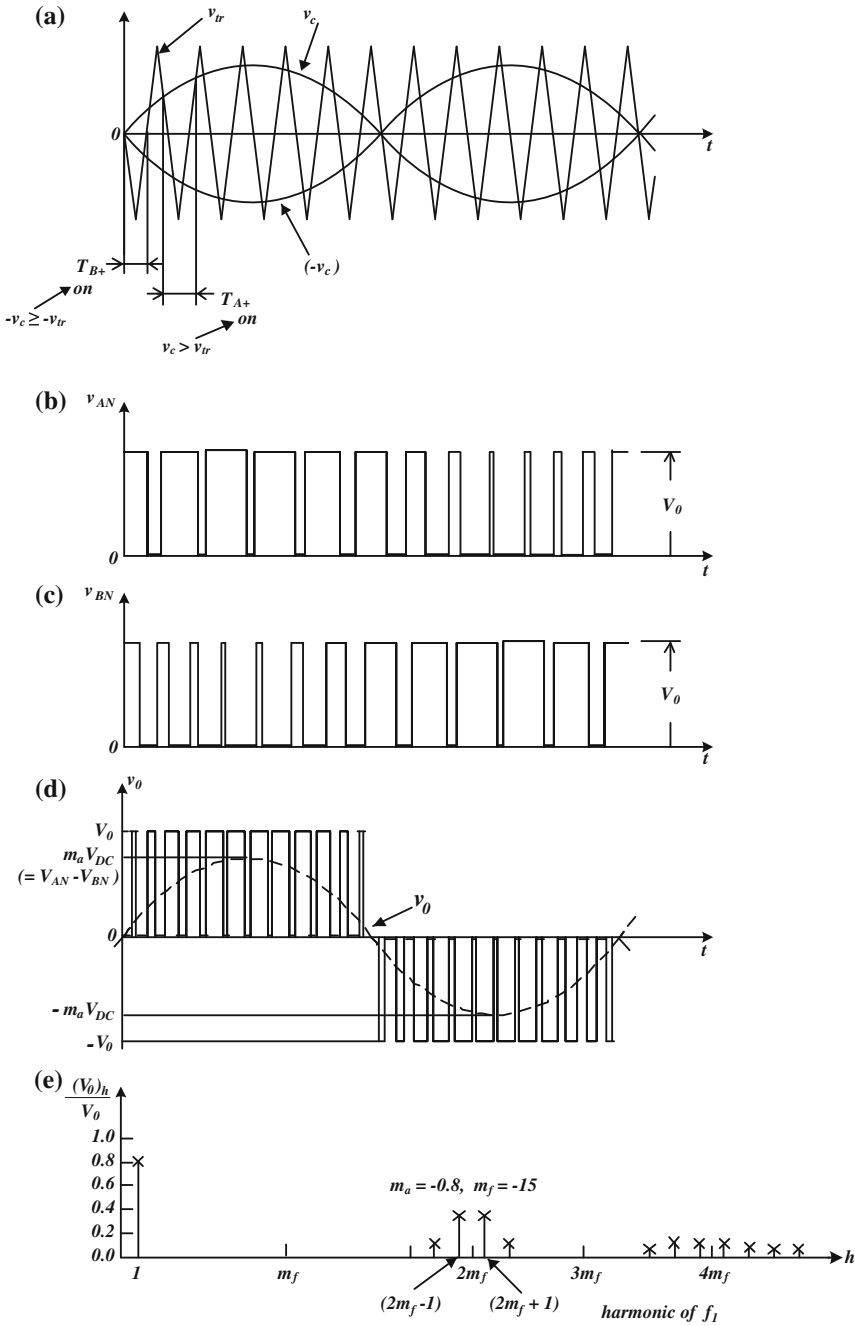


Fig. 6.12 Waveforms (a, b, c, and d) and frequency spectrum of a single-phase inverter based on unipolar PWM

Table 6.4 The states of the switches and voltage levels of a single-phase inverter based on unipolar PWM

Closed switches	V_{AN}	V_{BN}	$V_0 = V_{AN} - V_{BN}$
S_1, S_2	V_{DC}	0	V_{DC}
S_4, S_3	0	V_{DC}	$-V_{DC}$
S_1, S_3	V_{DC}	V_{DC}	0
S_2, S_4	0	0	0

Table 6.5 Normalized Fourier coefficients V_h/V_{DC} of an inverter based on unipolar PWM as functions of the amplitude modulation factor m_a [2]

hm_a harmonic	1	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
$h = 1$	1.00	0.90	0.80	0.70	0.60	0.50	0.40	0.30	0.20	0.10
$h = 2m_f \pm 1$	0.18	0.25	0.31	0.35	0.37	0.36	0.33	0.27	0.19	0.10
$h = 2m_f \pm 3$	0.21	0.18	0.14	0.10	0.07	0.04	0.02	0.01	0.00	0.00

Table 6.6 Turn-on conditions of switches

Closed switch	Condition
S_1	$V_c > V_{tr}$
S_2	$V_c > 0$
S_3	$V_c < 0$
S_4	$V_c < V_{tr}$

In addition to twice higher harmonics, the voltage variation across the load of the unipolar PWM is one half of that of a bipolar PWM, which reduces stress imposed on components during transients.

Table 6.5 shows the normalized Fourier coefficients V_h/V_{DC} of the unipolar PWM.

All switches for the described procedure of unipolar PWM operate at the frequency of the carrier signal, and thus have to be high-frequency switches. Another type of unipolar PWM uses two low-frequency switches (operating at the control frequency) and two high-frequency switches. The state of the switches S_1 and S_4 (the left-hand side of the bridge) depend on the ratio of V_c and V_{tr} , whereas the states of the switches S_2 and S_3 (the right-hand side of the bridge) depend on whether the control signal is positive or negative (Table 6.6).

The characteristic voltage waveforms are shown in Fig. 6.13. These inverters possess lower dynamic losses caused by the transient processes in the semiconductor switches.

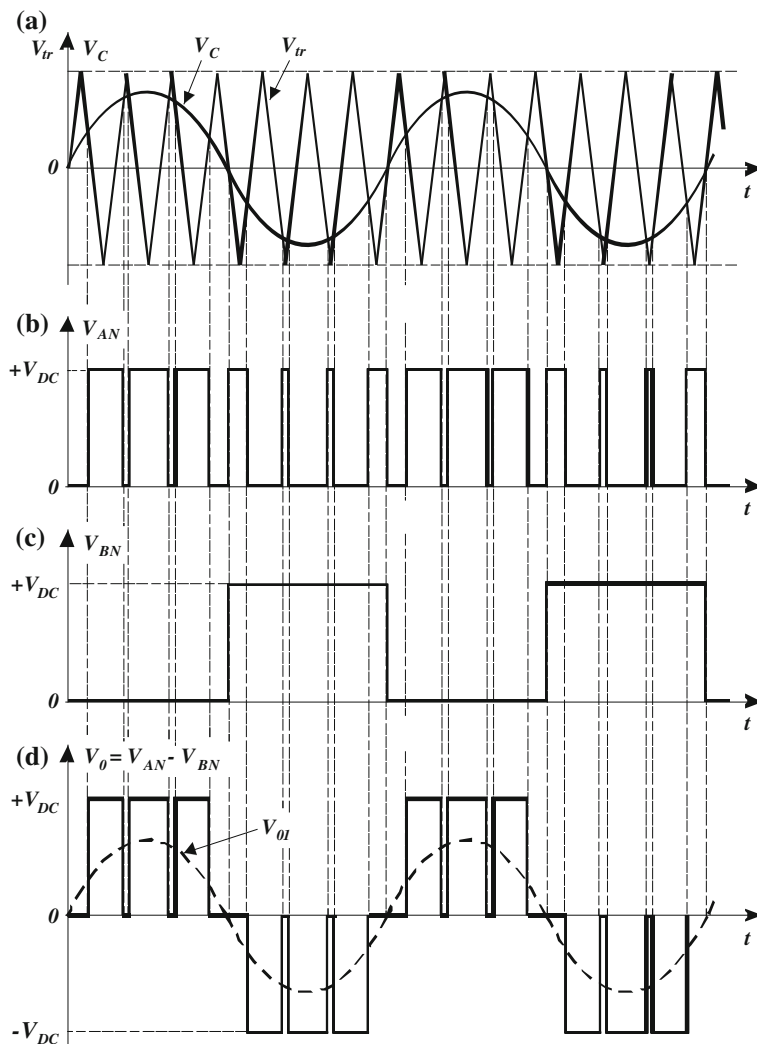
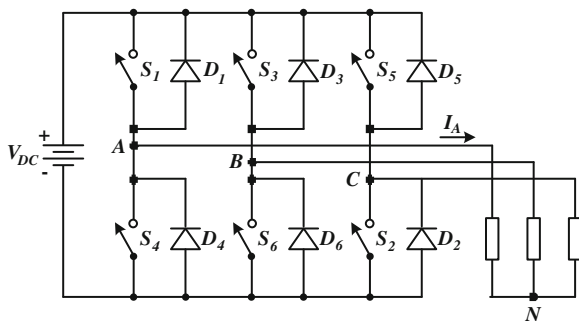


Fig. 6.13 Waveforms of a PWM inverter (a, b, c and d) having two high-frequency and two low-frequency switches

6.3 Three-Phase Inverters

Sometimes it is required to convert a DC voltage to a three-phase AC voltage. The supply and control of induction motors are typical examples. The basic circuit diagram of the three-phase inverter (Fig. 6.14) consists of three pairs of bilateral switches (switch S_i diode D_i) and the phase loads in this case in the star connection. The pairs of switches in each arm (S_1, S_4), (S_3, S_6), and (S_2, S_5) are complementary, i.e., when one is closed, the other is open.

Fig. 6.14 Basic circuit diagram of a three-phase voltage inverter



The state of the switches changes in $T/6 = 60^\circ$ phase steps (Fig. 6.15a), which provides the line and phase voltages as shown in Fig. 6.15b, c. Since within one cycle all six switches close and open once, these inverters are called the six-step inverters.

The frequency of the fundamental harmonic of the output voltage is that of the switches. The third harmonic and its integer multipliers as well as all even harmonics are suppressed. This means that the present harmonics are

$$n = 6k \pm 1, \quad k = 1, 2, \dots \quad (6.27)$$

If the load is an ungrounded star, the Fourier coefficients of the line and phase voltages are:

$$V_{h,L-L} = \left| \frac{4V_{DC}}{n\pi} \cos\left(\frac{n\pi}{6}\right) \right|, \quad (6.28)$$

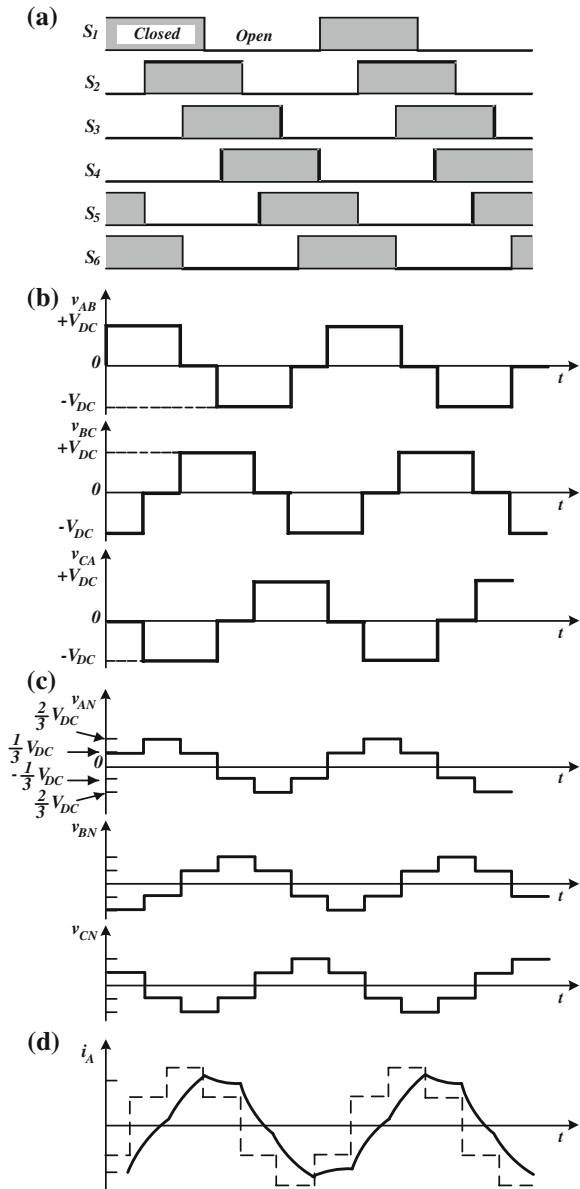
$$V_{h,L-N} = \left| \frac{2V_{DC}}{3n\pi} \left[2 + \cos\left(\frac{n\pi}{3}\right) - \cos\left(n\frac{2\pi}{3}\right) \right] \right|. \quad (6.29)$$

PWM is also applicable to three-phase inverters.

The advantages are the same as for the single-phase inverters. Thus, the frequency of the fundamental harmonic of each phase is equal to the frequency of the sinusoidal control voltage. The amplitude of this harmonic can be controlled by the ratio of the control and the carrier signal. Higher harmonics appear at the carrier signal frequency and the integer multipliers of this frequency, which facilitates filtering of the output voltage. Each pair of the switches (S_1, S_4), (S_3, S_6), and (S_2, S_5) requires one control (reference) signal. These three control voltages are phase shifted by 120° (Fig. 6.16). The conditions when the switches are closed are given in Table 6.7.

Higher harmonics will be reduced if the modulation factor is an odd multiple of 3, i.e., if the frequency of the carrier signal is 3, 9, 15, 21, 27, ... times higher than the control signal frequency.

Fig. 6.15 Cycle of changes of the states of switches (a), line voltages (b), phase voltages for a load connected as ungrounded star (c), and the current of phase A for an R-L load (d)



The Fourier coefficients of the line voltages are

$$V_{h3} = \sqrt{A_{h3}^2 + B_{h3}^2}, \quad (6.30)$$

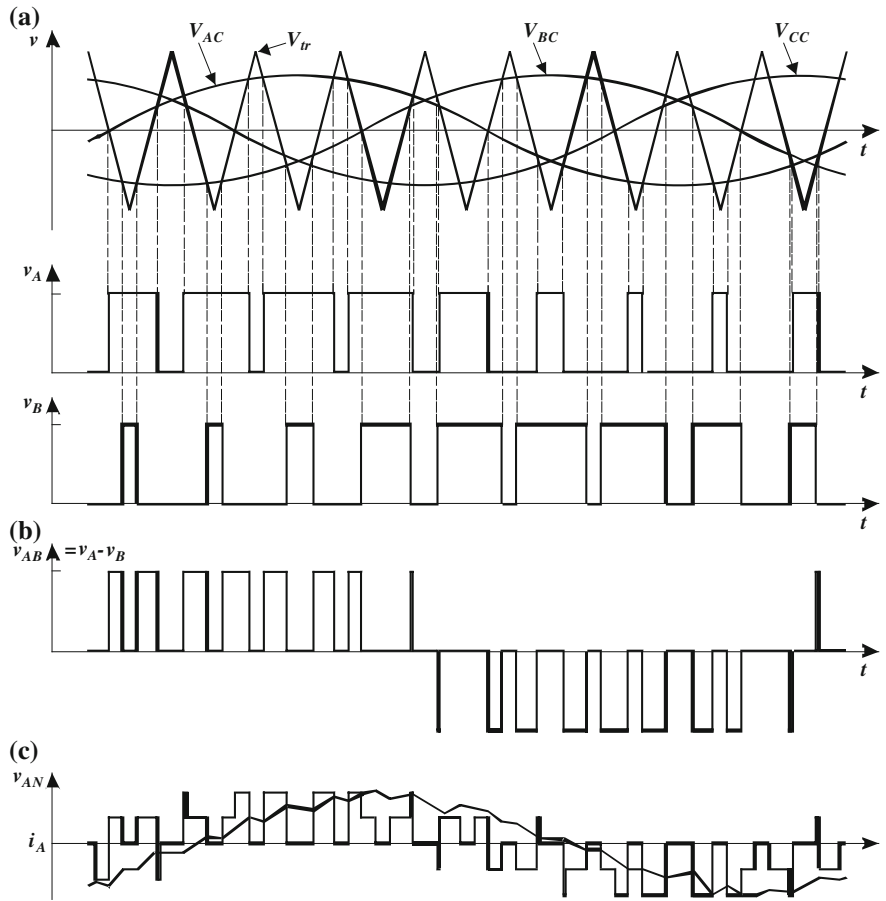


Fig. 6.16 Triangular carrier and sinusoidal control signals of a three-phase PWM inverter at $m_a=0.7$ and $m_f=0.9$ (a), the characteristic voltages (b), and the current in phase A for an R - L load (c)

Table 6.7 Conditions for the closed switches

Closed switch	Condition
S_1	$V_{AC} > V_{tr}$
S_2	$V_{CC} > V_{tr}$
S_3	$V_{BC} > V_{tr}$
S_4	$V_{AC} < V_{tr}$
S_5	$V_{CC} < V_{tr}$
S_6	$V_{BC} < V_{tr}$

where

$$A_{h3} = V_h \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right), \quad (6.31)$$

$$B_{h3} = V_h \sin\left(\frac{n\pi}{2}\right) \cos\left(\frac{n\pi}{3}\right). \quad (6.32)$$

The normalized values of these coefficients are shown in Table 6.8.

Example 6.4 Determine the total harmonic distortion of the load current for the six-step inverter shown in Fig. 6.13. The resistive-inductive load, $R = 10 \, \Omega$ and $L = 20 \, \text{mH}$, is in the star connection. The DC input voltage is $V_{\text{DC}} = 100 \, \text{V}$ and the fundamental frequency of the output voltage should be $f = 50 \, \text{Hz}$.

The amplitudes of the Fourier components of the line voltage are determined by (6.30). The amplitudes of the load currents are

$$I_h = \frac{V_{h,L-N}}{Z_h} = \frac{V_{h,L-N}}{\sqrt{R^2 + (h\omega L)^2}} = \frac{V_{h,L-N}}{\sqrt{10^2 + (h \times 2\pi \times 50 \times 0.02)^2}}.$$

The calculated values of $V_{h,L-N}$ and I_h are presented in Table 6.9.

The total harmonic distortion of the load current is determined by (1.26). From this and Table 6.9 it follows that

$$\text{THD}_I = \frac{\sqrt{\sum_{h=2}^{\infty} I_{h,\text{rms}}^2}}{I_{1,\text{rms}}} = \frac{\sqrt{0.27^2 + 0.14^2 + 0.06^2 + 0.04^2}}{4.17} = 0.075 = 7.5 \, \%.$$

The most often met case is when the factor of frequency modulation is chosen so that it is an odd multiple of the number three. In this case, the phase voltages at the carrier frequency will have the same amplitude and their phase displacement will be equal to 0. As a result, the harmonics of line voltages at this frequency will be 0.

For linear modulation ($m_a \leq 1$) the amplitude of the first harmonics changes linearly with the change of the amplitude modulation factor, so the expressions for phase and line voltages have the form

$$\begin{aligned} V_{1,LN} &= m_a \frac{V_{\text{DC}}}{2} \\ V_{1,LN\text{rms}} &= m_a \frac{V_{\text{DC}}}{2\sqrt{2}} \\ V_{1,LL\text{rms}} &= \frac{\sqrt{3}}{\sqrt{2}} m_a \frac{V_{\text{DC}}}{2} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_{\text{DC}}. \end{aligned} \quad (6.33)$$

Table 6.8 Normalized Fourier coefficients V_{h_s}/V_{DC} of the line voltages of a three-phase PWM inverter [2]

hm_d Harmonic	1	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
$h = 1$	0.866	0.799	0.693	0.606	0.520	0.433	0.346	0.260	0.173	0.087
$h = m_f \pm 2$	0.275	0.232	0.190	0.150	0.114	0.081	0.053	0.030	0.013	0.003
$h = 2m_f \pm 1$	0.157	0.221	0.272	0.307	0.321	0.313	0.282	0.232	0.165	0.086

Table 6.9 The calculated values of $V_{h, L-N}$ and I_h

n	$V_{h,L-N}$ (V)	$Z_n(W)$	$I_h(A)$	$I_{h,rms}(A)$
1	63.6	11.8	6.39	4.17
5	12.73	33.0	0.38	0.27
7	9.09	45.1	0.20	0.14
11	5.79	69.8	0.08	0.06
13	4.90	82.3	0.06	0.04

For $m_a = 1$: $V_{1,LLrms} = 0.612V_{DC}$.

6.3.1 Overmodulation ($m_a > 1$)

In the case of overmodulation ($m_a > 1$) the amplitude of the control signal is larger than the amplitude of the triangular signal and the amplitude of the first harmonic is not a linear function of the amplitude modulation factor. With an increasing m_a the output voltage has a waveform similar to the waveform of the voltage of the six-step inverter. The dependence of the effective value of the line-to-line voltage fundamental harmonic on the amplitude modulation factor is shown in Fig. 6.17.

With the transition to the overmodulation region the amplitude of the output voltage fundamental harmonic increases, but this dependence is not linear. For $m_a = 3.24$ the amplitude has the maximal value $(V_{1,LLrms})_{max} = \frac{\sqrt{6}}{\pi} V_{DC}$ and this value is equal to that of a six-step inverter. Also, unlike the linear modulation, in this case there are harmonics at lower frequencies besides the harmonics at the frequency of the carrier signal and its integer multiple.

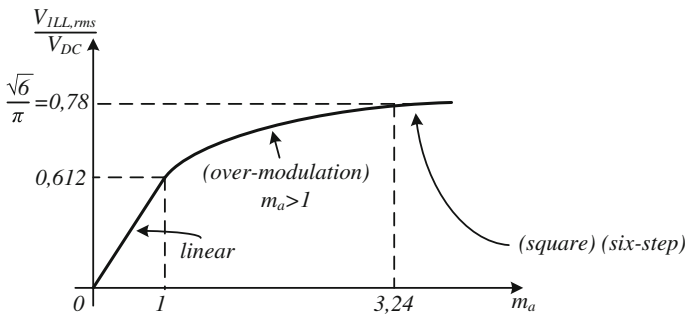


Fig. 6.17 Effective value of the fundamental harmonic of line voltage versus amplitude modulation factor [2]

6.3.2 Asynchronous PWM

For synchronous PWM the frequency modulation factor is an integer. In asynchronous PWM the switching frequency is constant, while the frequency of fundamental harmonic is changed, and m_f may not be an integer. As a consequence subharmonics may occur with a frequency lower than the frequency of the first harmonic. Although small in amplitude, these harmonics can cause significant currents in predominantly inductive loads, which should be taken into account.

6.4 Space Vector Modulation

Space vector modulation (SVM) is a very important contemporary control technique of power converters. Its main application is control of three-phase voltage controlled DC/AC converters, but it is also used for control of other types of converters such as AC/DC power converters, resonant three-phase inverters, multilevel converters, matrix converters, etc.

Today there are a number of different variants of SVM, which differ with respect to the complexity of realization and the quality of the results.

6.4.1 Space Vector Modulation—Basic Principles

A three-phase symmetrical power supply system is observed. In this system, only two currents and two voltages are linearly independent, while the third current or voltage can be expressed as a linear combination of the other two. Introducing an algorithm that includes coupling of the third phase with the first two better results can be achieved.

By applying the Clark transformation three dependent variables a, b, c are transformed into two independent variables α, β (Fig. 6.18). For simplicity it is assumed that the a -axis coincides with the α -axis in the orthogonal α, β coordinate system. The projection of the current vector $\underline{i}_s = i_a \underline{a}_0 + i_b \underline{b}_0 + i_c \underline{c}_0$, where $\underline{a}_0, \underline{b}_0, \underline{c}_0$ are the unit vectors, which lie on the a, b and c axis, respectively, to the α and β axis gives

$$\begin{aligned} i_\alpha &= i_a - \frac{1}{2}i_b - \frac{1}{2}i_c, \\ i_\beta &= \frac{\sqrt{3}}{2}i_b - \frac{\sqrt{3}}{2}i_c, \end{aligned} \tag{6.34}$$

or presented in the matrix form

Fig. 6.18 Transformation of current vector from three-phase a, b, c system to stationary α, β coordinate system

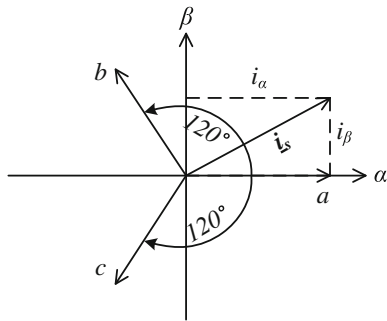
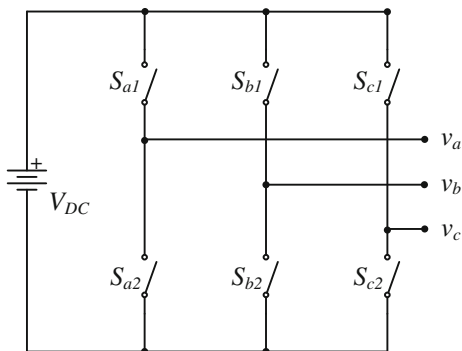


Fig. 6.19 Three-phase inverter bridge



$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}. \quad (6.35)$$

Analogously, by the same transformation of voltages it is obtained that

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \quad (6.36)$$

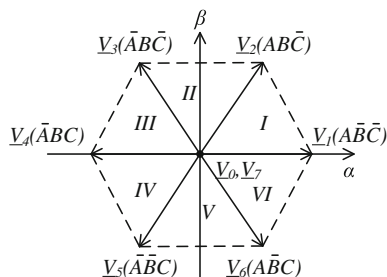
A three-phase inverter bridge controlled by the space vector modulation technique is shown in Fig. 6.19. The input voltage is DC and the output voltages are the phase voltages v_a , v_b and v_c .

It is known that the switches in the same branch of the inverter bridge must not simultaneously lead, because in that case a DC voltage source is short-circuited. This means that if one knows the states of the upper switches in the bridge, the states of the lower switches of the inverter bridge are also known and vice versa.

One binary variable is assigned to each switch of the inverter bridge, A (for S_{a1}), B (for S_{b1}) and C (for S_{c1}) and the state of the binary variable is 1 if the

Table 6.10 Applied switching sequence and phase voltages associated with the corresponding switching states

Switching sequence	Vector	Phase voltages			v_α	v_β
		v_a	v_b	v_c		
$\overline{ABC}$	$\underline{V}_0$	0	0	0	0	0
$A\overline{BC}$	$\underline{V}_1$	V_{DC}	0	0	V_{DC}	0
$AB\overline{C}$	$\underline{V}_2$	V_{DC}	V_{DC}	0	$\frac{1}{2} V_{DC}$	$\frac{\sqrt{3}}{2} V_{DC}$
$\overline{A}BC$	$\underline{V}_3$	0	V_{DC}	0	$-\frac{1}{2} V_{DC}$	$\frac{\sqrt{3}}{2} V_{DC}$
$\overline{A}\overline{B}C$	$\underline{V}_4$	0	V_{DC}	V_{DC}	$-V_{DC}$	0
$\overline{A}\overline{B}\overline{C}$	$\underline{V}_5$	0	0	V_{DC}	$-\frac{1}{2} V_{DC}$	$-\frac{\sqrt{3}}{2} V_{DC}$
$A\overline{B}C$	$\underline{V}_6$	V_{DC}	0	V_{DC}	$\frac{1}{2} V_{DC}$	$-\frac{\sqrt{3}}{2} V_{DC}$
ABC	$\underline{V}_7$	V_{DC}	V_{DC}	V_{DC}	0	0

Fig. 6.20 Vectors of stator voltages for applied control sequence 000-111 in α, β coordinate system

corresponding switch is closed, and 0 if the switch is opened. With these three binary variables eight different states can be presented, i.e., any situation in which the converter can be found (Table 6.10). Vectors of the stator voltage applied to the control sequence of binary variables 000-111 in the α, β coordinate system are presented in Fig. 6.20.

The vectors $\underline{V}_1 - \underline{V}_6$ end up in the points, which represent vertexes of a regular hexagon and they divide the regular hexagon into six segments, regular triangles (Fig. 6.20). Vectors of the stator voltage applied to the control sequence of binary variables 000-111 in the α, β coordinate system are presented in Fig. 6.20. The amplitudes of these vectors are equal among themselves and their value is

$$|\underline{V}_{\alpha\beta}| = \sqrt{v_\alpha^2 + v_\beta^2} = V_{DC}. \quad (6.37)$$

The vectors $\underline{V}_0$ and $\underline{V}_7$ are zero vectors and upon the application of these vectors the line to line voltages are equal to 0.

Using two adjacent vectors and possibly a zero vector any voltage vector whose tip lies inside a regular hexagon defined by the vectors $\underline{V}_1 - \underline{V}_6$ can be obtained. In other words, we can get a voltage vector of a desired amplitude and phase. The

obtained voltages at the inverter output v_{ab} , v_{bc} , and v_{ca} must make a symmetrical three-phase system, which means that the output voltage vector describes a circle with the corresponding frequency. This determines the voltage amplitude of the three-phase inverter controlled by the space vector modulation technique, and this amplitude is equal to the radius of a circle inscribed in the hexagon defined by the vectors $\underline{V}_1 - \underline{V}_6$:

$$\left| \underline{V_{\alpha\beta}} \right|_{\max} = \frac{\sqrt{3}}{2} V_{DC}. \quad (6.38)$$

The maximum value of the three-phase inverter phase voltage controlled by the space vector modulation technique is

$$(V_{LN\max})_{SVM} = \frac{2}{3} \left| \underline{V_{\alpha\beta}} \right|_{\max} = \frac{\sqrt{3}}{3} V_{DC}, \quad (6.39)$$

and the maximum rms value of the line to line voltage is equal to

$$(V_{LLrms})_{SVM} = \frac{\sqrt{3}}{\sqrt{2}} \frac{\sqrt{3}}{3} V_{DC} = \frac{1}{\sqrt{2}} V_{DC}. \quad (6.40)$$

The maximum rms value of the line to line voltage that can be obtained for the same input voltage by the sine pulse width modulation technique (for $m_a = 1$) (6.33) is

$$(V_{LLrms})_{SM} = \frac{\sqrt{3}}{2\sqrt{2}} V_{DC}. \quad (6.41)$$

Comparing the obtained expressions for the rms values of the line to line voltages, one obtains from (6.40) and (6.41)

$$\frac{(V_{LLrms})_{SVM}}{(V_{LLrms})_{SM}} = \frac{\frac{1}{\sqrt{2}} V_{DC}}{\frac{\sqrt{3}}{2\sqrt{2}} V_{DC}} = \frac{2}{\sqrt{3}}. \quad (6.42)$$

From Eq. (6.42) one can conclude that for the space vector modulation technique and the same input voltage, a higher effective value of the line to line voltage can be obtained, than if the sine PWM technique is applied.

6.4.2 Application of Space Vector Modulation Technique

Suppose that the voltage vector $\underline{V}$ whose amplitude is $V = |\underline{V}|$ and the phase is $\varphi(\underline{V}) = \vartheta$ should be realized (Fig. 6.21). The vector $\underline{V}$ is in first sector, so it can be realized by applying the vectors $\underline{V}_1$, $\underline{V}_2$ and one zero vector $\underline{V}_0$ or $\underline{V}_7$ (Fig. 6.22). The period

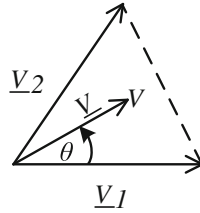


Fig. 6.21 Reference vector and vectors defining the boundaries of the sector in which is the reference vector

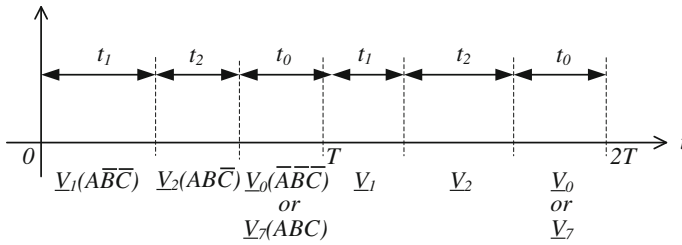


Fig. 6.22 Control sequence generating the reference voltage vector $\underline{V}$

T divided into three time intervals, the interval t_1 in which the vector $\underline{V}_1$ is applied, t_2 in which the vector $\underline{V}_2$ is applied and the interval t_0 when a zero vector is applied.

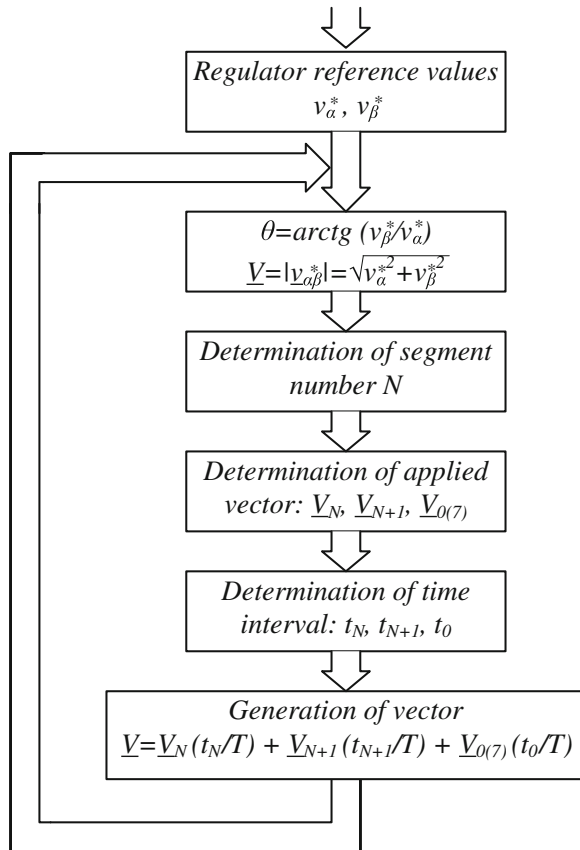
The times t_1 , t_2 , and t_0 are determined by the following expressions

$$\begin{aligned} t_1 &= \frac{V}{|V_{\alpha\beta}|_{\max}} T \sin\left(\frac{\pi}{3} - \vartheta\right) \\ t_2 &= \frac{V}{|V_{\alpha\beta}|_{\max}} T \sin(\vartheta) \\ t_0 &= T - t_1 - t_2. \end{aligned} \quad (6.43)$$

In the next period, it was assumed that the amplitude of the vector $\underline{V}$ is constant and that it remains in the first quadrant, the angle θ is changed, and thus the time intervals t_1 and t_2 are changed. The implementation of the space vector modulation algorithm is presented by the block diagram in Fig. 6.23. Based on the reference value obtained from the controller $(v_{\alpha}^*, v_{\beta}^*)$, the amplitude $|V^*|$ and the phase $\theta^* = \varphi(\underline{V}^*)$ the reference vector $\underline{V}^*$ is determined. The angle θ^* determines the segment containing the vector $\underline{V}^*$ from the condition

$$0 \leq \vartheta^* - (N - 1) \frac{\pi}{3} < \frac{\pi}{3}. \quad (6.44)$$

Fig. 6.23 Implementation of space vector modulation algorithm



When the segment N is determined, the vectors $\underline{V}_N$ and $\underline{V}_{N+1}$ are determined as well as the time intervals in the which vectors $\underline{V}_N$, $\underline{V}_{N+1}$ and the zero vector $\underline{V}_{0(7)}$ should be applied.

The control of switches in the inverter is such that the following voltage vector is realized:

$$\underline{V}^* = \underline{V}_N \frac{t_N}{T} + \underline{V}_{N+1} \frac{t_{N+1}}{T} + \underline{V}_{0(7)} \frac{T - (t_N + t_{N+1})}{T}. \quad (6.45)$$

In order to obtain the vector $\underline{V}$, the vectors $\underline{V}_1$, $\underline{V}_2$ and $\underline{V}_{0(7)}$ can be applied in a different order, direct sequencing $\underline{V}_1$, $\underline{V}_2$ and $\underline{V}_{0(7)}$ and inverse sequencing $\underline{V}_2$, $\underline{V}_1$ and $\underline{V}_{0(7)}$. The waveforms of phase voltages when direct sequencing and one zero vector are applied, for example $\underline{V}_0(\overline{ABC})$, are shown in Fig. 6.24.

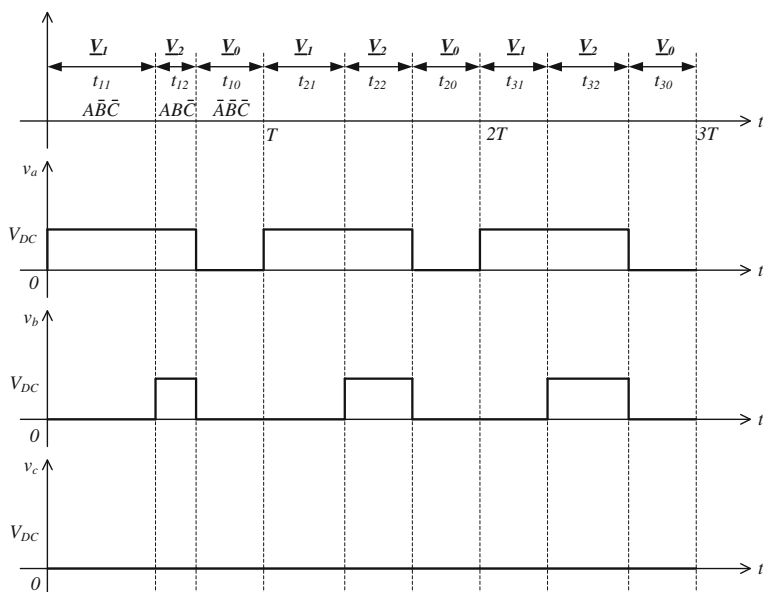


Fig. 6.24 Waveforms of phase voltages when direct sequencing and zero vector $\underline{V}_0(\underline{ABC})$ are applied

6.4.3 Direct and Inverse Sequencing

To prevent greater heating, the zero vector can be alternatively applied first to one group of switches and then to another group (one group of switches remains longer in the on state), so that the vector $\underline{V}_0$ is used in the even segments and the vector $\underline{V}_7$ in the odd segments. If direct and inverse sequencing are alternatively applied we get $d-i$ or $i-d$ sequencing. Figure 6.24 shows $d-i$ sequencing with changing of zero vector. By such sequencing, there is only one switch commutation during the period T , i.e., a total 3-switch commutation in the inverter during one period is obtained. Choosing the appropriate sequencing techniques and the zero vector, optimization with respect to the number of switch commutation and switch stresses can be achieved. Inverse sequencing with a change of zero vector is shown in Fig. 6.25.

As previously mentioned, there are several different variants of SVM. A very important application of this technique is for the multilevel converter, which will be more discussed in Chap. 10.

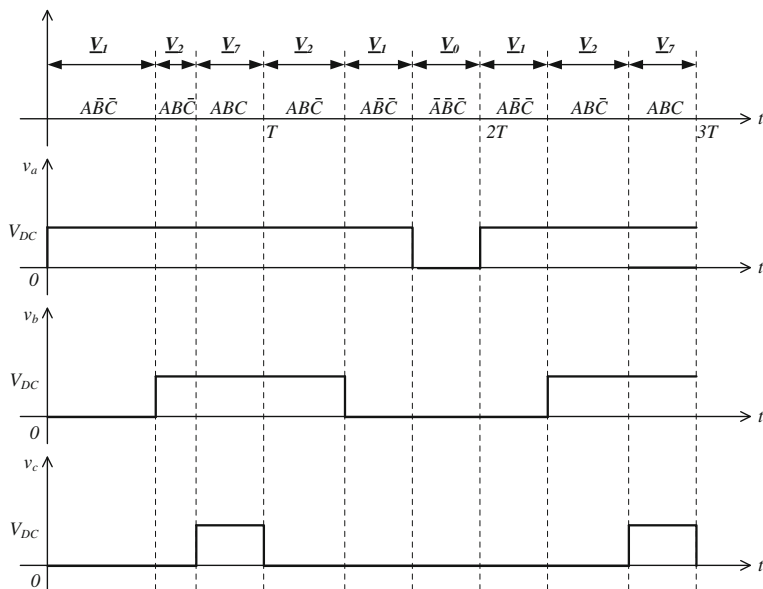


Fig. 6.25 Waveforms of phase voltages when inverse sequencing and changing of zero vector are applied

6.5 Real Drive Influence

In the previous considerations of inverters the switches have been assumed ideal. Therefore, simultaneous closing of one switch and opening of the other in the same arm of the bridge was possible. In reality, however, this cannot be done because there exist finite closing and opening times of the switches. During the transient regimes of ideally driven switches (Fig. 6.26a) the primary source could be short-circuited by the switches S_1 and S_4 (Fig. 6.26a). Namely, while one of the switches is closing, the other is opening and within certain interval they are both conducting. To avoid this, the closed switch has to open before the open switch starts closing. Therefore, in reality there has to be a time shift Δt (Fig. 6.26c) between the change of states of the switches in the same arm. The interval Δt ranges from several to several tens of microseconds for fast switches, while for the slow switches it is several hundreds of microseconds. Several names are used for the interval Δt : idling time, dead time, non-overlap time, etc. This interval introduces a certain offset in the output voltage. For PWM inverters this offset is approximately determined by

$$\Delta V_0 = \begin{cases} \frac{2\Delta t}{T_s} V_{DC}, & i_0 > 0 \\ -\frac{2\Delta t}{T_s} V_{DC}, & i_0 < 0, \end{cases} \quad (6.46)$$

where T_s is the cycle of the carrier signal.

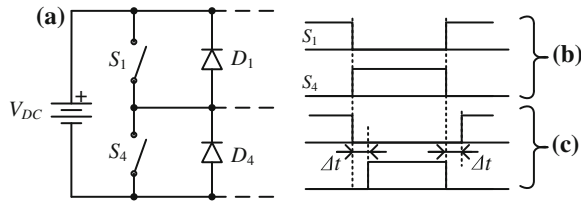


Fig. 6.26 One arm of the inverter bridge (a) and the states of ideal (b), and real switches (c)

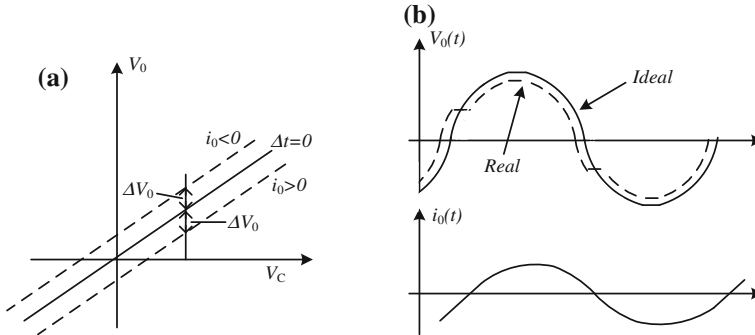


Fig. 6.27 The real (dashed) and ideal (full line) characteristics $V_0(V_c)$ of PWM inverter (a) and the influence of idling time Δt on output voltage (b)

The transfer characteristic $V_0(V_c)$ for the case with ideal switches crosses the origin (Fig. 6.27a), whereas with real switches it is shifted by $\pm\Delta V_0$, where the sign depends on the direction of the output current. The influence of Δt to the output voltage is illustrated in Fig. 6.27b.

In the design of an inverter, or more precisely of its control module, it is necessary to introduce the non-overlap time. It is determined on the basis of the dynamic pulse characteristic of the semiconductor switches at given loads.

Problems

- 6.1 The single-phase full-bridge inverter from Fig. 6.2a has a square-wave voltage across a series R - L load. The switching frequency is 50 Hz, the DC input voltage is 250 V, and the load is a serial connection of $R = 10\ \Omega$ and $L = 50\text{ mH}$.
 - (a) Determine expression for the load current and
 - (b) The power absorbed by the load.
- 6.2 The square-wave inverter from Fig. 6.2 has a DC source $V_{DC} = 250\text{ V}$ and the load is a serial R - L connection with $R = 10\ \Omega$ and $L = 20\text{ mH}$. The switching frequency is 50 Hz.

- (a) Determine the peak value of the load current in a steady state.
 - (b) Draw the waveform of the load current and determine the time intervals when each switch component is conducting.
- 6.3 A single-phase full-bridge inverter has a DC source 150 V, and the load is a serial R - L connection with $R = 10\ \Omega$ and $L = 20\text{ mH}$. The switching frequency is 50 Hz, and the switching scheme is shown in Fig. 6.7a.
- (a) Determine the angle α , so the rms value of the output voltage at the fundamental frequency is 117 V.
 - (b) Determine the THD of the load current.
- 6.4 Calculate the rms values of the fundamental harmonic and some of the higher harmonics of a single-phase inverter based on PWM if $V_{DC} = 300\text{ V}$, $m_a = 0.8$, $m_f = 39$, and $f_1 = 47\text{ Hz}$.
- 6.5 A DC source supplies an inverter with bipolar PWM control. The effective value of the output voltage on the fundamental frequency of 50 Hz is 220 V. The load is a serial R - L connection with a resistance $R = 10\ \Omega$ and an inductance $L = 50\text{ mH}$.
- (a) Specify the amplitude modulation ratio if the DC voltage is 444 V.
 - (b) If the frequency modulation ratio is 21, determine the THD of the load current.
- 6.6 A full-bridge single-phase PWM inverter has a DC source 150 V, and the load is a serial R - L connection with $R = 10\ \Omega$ and $L = 20\text{ mH}$. The fundamental frequency is 50 Hz and the amplitude modulation factor is 0.8. Determine the THD of the load current if $m_f = 15$ when
- (a) bipolar PWM is applied,
 - (b) unipolar PWM is applied.
- 6.7 The switches of the six-step inverter from Fig. 6.14 are controlled according to the time diagram shown in Fig. 6.15b.
- (a) Draw the waveforms of currents through the switches and the diodes.
 - (b) Draw the waveforms of the phase voltages v_a , v_b , and v_c .
 - (c) For the voltage v_a calculate the rms value and the amplitude of the first harmonic.
- 6.8 The six-step three-phase inverter from Fig. 6.14 has a 511 V DC voltage source, and its output frequency varies in the range 25–50 Hz. The load is Y-connected with a serial connection of $R = 10\ \Omega$ and $L = 20\text{ mH}$ in each phase. Determine the range of the rms values of the fundamental component of the load current when the frequency is varied.
- 6.9 To control the three-phase inverter the space vector modulation technique is used. The reference voltage vector $\underline{V}$ has an amplitude of $0.6 V_{DC}$, a frequency 50 Hz, and a phase $\theta = 75^\circ$.

- (a) Determine the reference phase voltages v_a , v_b and v_c .
- (b) Define the switching frequency and the corresponding vectors, which should be applied to realize the reference vector.
- (c) Define the time intervals in which the corresponding vectors are applied.

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2. Hart D.W.: Introduction to Power Electronics, Prentice-Hall (1997)

Chapter 7

AC/DC Converters–Rectifiers

An AC/DC converter usually interconnects the primary source and a DC/DC controller (Fig. 7.1). In the supply systems where a high stability of the DC voltage is not necessary, the application of DC/DC controllers is not required. An AC/DC converter usually consists of:

- transformer,
- rectifier,
- filter, and
- control block of the rectifier.

The transformer adjusts the primary AC source to the input of the rectifier and separates galvanically the primary source (usually the mains network) from the load. The rectifier converts (rectifies) the AC energy to DC. In that sense, it is the basic subassembly of an AC/DC converter and because of that many people imply that the rectifier is a complete AC/DC converter. A rectifier comprises diodes and/or thyristors. The voltage and the current at the output of a rectifier are subject to considerable pulsations and for that reason their filtering is necessary. The filters are usually very simple and comprise of a capacitor and/or inductor.

The control block of the rectifier controls the angle of the thyristor conduction and in this way controls the output voltage and current. In such a situation, one talks of controlled rectifiers. The controlled rectifier consists of thyristors or transistors. A diode rectifier is not controlled. In that case, the rectifier does not have a control block. In some cases, a transformer is not required. When the primary AC voltage is directly fed to the input of the rectifier it is then, as a rule, a controlled rectifier.

This chapter is dedicated to rectifiers. They can be divided on the basis of the mode of their connection to the AC network, or on the basis of the mode of using the energy from the AC source, or on the basis of the character of the output voltage and the degree of its control. With respect to the mode of using the energy from the AC source rectifiers can be one-sided (half-wave) or two-sided (full-wave).

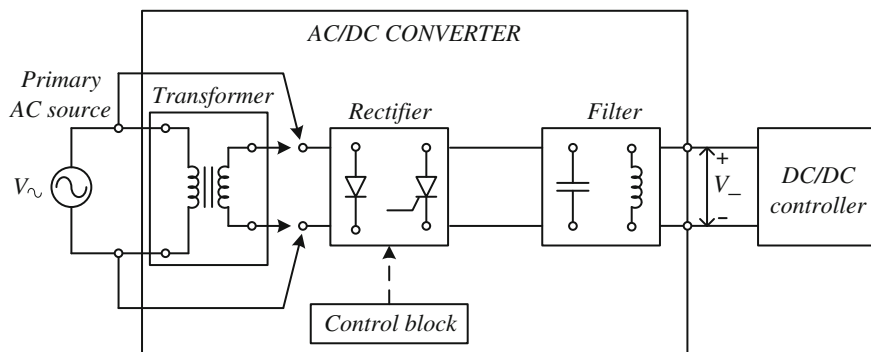


Fig. 7.1 The block diagram of an AC/DC converter

7.1 Half-Wave Single-Phase Rectifiers

The simplest rectifier includes only one diode (Fig. 7.2a). The diode conducts only during the positive half-cycle of the secondary voltage. If the voltage drop across the diode is neglected, the voltage across the load will be equal to the secondary voltage, i.e.,

$$v_o = v_s = V_{SM} \sin(\omega t), \quad 2k\pi \leq \omega t \leq (2k+1)\pi, \quad k = 0, 1, 2, \dots \quad (7.1)$$

where V_{SM} is the amplitude of v_s . During the negative half-cycle the diode is blocked and $v_o = 0$. Therefore, one obtains a sequence of pulses (positive half-cycles) across the load (Fig. 7.2b). These pulses ought to be averaged and for that purpose filters are used at the output of the rectifier. The DC component of the output voltage is determined by

$$V_o = \frac{1}{2\pi} \int_0^\pi V_{SM} \sin(\omega t) d(\omega t) = \frac{V_{SM}}{\pi}, \quad (7.2)$$

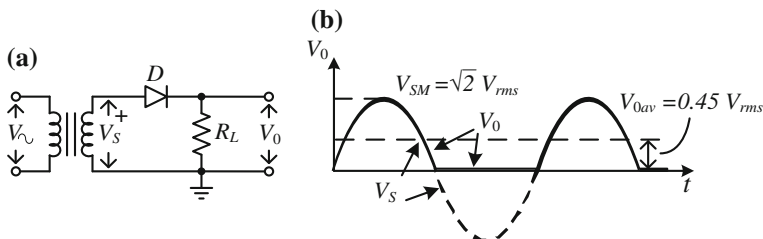


Fig. 7.2 Half-wave rectifier (a) and its output voltage (b)

where as the root mean square value of the voltage V_S is

$$V_{\text{rms}} = \sqrt{\frac{1}{2\pi} \int_0^\pi [V_{\text{SM}} \sin(\omega t)]^2 d(\omega t)} = \frac{V_{\text{SM}}}{\sqrt{2}}. \quad (7.3)$$

Thus the DC component is

$$V_o = (\sqrt{2}/\pi) V_{\text{rms}} \approx 0.45 V_{\text{rms}}.$$

The relatively small value of the DC component and the connection of the transformer to the load only during one half-cycle point are a poor use of the energy source. The average value of the current is not zero, which has an adverse influence on the transformer characteristics. In addition, the output voltage ripple is quite high. Due to all these reasons, a half-wave rectifier is very seldom used.

7.2 Full-Wave Rectifiers

Two-sided rectifiers rectify both half-cycles. For this reason, they are often called the full-wave rectifiers. Two types can be distinguished: rectifiers having a center-tapped secondary winding and two-sided rectifiers having a diode (thyristor) bridge (Graetz bridge).

A single-phase full-wave rectifier having a center-tapped secondary winding has two diodes (Fig. 7.3a). When the input voltage is positive D_1 is conducting and D_2 is blocked. During the negative half-cycle D_2 is conducting and D_1 is blocked. The direction of the current in both cases is the same so that the negative half-cycle

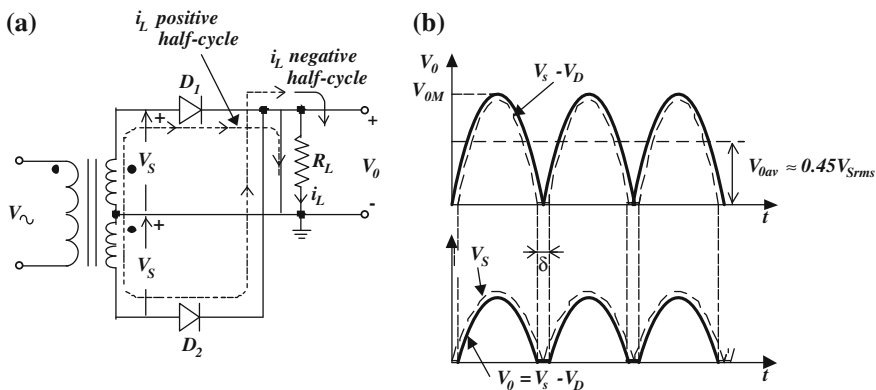


Fig. 7.3 Single-phase full-wave rectifier having center-tapped secondary (a) and its output voltage (b)

appears on the positive side at the output (Fig. 7.3b). During each of the half-cycles, the current flows only through one half of the secondary winding, consequently the secondary winding has to contain a double number of turns.

The maximum reverse voltage across the diode is twice the amplitude of the secondary voltage. Therefore, the breakdown voltage of the diode has to be

$$BV_D > 2V_{SM}. \quad (7.4)$$

The maximum permitted current through the diode has to be higher than the maximum expected load current.

In reality, the voltage across a conducting diode is greater than zero and, depending upon the load current, it amounts 0.7 to 1 V. The voltage V_D of the diode can justifiably be neglected only if $V_{oav} \gg V_D$. At small voltages, the influence of V_D should be taken into account. The output voltage is zero during δ/ω , where δ is the angle when both diodes are blocked (Fig. 7.3b).

The second type of the full-wave rectifier is a Graetz bridge rectifier (Fig. 7.4a). It consists of four diodes in a bridge circuit. During each half-cycle, one pair of the diodes is conducting (during the positive one D_1 and D_2 , during the negative D_3 and D_4). Here too the load current in both half-cycles flows in the same direction so the output voltage is of the same polarity. The DC component of the full-wave rectifiers is twice the current of the half-wave rectifiers, i.e.,

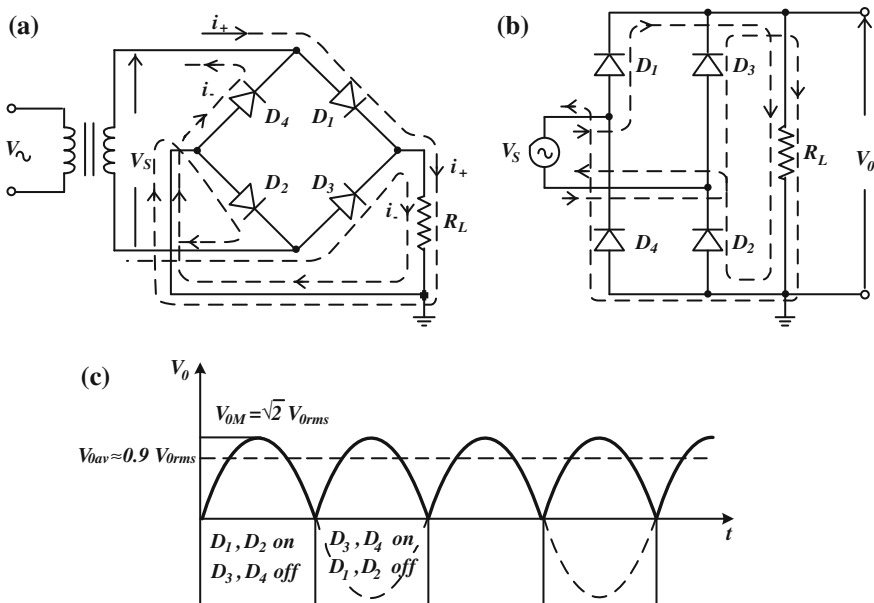


Fig. 7.4 A Graetz (bridge) full-wave rectifier (a), an alternative representation (b), and the waveform (c)

$$V_0 = \frac{2}{\pi} V_{SM} = 0.9 V_{\text{srms}}. \quad (7.5)$$

In addition, the ripple is considerably smaller. The diodes of the Graetz bridge should have the maximum current higher than the maximum load current and the breakdown voltage BV_D higher than the amplitude of the secondary voltage. i.e.,

$$BV_D > V_{SM}. \quad (7.6)$$

By comparing full-wave rectifiers it may be concluded that a Graetz bridge, although having two more diodes, has an advantage because it uses a transformer having one half of the number of turns in the secondary and diodes having one half of the breakdown voltage. Of course the need for four diodes is a disadvantage of the Graetz bridge, not from the point of view of the used-up material but because of the doubled voltage across the diodes and the doubled dissipation in them. This is particularly inconvenient at small DC voltages, when the voltage drop across the diodes cannot be neglected. Because of that the efficiency factor is considerably reduced.

It should be emphasized that the manufacturers offer the Graetz bridge as an element in a single case. Also the diode pairs for the other type of the full-wave rectifier are manufactured as a single element.

By altering the directions of the diodes, a negative voltage rectifier is obtained. Some electronic systems (e.g., the systems containing linear electronic circuits) require positive and negative voltages with respect to the ground. The rectifiers of such power supplies are designed using one Graetz bridge and a transformer having the center-tapped secondary winding (Fig. 7.5a). Now, both halves of the secondary are active throughout the cycle. For instance, during the positive half-cycle by the upper part of the secondary and the diode D_1 – the load R_L is supplied by the current

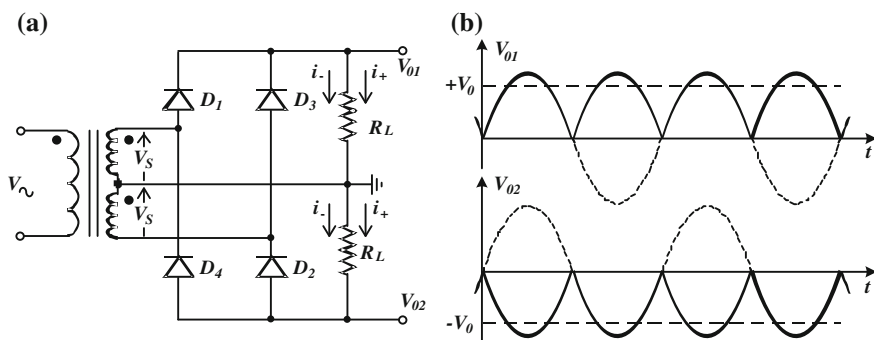


Fig. 7.5 The double full-wave single-phase rectifier (a) and the waveforms of the output voltages V_{01} and V_{02} (b)

i_+ . At the same time, by the lower part of the secondary and the diode D_2 the load R_L is supplied by the current i_+ . During the negative half-cycle, the diodes D_3 and D_4 provide the flow of the current i_- through the load R_L in the same direction as the current i_+ . The waveforms of the output voltages are shown in Fig. 7.5b.

7.2.1 Commutation of Current

The commutation of the currents (taking over the current by one group of diodes from the other group of diodes) in ideal rectifiers occurs instantly. In reality, however, this is not possible owing to the inductances in the commutation loop. These inductances in the commutation loop are mainly the sums of the inductances of the commutation network referred to the secondary side of the network and the stray inductances of the windings. The commutation time is usually expressed in terms of an angle called the angle of commutation or the angle of coverage.

A real secondary circuit of a transformer can be represented by a series of connection to a generator v_s and an inductance L_S (Fig. 7.6a). Let a Graetz bridge operate in the constant output current mode. Then for an ideal rectifier ($L_S = 0$) the current of the primary source would be $i_s = +I_0$ during the positive and $i_s = -I_0$ during the negative half-cycle (Fig. 7.6e). In reality, however, the inductance L_S resists any change and at the beginning of conduction of one pair of the diodes the other pair will stay turned on for a while. This happens at the beginning of each half-cycle. Then all four diodes are conducting, the output voltage is $v_0 = 0$ (Fig. 7.6c), and the inductance L_S takes over the voltage (Fig. 7.6d).

The relationships at the beginning of the positive half-cycle will be considered. For $\omega t \geq 0$ the diodes D_1 and D_2 are conducting. Due to the action of L_S the diodes D_3 and D_4 do not turn off immediately. During their conduction, there are three current loops (Fig. 7.6b). If diodes were ideal ($V_D = 0$) the following would hold

$$v_L = L_S \frac{di_s}{dt} = v_s = V_{SM} \sin(\omega t). \quad (7.7)$$

The current of the turned on diodes D_1 and D_2 is $i_{D1} = i_{D2} = i_k$, whereas the current of the turned off diodes D_3 and D_4 is $i_{D3} = i_{D4} = I_0 - i_k$. The line current is determined by

$$i_s = -I_0 + 2i_k \quad (7.8)$$

The commutation process will go on until the current through the diodes D_1 and D_2 becomes I_0 , when the diodes D_3 and D_4 are turned off.

Therefore, the process of taking over of the current by the diodes, as a consequence of the real drive of the rectifier circuit, has an important influence on the

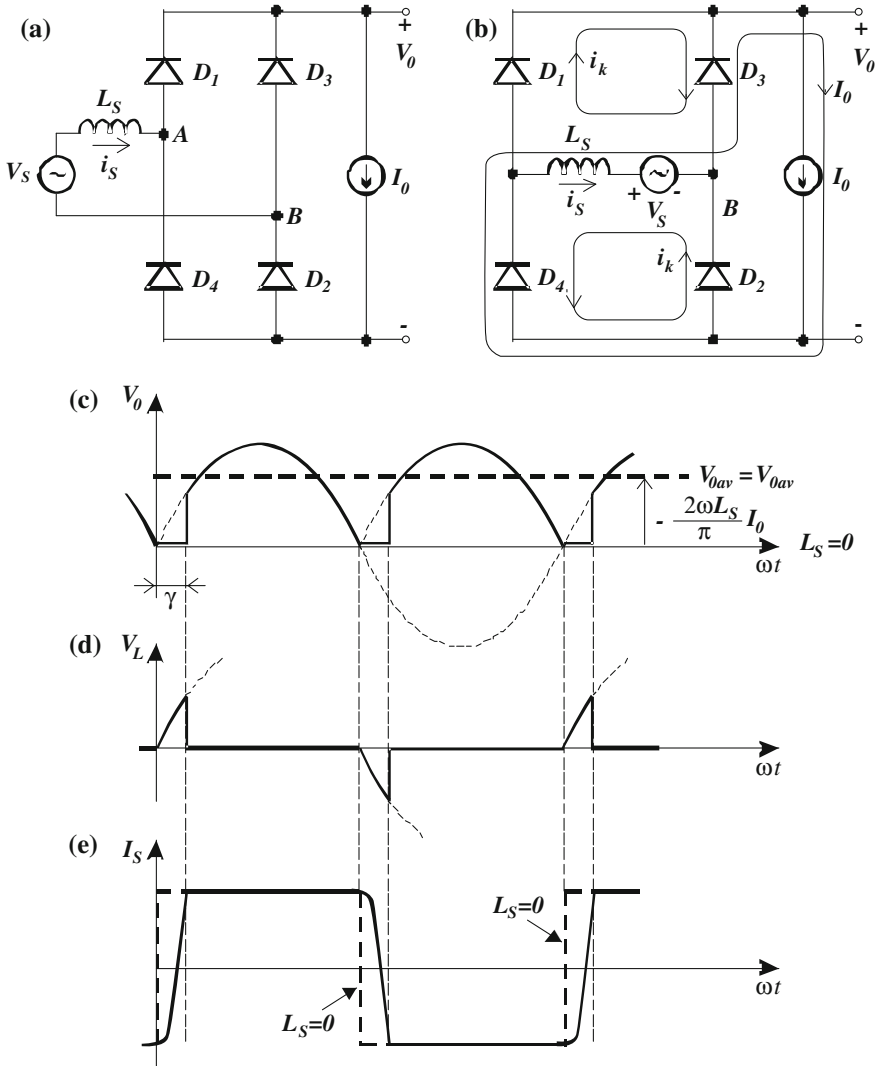


Fig. 7.6 Real drive of a Graetz bridge in the constant output current mode (a and b), constant current at the beginning of the positive half-cycle and the waveforms of the output voltage (c), voltage across inductance (d), and source current (e)

rectifier characteristics. The waveforms of the voltage and the current change and higher harmonics appear in the rectified voltage and the load current. The average value of the rectified voltage decreases and is determined by

$$\begin{aligned}
 V_{\text{oav}} &= \frac{1}{\pi} \int_{\pi}^{\pi} V_{\text{SM}} \sin(\omega t) d(\omega t) \\
 &= \frac{1}{\pi} \left[\int_0^{\pi} V_{\text{SM}} \sin(\omega t) d(\omega t) - \int_0^{\gamma} V_{\text{SM}} \sin(\omega t) d(\omega t) \right]. \quad (7.9)
 \end{aligned}$$

The solution of (7.9) gives

$$V_{\text{oav}} = \frac{2V_{\text{SM}}}{\pi} - \frac{V_{\text{SM}}}{\pi} (1 - \cos \gamma), \quad (7.10)$$

where γ is the angle of commutation. Taking (7.7) into account it follows that

$$\int_0^{\gamma} V_{\text{SM}} \sin(\omega t) d(\omega t) = \int_0^{\gamma} L_S \frac{di_s}{dt} d(\omega t) = \omega L_S \int_{-I_0}^{I_0} di_s = 2\omega L_S I_0. \quad (7.11)$$

By combining (7.11) with the second member of (7.10) one obtains

$$\cos \gamma = 1 - \frac{2\omega L_S}{V_{\text{SM}}} I_0, \quad (7.12)$$

and the average value of the output voltage is

$$V_{\text{oav}} = 0.9V_{\text{s rms}} - \frac{2\omega L_S}{\pi} I_0 = V_{\text{oav}}|_{L_S=0} - \frac{2\omega L_S}{\pi} I_0. \quad (7.13)$$

Now let the Graetz bridge operate in the constant output voltage mode (Fig. 7.7a). This situation is very close to reality when the rectifier is loaded by a large capacitor. The equivalent circuit of the rectifier is represented in Fig. 7.7b. The diodes D_1 and D_2 start conducting at an angle θ_b when $|v_s|$ reaches V_o (Fig. 7.7c), i.e.

$$V_o = V_{\text{SM}} \sin \vartheta_b. \quad (7.14)$$

The current i_o reaches its maximum at $\omega t = \theta_p$ when the voltage across the inductance becomes negative, or when the condition $|v_s| = V_o$ is met again. Owing to the symmetry of the half-cycle

$$\theta_p = \pi - \theta_b. \quad (7.15)$$

Because of the action of L_S the diodes D_1 and D_2 will stay turned off for a while until the areas A and B (Fig. 7.7d) become equal. While the current flows through the diodes

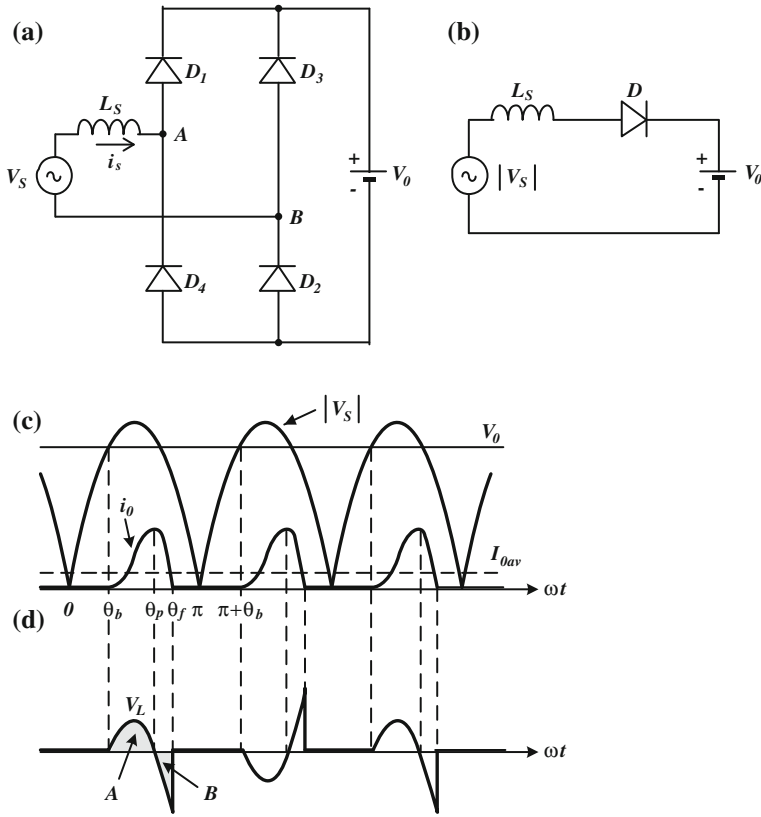


Fig. 7.7 Graetz bridge in the constant output voltage mode (a), the equivalent circuit (b), and the corresponding waveforms (c and d)

$$v_L = L_s \frac{di}{dt} = V_{SM} \sin(\omega t) - V_0. \quad (7.16)$$

By integrating (7.16) one obtains

$$i_0(\omega t) = \frac{1}{\omega L_s} \int_{\Theta_b}^{\omega t} [V_{SM} \sin(\omega t) - V_0] d(\omega t), \quad (7.17)$$

where $\theta_b \leq \omega t \leq \theta_f$. The angle θ_f when i_0 is zero again is determined from the condition

$$\int_{\Theta_b}^{\Theta_f} v_L(\omega t) d(\omega t) = \int_{\Theta_b}^{\Theta_f} [V_{SM} \sin(\omega t) - V_0] d(\omega t) = 0, \quad (7.18)$$

which corresponds to equating the surfaces A and B (Fig. 7.7d). The average value of the output current is

$$I_o = \frac{1}{\pi} \int_{\Theta_b}^{\Theta_f} i_0(\omega t) d(\omega t). \quad (7.19)$$

7.3 Output Filters

The output voltage of a rectifier varies over a very wide range, from practically zero to the maximum of the secondary voltage. For this reason at the output of a rectifier use is made of filters which reduce the harmonic currents through the load and the ripple of the output voltage. In practice, two types of filters are mostly used: the capacitive filter for small currents and the L filter for large load currents.

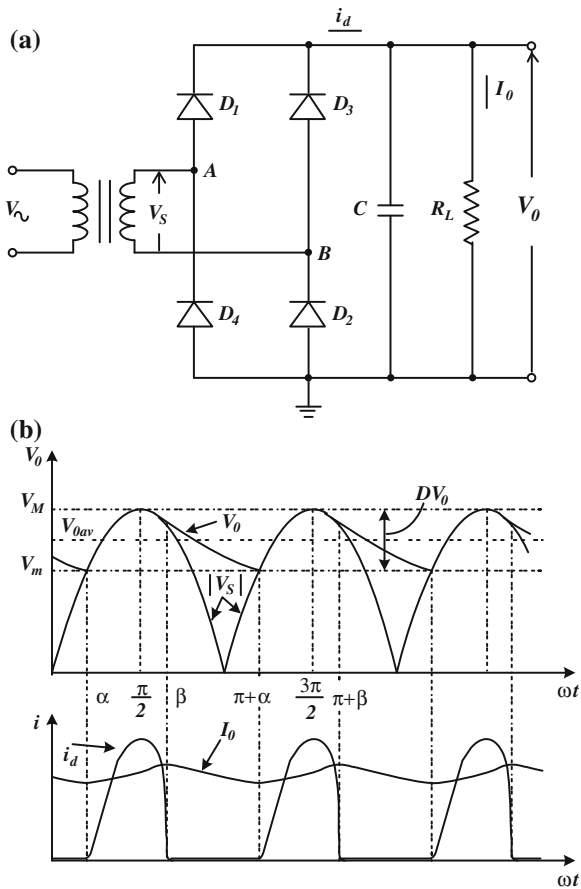
7.3.1 Capacitive Filter

The load to be supplied is usually resistive. The capacitive filter consists of only one capacitor of high capacitance, or appropriate connection of capacitors connected in parallel with the load (Fig. 7.8a). It supports the output voltage across the load and supplies the current at small values of the rectified secondary voltage. The peak-to-peak variation of the output voltage is considerably smaller than its average value. The diode pairs are conducting only at small intervals within a half-cycle when the rectified secondary voltage is higher than the voltage across the capacitor. Then $v_o = v_s$. During the remaining part of the half-cycle, the diodes are off and the capacitor discharges exponentially through the load R_L . By using the notation of Fig. 7.8b, the output voltage can be written in the following form

$$V(\omega t) = \begin{cases} |V_{SM} \sin(\omega t)|, & \alpha \leq \omega t \leq \beta \quad \text{and} \quad \pi + \alpha \leq \omega t \leq \pi + \beta \\ (D_1 \text{ and } D_2 \text{ conducting}) & (D_3 \text{ and } D_4 \text{ conducting}) \\ (V_{SM} \sin \beta) e^{-(\omega t - \beta)/(\omega R_L C)} & \text{otherwise (all diodes are off)}. \end{cases} \quad (7.20)$$

The angle β at which the diodes stop conducting can be determined by equating the slopes of functions (7.20)

Fig. 7.8 Single-phase Graetz rectifier with a capacitive filter (a) and the voltage and current waveforms (b)



$$\frac{d}{d(\omega t)} [V_{SM} \sin(\omega t)] = V_{SM} \cos(\omega t) \quad (7.21)$$

and

$$\frac{d}{d(\omega t)} [(V_{SM} \sin \beta) e^{-(\omega t - \beta)/(\omega R_L C)}] = (V_{SM} \sin \beta) \left(-\frac{1}{\omega R_L C} \right) e^{-(\omega t - \beta)/(\omega R_L C)}. \quad (7.22)$$

At $\omega t = \beta$ these slopes are equal, thus it follows

$$V_{SM} \cos \beta = \frac{V_{SM} \sin \beta}{-\omega R_L C}. \quad (7.23)$$

From (7.23) β is

$$\beta = \tan^{-1}(-\omega R_L C) = -\tan^{-1}(\omega R_L C) + \pi. \quad (7.24)$$

In practice the time constant $R_L C$ is quite large, so

$$\beta \approx \pi/2, V_{SM} \sin \beta = V_{SM}. \quad (7.25)$$

In other words, the capacitor provides the load current during $\pi/2 + k\pi \leq \omega t \leq (k+1)\pi + \alpha$; $k = 1, 2, \dots$. The angle α can be determined from the condition

$$|V_{SM} \sin(\pi + \alpha)| = (V_{SM} \sin \beta) e^{-(\omega t - \beta)/(\omega R_L C)}. \quad (7.26)$$

Since $\beta \approx \pi/2$, then

$$|\sin(\pi + \alpha)| = e^{-(\pi/2 + \alpha)/(\omega R_L C)}. \quad (7.27)$$

The minimum value of the output voltage is determined by

$$V_{om} \approx V_{SM} e^{-(\pi/2 + \alpha)/(\omega R_L C)}. \quad (7.28)$$

Usually $\omega R_L C \gg \pi$ so $\alpha \approx \pi/2$ and

$$V_{om} \approx V_{SM} e^{-\pi/(\omega R_L C)} = V_{SM} \sin \alpha. \quad (7.29)$$

The peak-to-peak variation of the output voltage is determined by

$$\Delta V_o = V_{SM} - V_{om} \approx V_{SM}(1 - e^{-\pi/(\omega R_L C)}). \quad (7.30)$$

Taking into account that $\omega R_L C \gg \pi$,

$$e^{-\pi/(\omega R_L C)} \approx 1 - \frac{\pi}{\omega R_L C}, \quad (7.31)$$

the variation of the output voltage is

$$\Delta V_o \approx V_{SM} \frac{\pi}{\omega R_L C} = \frac{V_{SM}}{2f R_L C}. \quad (7.32)$$

It should be emphasized that (7.30) is a rough estimate of the variation of V_o basically because of the rough estimate of the angle α at which the diodes start conducting. Usually $\alpha < \pi/2$.

Example 7.1 A fullwave rectifier (Fig. 7.8a) with a capacitive filter has $V_{seff} = 220$ V, $f = 50$ Hz, $R = 220$ Ω and $C = 100$ μ F.

(a) Determine an expression for the load current.

- (b) Determine the average value of the load current.
 - (c) Calculate the maximum change of the load voltage.
 - (d) Draw the waveforms of the load voltage and the current through the capacitor using PSPICE software.
- (a) Voltage on the load can be calculated following the expression (7.20). The angle β at which the diodes stop conducting can be determined by equating the slopes of functions (7.20). Solving Eq. (7.21) one obtains

$$\beta = \pi - \arctg(\omega RC) = 1.71 \text{ rad.}$$

The angle α is determined from the condition that the capacitor begins to recharge (7.26). Solving Eq. (7.26) one obtains $\alpha = 0.76$. The load current is equal to v_p/R , so the expression for the load current can be written as

$$i_p(\omega t) = \begin{cases} 1.41 \sin(\omega t) [A], & 0.8 \leq \omega t \leq 1.71 \\ 1.4e^{\frac{-\omega t - 1.71}{6.91}} [A], & 1.71 \leq \omega t \leq \pi + 0.8 \end{cases}$$

- (b) The average value of the load current is

$$I_{psr} = \frac{1}{\pi} \left[\int_{0.8}^{1.71} 1.41 \sin(\omega t) d(\omega t) + \int_{1.71}^{\pi+0.8} 1.4e^{\frac{-\omega t - 1.71}{6.91}} d(\omega t) \right] = 1.22 \text{ A.}$$

- (c) The maximum change in the load voltage is determined as the difference between the maximum and the minimum voltage on the load (Figs. 7.9 and 7.10)

$$\Delta V_p = V_{p\max} - V_{p\min} = V_{SM} - V_{SM} \sin \alpha = 87.9 \text{ V.}$$

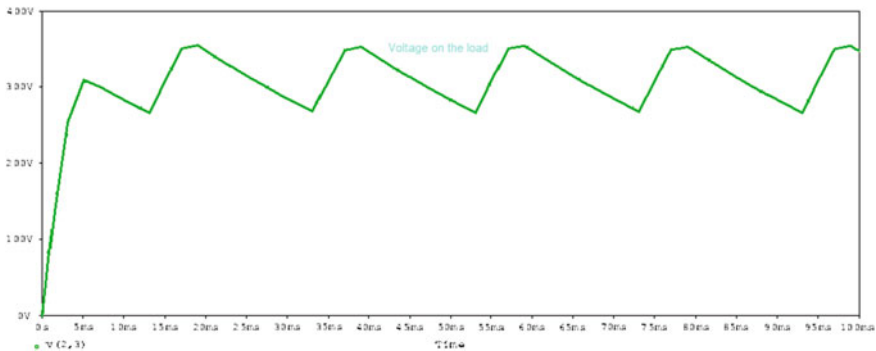


Fig. 7.9 Voltage on the capacitor for the circuit shown in Fig. 7.8a

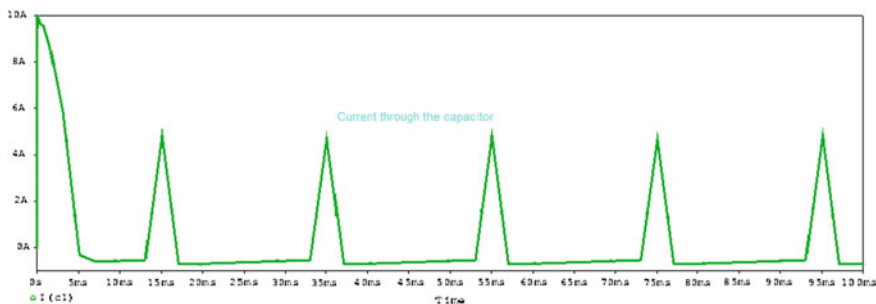


Fig. 7.10 Current through the capacitor for the circuit shown in Fig. 7.8a

7.3.2 L Filter

For supplying large load currents use is made of L filters consisting of a series inductance L and a parallel capacitance C (Fig. 7.11a). The action of these filters distinctly depends on the load current. When this current is small, the filter behaves as if it were capacitive since the influence of the choke can be neglected because the accumulated energy ($LI^2/2$) is small. Then the current through the diodes flows only in a fraction of the half-cycle, in the vicinity of the maximum value of the mains voltage (Fig. 7.11b), when the input voltage of the filter is higher than the output voltage. By increasing the load current, the energy of the choke increases and also increases the angle of conduction of the diodes owing to the counter-electromotive force supporting the existing current through the choke.

In this process, the output voltage decreases with increasing the load current. This operating mode is called the mode of the discontinuous choke current. The current through the choke will flow throughout the whole cycle (the continuous mode) if the load current is higher than certain critical value I_{0k} . Then the angle of diode conduction is 180, i.e., the diodes are conducting alternately throughout the whole half-cycle. In this mode ($I_0 > I_{0k}$), the average value of the output voltage does not depend on the load current (Fig. 7.12). Then the L filter can be analyzed in the steady state harmonic mode driven by a full-wave rectified sine function whose Fourier series expansion is

$$V_i = \frac{2V_{SM}}{\pi} - \frac{4V_{SM}}{3\pi} \cos(2\omega t) - \frac{4V_{SM}}{15\pi} \cos(4\omega t) + \dots \quad (7.33)$$

To make higher harmonics negligible, it is necessary to have the impedance of the capacitor at these frequencies much lower compared to the impedance of the choke, i.e.,

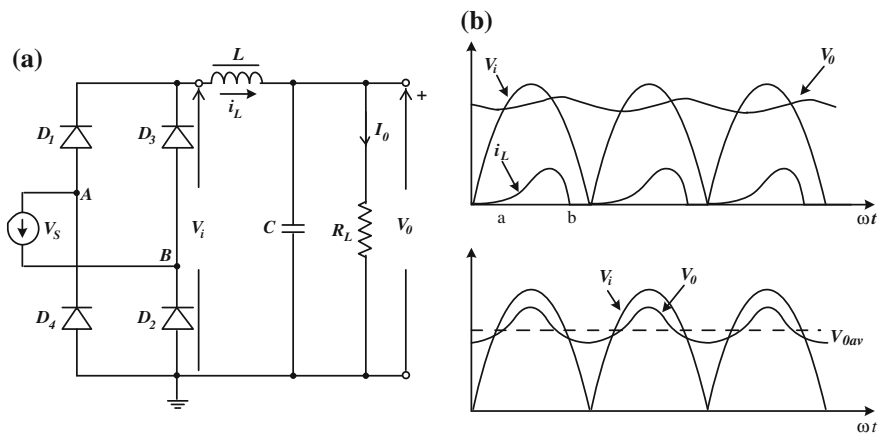
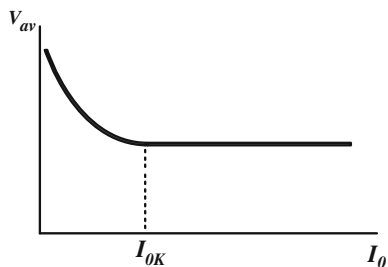


Fig. 7.11 Single-phase Graetz bridge with an L filter (a) and the characteristic waveforms in the modes of discontinuous (b) and continuous choke current (c)

Fig. 7.12 Regulation characteristics of the L filter



$$X_C = 1/2\omega C \ll X_L = 2\omega L, \quad (7.34)$$

This condition is usually satisfied since the capacitance C and the inductance L are quite large. By neglecting the harmonics higher than the second, it is obtained that the output voltage is the sum of the average value and the second harmonic (Fig. 7.11c). The average value is

$$V_{osr} = 2 \frac{V_{SM}}{\pi}, \quad (7.35)$$

and the amplitude of the second harmonic across the load, since $1/(2\omega C) \ll R_L$, is

$$V_{o2} \approx \frac{1}{2\omega L} \frac{4V_{SM}}{3\pi} = \frac{V_{SM}}{3\pi\omega^2 LC}. \quad (7.36)$$

The ripple factor is

$$FT = \frac{V_{o2}}{V_{osr}} = \frac{1}{6\omega^2 LC} \quad (7.37)$$

and in this mode is not dependent on the load current. The critical load current is determined from the condition of continuity of the current through the choke. In this case the DC load current, $I_o = V_{oav}/R_L$, should be higher or equal to the amplitude of the second harmonic of the choke current $I_{L2\omega}$. If the impedance of the capacitor is much lower than the load resistance, i.e., $1/(2\omega C) \ll R_L$ then

$$I_{L2} = \frac{2V_{SM}}{3\pi\omega L} = I_{0k}. \quad (7.38)$$

From the condition of continuity $I_o > I_{0k}$ it will be met if

$$R_L \leq 3\omega L. \quad (7.39)$$

In the design of an L filter, one starts from the maximum load resistance R_{Lmax} . For this value, on the basis of (7.39), the critical inductance is determined as:

$$L_K = R_{Lmax}/(3\omega). \quad (7.40)$$

The capacitance is determined from the relation $1/(\omega C) \ll L_K\omega$. If the load resistance varies over a wide range, and if the output is a fixed load the critical inductance is calculated according to this value.

7.4 Voltage Doublers

The circuit for doubling a DC voltage consists of two half-wave rectifiers connected to the same secondary but with reverse connected diodes and with two series capacitors (Fig. 7.13a). During the positive half-cycle the capacitor C_1 is charged through the diode D_1 and during the negative half-cycle the capacitor C_2 is charged through the diode D_2 . The capacitances are equal and quite large. Figure 7.13b shows the voltage waveforms across the capacitor and across the output. Even though the mains voltage is rectified as if by a full-wave rectifier, each of the capacitor discharges as in a half-wave rectifier. For this reason the ripple is quite high and it increases with the reduction of the load resistance. Therefore this circuit is used only at small load currents.

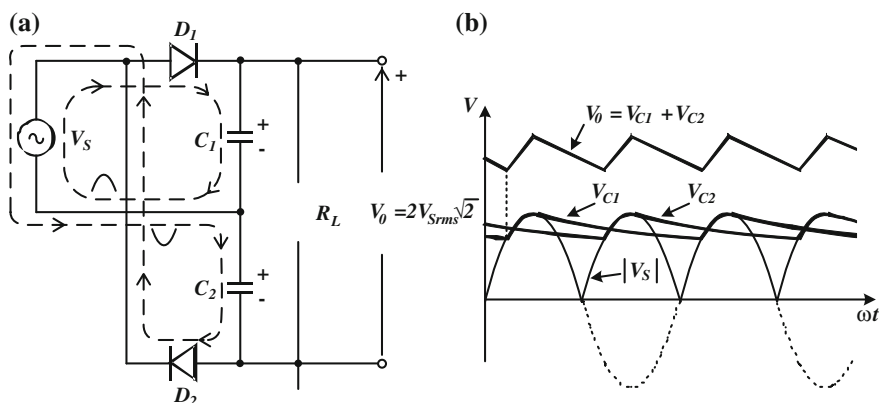


Fig. 7.13 The voltage doubler (a) and voltage waveforms (b)

7.5 Three-Phase Rectifiers

In industrial applications, where three-phase AC voltages are available, it is recommendable to use three-phase rectifiers. At the output of this type of rectifier compared to the single-phase rectifiers, the DC component is higher, the ripple of the output voltage is lower, and the output power is higher. Three-phase rectifiers have favorable features for equipment and installations requiring high power, where very high DC currents and relatively high voltages are necessary. Most frequently these are full-wave bridge rectifiers (Fig. 7.14a). As in the single-phase rectifiers, a simple capacitive filter is used at the output.

In order to facilitate understanding, a real rectifier circuit (Fig. 7.14a) is simplified by assuming an idealized drive and by replacing a real load by a current generator (Fig. 7.14b). Due to neglecting the series inductances of the driving generators (Fig. 7.14b), the output current I_0 flows through one diode of the upper

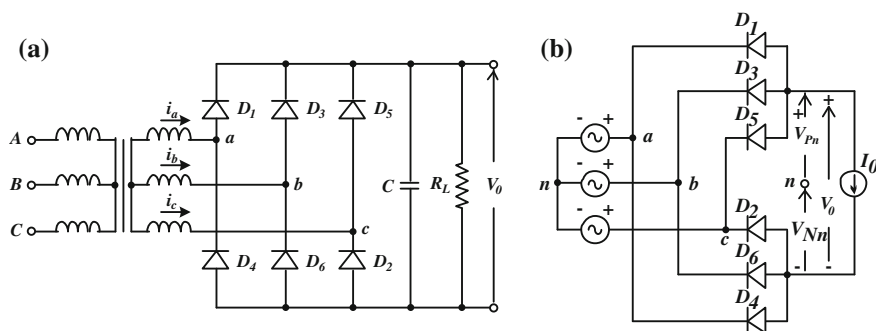


Fig. 7.14 Three-phase bridge rectifier (a) and its ideal equivalent circuit (b)

group and one diode of the lower group of diodes. In the upper group the diode having the anode at the highest potential will conduct. The other two are reverse biased, thus they are off. In the lower group only the diode having the cathode at the lowest potential will conduct. The output voltage is equal to the difference of the voltages at the points P and N compared to the neutral point n, i.e.,

$$V_o = V_{Pn} - V_{Nn}. \quad (7.41)$$

Since one diode of the upper group and one diode of the lower group are always conducting, the voltages V_{Pn} and V_{Nn} are equal to one of the AC voltages V_{an}, V_{bn} or V_{cn} (Fig. 7.15a). So, the output voltage consists of the six segments of the line voltage during one cycle (Fig. 7.15b). For this reason, these rectifiers are often called the six-pulse rectifiers. The output voltage during one cycle practically consists of six sinusoidal peaks (Fig. 7.15b) thus its ripple is small and the average value is close to the amplitude of the line voltages. Each diode conducts during 120° . They conduct in pairs (6, 1), (1, 2), (2, 3), (3, 4), (4, 5), (5, 6), and (6, 1). The phase currents are determined by

$$i_a = i_{d1} - i_{d4}, i_b = i_{d3} - i_{d6}, i_c = i_{d5} - i_{d2} \quad (7.42)$$

and are represented in Fig. 7.15c. Thus the current of, e.g., the phase a is

$$i_a = \begin{cases} I_0 & \text{if } D_1 \text{ conducting} \\ -I_0 & \text{if } D_4 \text{ conducting} \\ 0 & \text{if } D_1 \text{ and } D_4 \text{ are turned off} \end{cases} \quad (7.43)$$

The maximum reverse voltage of a diode is equal to the amplitude of the line voltage. The output voltage is cyclic with the cycle $\pi/3$. The corresponding Fourier series is

$$v_o(t) = V_0 + \sum_{n=6,12,18}^{\infty} V_n \cos(n\omega_0 t + \pi), \quad (7.44)$$

where the average value is

$$V_0 = \frac{1}{\pi/3} \int_{\pi/3}^{2\pi/3} V_{LLM} \sin(\omega t) d(\omega t) = \frac{3V_{LLM}}{\pi} = 0.955V_{LLM}. \quad (7.45)$$

Therefore, the average value of the output voltage is approximately equal to the amplitude of the line voltage, V_{LLM} . The amplitudes of the harmonics are

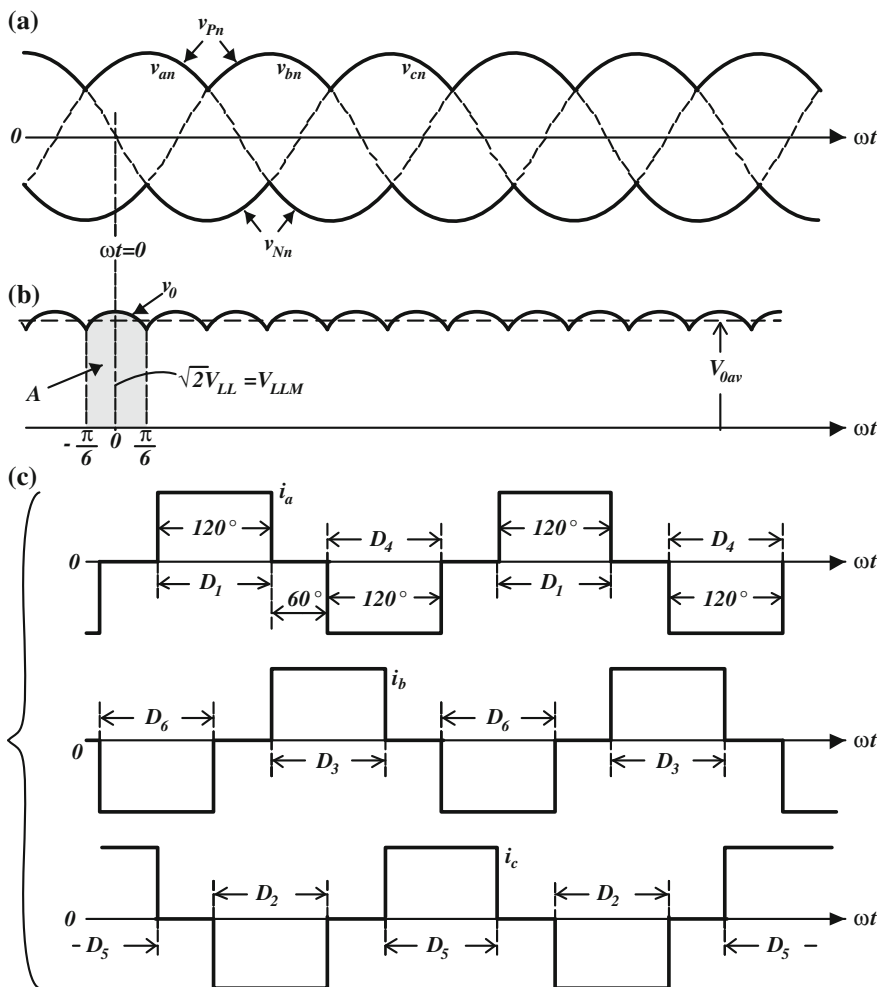


Fig. 7.15 Waveforms of voltages and currents of a three-phase rectifier operating in the constant load current mode

$$V_n = \frac{6V_{LLM}}{\pi(n^2 - 1)}, \quad n = 6, 12, 18, \dots \quad (7.46)$$

The harmonics of the output voltage are at frequencies $6k\omega$, $k = 1, 2, 3, \dots$, because the cycle of the output voltage is $1/6$ of the cycle of the input voltage. This is also an advantage of a three-phase rectifier compared to a single-phase rectifier. The AC components are at higher frequencies and are of smaller amplitudes, so they can be filtered out more readily. Owing to their bipolar shape the currents have odd

harmonics 5, 7, 11, 13, 17, 23, ..., because those involving integer factor 3 are zero. The amplitude of the first harmonic is

$$I_{s1} = \frac{2}{\pi} \sqrt{3} I_0, \quad (7.47)$$

whereas the amplitudes of the higher harmonics are

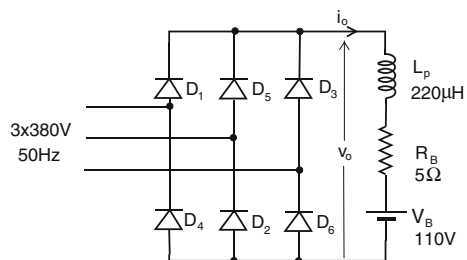
$$I_n = I_{s1}/n, \quad n = 5, 7, 11, 13, \dots \quad (7.48)$$

As already stressed at the beginning, the preceding analysis dealt with a simplified circuit of the rectifier (Fig. 7.14b). The analysis of a real rectifier circuit should be taken into account the series inductance of the line drive and the influence of the filter capacitor. Owing to the series inductance, like in a single-phase rectifier, the current commutation is not instantaneous. This leads to a certain reduction of the output voltage. The filter capacitor at the output supports the output voltage so that the rectifier operates closer to the constant output voltage mode than to the constant current mode. Because of that, the diodes will not conduct 120° each but only while the line voltage is higher than the voltage across the capacitor. The effect is similar to that in single-phase rectifiers.

Example 7.2 For the battery charger with a three-phase rectifier (Fig. 7.16)

- (a) Draw waveforms of the line to line input voltages, the load voltage and the frequency characteristics of the load current using PSPICE software package.
 - (b) Using PSPICE software package and Fourier analysis of the circuits from Fig. 7.16 determine the average value and sixth harmonic of the current through the load.
- (a) The waveforms of the line to line input voltages, the load voltage and the frequency characteristics of the load current are presented in Figs. 7.17 and 7.18 respectively.

Fig. 7.16 Three-phase battery charger



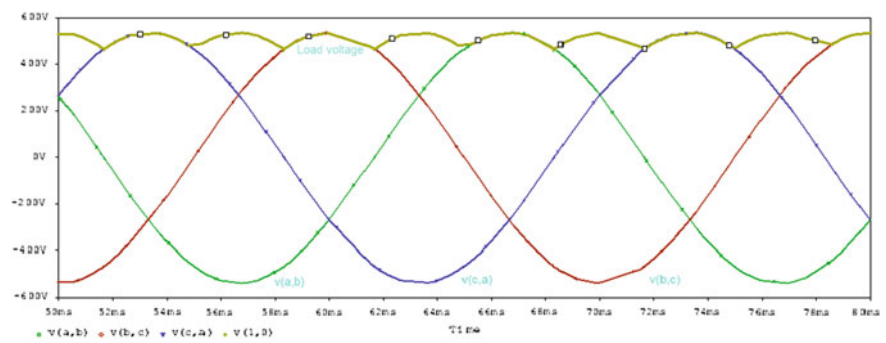


Fig. 7.17 Waveforms of line to line input voltages and load voltage for the rectifier from Fig. 7.16

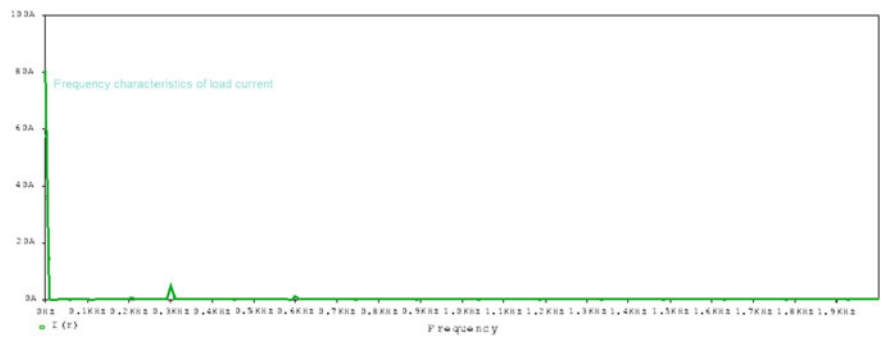


Fig. 7.18 Frequency characteristics of load current for the rectifier from Fig. 7.16

(b) Fourier components of load current $I(r)$.

DC Component = 8.026711E+01

Harmonic No (Hz)	Frequency component	Fourier component	Normalized (deg)	Phase phase (deg)	Normalized
1	5.000E+01	3.962E-01	1.000E+00	9.910E+01	0.000E+00
2	1.000E+02	7.468E-01	1.885E+00	-6.934E+01	-2.675E+02
3	1.500E+02	1.925E-01	4.860E-01	6.163E+01	-2.357E+02
4	2.000E+02	7.949E-01	2.006E+00	1.032E+02	-2.932E+02
5	2.500E+02	1.850E-01	4.669E-01	1.232E+01	-4.832E+02
6	3.000E+02	4.913E+00	1.240E+01	8.827E+01	-5.063E+02
7	3.500E+02	3.585E-01	9.049E-01	1.293E+01	-6.808E+02
8	4.000E+02	3.179E-01	8.025E-01	1.406E+02	-6.522E+02
9	4.500E+02	1.411E-01	3.561E-01	5.046E+01	-8.414E+02
10	5.000E+02	2.639E-01	6.662E-01	5.142E+01	-1.042E+03
11	5.500E+02	6.559E-02	1.656E-01	-5.347E+01	-1.144E+03
12	6.000E+02	8.898E-01	2.246E+00	-1.151E+02	-1.304E+03
13	6.500E+02	1.317E-01	3.324E-01	-7.653E+01	-1.365E+03
14	7.000E+02	3.288E-01	8.299E-01	-1.054E+02	-1.493E+03

On the basis of Fourier analysis it is obtained that the average value and sixth harmonic are $I_0 = 80.26$ A and $I_6 = 12.4$ A.

7.6 Phase Controlled Rectifiers

In phase controlled rectifiers thyristors are used instead of diodes. The average value of the output voltage is controlled by controlling the start of thyristor conduction. This will be considered in the example of a half-wave thyristor rectifier (Fig. 7.19).

The waveforms of this circuit, assuming that the thyristor was ideal, are shown in Fig. 7.19b. The thyristor starts conducting when a short pulse is fed to its gate. The input voltage is then transferred to the load. The thyristor turns off when the input voltage becomes negative. Therefore, the output voltage during one cycle is

$$v_o = \begin{cases} V_{SM} \sin(\omega t), & 0 \leq \omega t \leq \pi \\ 0, & \pi \leq \omega t \leq 2\pi + \alpha \end{cases} \quad (7.49)$$

Since the load is resistive, the current i_o follows the variation of v_o .

If the load is inductive-resistive (Fig. 7.20a), the thyristor will not turn off at the zero voltage crossing, but will continue conducting until the current i_o becomes zero (Fig. 7.20a). Owing to that the output contains a negative component. The delayed turning off of the thyristor is the consequence of the phase shift of the current i_o introduced by the inductance L . The angle is calculated from the condition $i_o(\beta) = 0$ (Fig. 7.20).

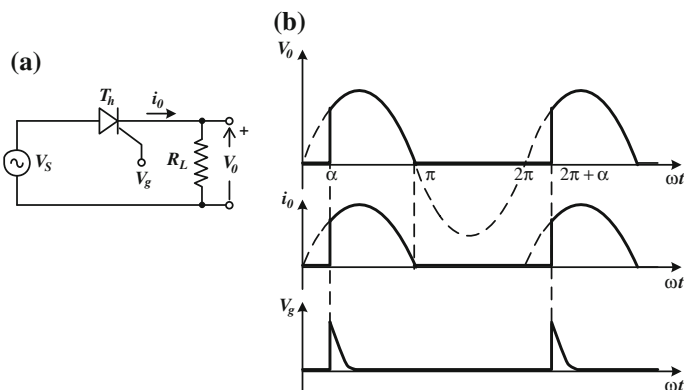


Fig. 7.19 A half-wave thyristor rectifier (a) and the voltage and current waveforms (b)

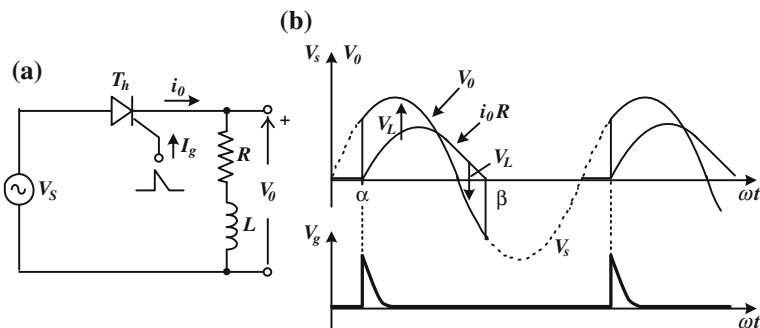


Fig. 7.20 A half-wave thyristor rectifier loaded by inductance and capacitance (a) and the corresponding voltage waveforms (b)

By varying the angle α the average value of the output voltage can be controlled from zero to the maximum value which is obtained for $\alpha = 0$. In order to accomplish that, there must be a generator of synchronization pulses for triggering of the thyristor in such a way that the angle α can be varied from 0 to 180° ($0 \leq \alpha \leq \pi$). A block diagram of such generator is shown in Fig. 7.21a. It consists of a source of the mains synchronization voltage $v_{\sin}$, a generator of a saw tooth voltage v_{ts} , a comparator, and a differentiator. The voltage $v_{\sin}$ synchronizes the saw tooth voltage with the zero crossing of the sin function. When the saw tooth voltage is equal to the control voltage, i.e., when $v_{ts} = v_{\sin}$, the output of the comparator becomes positive. At the output of the buffer B a short pulse is generated. Its duration depends on the time constant RC . Since the buffer B is synchronized with $v_{\sin}$, the pulse v_g will appear only during the positive half-cycle.

Since $v_{ts} = V_{tsM}(\omega t/\pi)$, from the condition $v_{ts}(\alpha/\omega) = V_{con.}$, it follows that

$$\alpha = \pi(V_{con.}/V_{tsM}) = 180^\circ(V_{con.}/V_{tsM}), \quad (7.50)$$

where V_{tsM} is the amplitude of the saw tooth voltage. Therefore, by varying the control voltage within the limits $0 \leq V_{con.} \leq V_{tsM}$ the angle α can be controlled within the limits $0 \leq \alpha \leq \pi$.

There are several types of integrated circuits, such as TCA780, developed for the triggering of thyristors and control of the angle α according to (7.50).

7.6.1 Full-Wave Thyristor Rectifiers

Two types of the full-wave thyristor rectifiers are used. A full-wave thyristor rectifier with a purely resistive load and a center-tapped secondary is shown in Fig. 7.22. The triggering pulses V_{g1} and V_{g2} are phase shifted by π so that the thyristor Th_1 is triggered at angles $2k\pi + \alpha$, and the thyristor Th_2 at $(2k+1)\pi + \alpha$, $k = 1, 2, 3, \dots$ Such a generator can be made if the circuit in Fig. 7.21a is added to

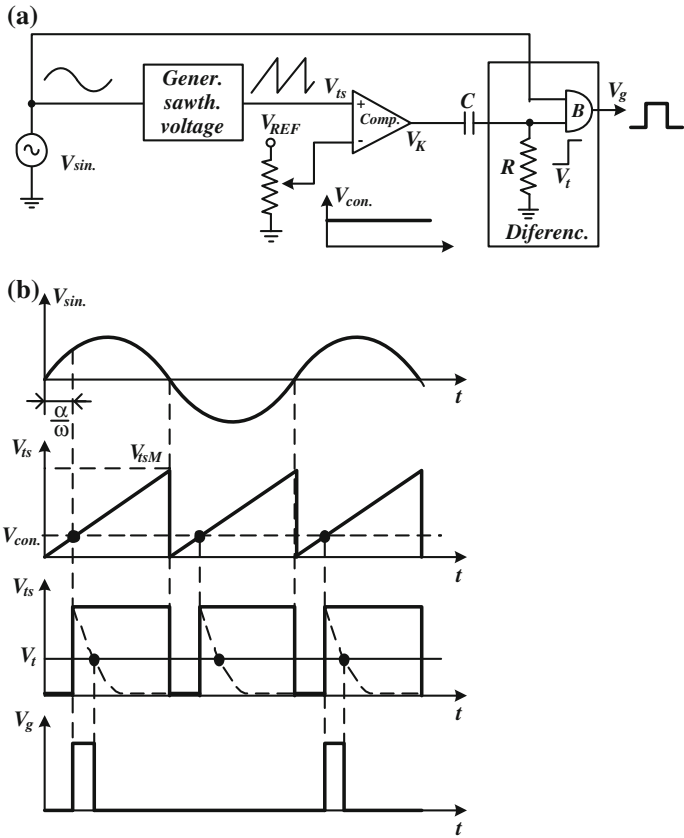


Fig. 7.21 A generator of triggering pulses for driving the thyristor (a) and the corresponding voltage waveforms (b)

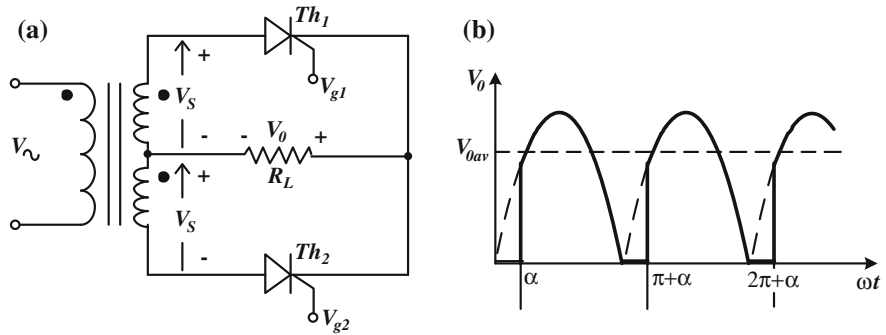


Fig. 7.22 A full-wave single-phase thyristor rectifier with a center-tapped secondary (a) and the waveform of the output voltage (b)

another differentiator synchronized with the negative half-cycle of $V_{\sin}$. At its output, one will obtain pulses V_{g2} for triggering Th_2 .

Before any thyristor is turned on the output voltage is zero, and when one of the thyristors is on, then $v_o = |v_s|$ (Fig. 7.22b). The average value of the output voltage is determined by

$$V_{\text{Oav}} = \frac{1}{\pi} \int_{\alpha}^{\pi} V_{\text{SM}} \sin(\omega t) d(\omega t) = \frac{V_{\text{SM}}}{\pi} (1 + \cos \alpha). \quad (7.51)$$

Since α can be controlled within the limits $0 \leq \alpha \leq \pi$ and in these limits $-1 \leq \cos \alpha \leq 1$, it follows that

$$0 \leq V_{\text{Oav}} \leq V_{\text{SM}}/\pi. \quad (7.52)$$

The average value of the load current is $I_{\text{Oav}} = V_{\text{Oav}}/R_L$, and its root mean square value is

$$I_{\text{orms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\pi} \left[\frac{V_{\text{SM}}}{\pi} \sin(\omega t) \right]^2 d(\omega t)} = \frac{V_{\text{SM}}}{R} \sqrt{\frac{1}{2} - \frac{\alpha}{2\pi} + \frac{\sin(2\alpha)}{4\pi}}. \quad (7.53)$$

The allowed load of the thyristor bridge rectifier is the R - L type (Fig. 7.23b). With this load, two operating modes are possible:

- discontinuous and
- continuous.

In the first mode, the load current does not flow during the whole of the cycle (Fig. 7.23b), and in the second it is continuous (Fig. 7.23c). Owing to the reactive component of the load the conducting pair of thyristors remains on after the polarity of the input voltage has changed. They conduct until the current through them drops to zero. If this happens before the second thyristor pair is triggered, the operating mode is discontinuous. If the conducting pair of thyristors is still conducting at the moment of triggering of the second pair, the current through the load will be continuous (Fig. 7.23c).

In the first case, the load current is non-zero during $\alpha \leq \omega t \leq \beta$ and it amounts to

$$i_0(\omega t) = \frac{V_{\text{SM}}}{Z_L} [\sin(\omega t - \Theta) - e^{-(\omega t - \alpha)/(\omega \tau)} \sin(\alpha - \Theta)], \quad \alpha \leq \omega t \leq \beta \quad (7.54)$$

where

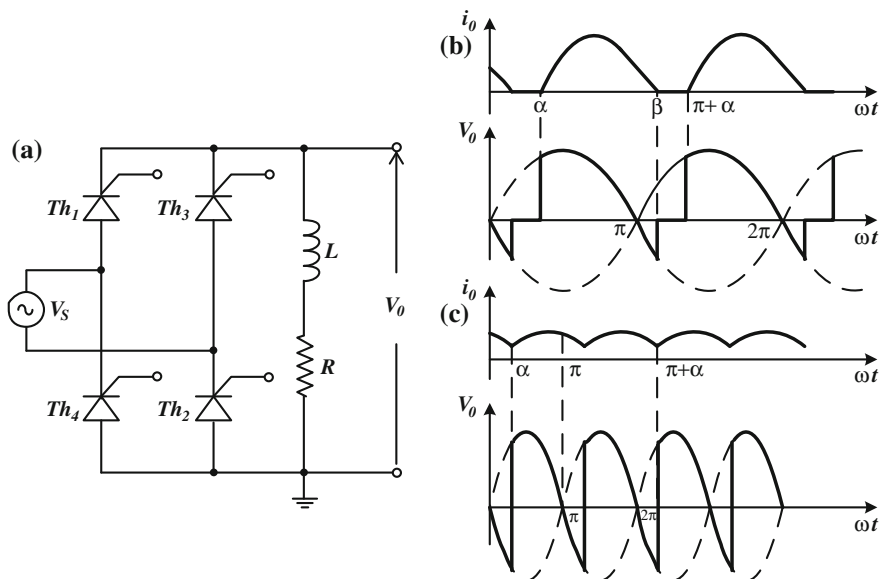


Fig. 7.23 A thyristor single-phase bridge rectifier with an R - L load (a) and the output current and voltage in the discontinuous (b) and continuous mode (c)

$$Z_L = \sqrt{R^2 + (\omega R)^2}, \quad \Theta = \tan^{-1}(\omega\tau) \text{ and } \tau = L/R.$$

During the positive half-cycle of the input voltage while $\alpha \leq \omega t \leq \beta$ the thyristors Th_1 and Th_2 are conducting whereas the other pair Th_3 and Th_4 are off. The pair Th_1 and Th_2 is turned off at the instant β/ω . The thyristors Th_3 and Th_4 are turned on at the instant $(\pi + \alpha)/\omega$, so that during the time interval $\beta/\omega \leq t \leq (\pi + \alpha)/\omega$ all thyristors are off and the load current is zero. Thus, the discontinuous mode will exist if

$$\beta < \pi + \alpha. \quad (7.55)$$

The boundary between the continuous and the discontinuous modes is defined by $\beta = \pi + \alpha$, i.e. by

$$i_o(\pi + \alpha) > 0. \quad (7.56)$$

On the basis of (7.54) and (7.56), it follows that

$$\sin(\pi + \alpha - \Theta) - e^{-(\pi + \alpha - \alpha)/(\omega\tau)} \sin(\alpha - \Theta) \geq 0. \quad (7.57)$$

Since $\sin(\pi + \alpha - \theta) = \sin(\theta - \alpha)$, (7.57) reduces to

$$\left(1 - e^{-\pi/(\omega\tau)}\right) \sin(\vartheta - \alpha) \geq 1, \quad (7.58)$$

where from it follows that

$$\alpha \leq \theta = \tan^{-1}(\omega L/R). \quad (7.59)$$

Therefore, the continuous mode will be sustained if condition (7.59) is satisfied. The DC component (average value) of the output voltage for the continuous mode is determined by

$$V_{\text{oav}} = \frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} V_{\text{SM}} \sin(\omega t) d(\omega t) = \frac{2V_{\text{SM}}}{\pi} \cos \alpha. \quad (7.60)$$

Example 7.3 For the rectifier in Fig. 7.24 determine the average value of the voltage across the load, the average load current, and the average values of the thyristor and the diode currents if the load is:

- (a) resistance R ,
- (b) a series connection of the resistance R and the inductance L .

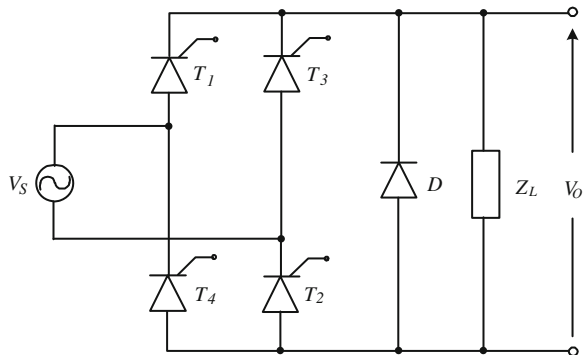
It is known that $V_{\text{SM}} = 311 \text{ V}$, $f = 50 \text{ Hz}$, $R = 10 \Omega$, $\omega L > R$, and $\alpha = \pi/3$.

- (a) The load is the resistor R .

The average value of the voltage across the load is

$$V_o = \frac{1}{\pi} \int_{\alpha}^{\pi} V_{\text{SM}} \sin(\omega t) d(\omega t) = \frac{V_{\text{SM}}}{\pi} (1 + \cos \alpha) = \frac{311}{\pi} (1 + 0.5) = 148.5 \text{ V}.$$

Fig. 7.24 Full-wave thyristor rectifier



The average value of the load current is

$$I_0 = V_0/R = 14.85\text{V}.$$

For a purely resistive load, there is no current through the diode, so $I_{d0} = 0$.

The average value of the thyristor current is one half the load current.

(b) The load is a series R - L circuit.

The average values of the load voltage and the load current are the same as in the case (a). Since the load is inductive, the current through the load is continuous and the diode D conducts when all thyristors in the bridge are off.

The average value of the current through the diode is $I_{d0} = \alpha/\pi \cdot I_0 = 4.95\text{ A}$, and the average value of the current through the thyristor is also $I_{T0} = (\pi - \alpha)/\pi \cdot I_0 = 4.95\text{ A}$.

Example 7.4 Determine the average value of the load current for the rectifier from Fig. 7.25 and draw the waveforms of the load current and the load voltage using PSPICE software package.

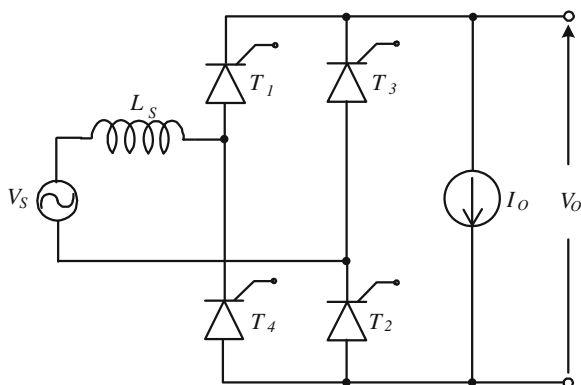
It is known that $v_s(\omega t) = 311 \sin(\omega t)\text{V}$, $f = 50\text{ Hz}$, $R = 10\ \Omega$, $L_s = 10\text{ mH}$, $\omega L > R$, and $\alpha = \pi/3$.

Let us consider the instant of turning on of the thyristors Th_1 and Th_2 , if the thyristors Th_3 and Th_4 were conducting before them. Due to the inductivity of the source, the source current will lag behind the source voltage, so the thyristors Th_3 and Th_4 are turned on for some time while the thyristors Th_1 and Th_2 take over the load current. If the angle of commutation is denoted by γ , the average value of the load current is

$$I_0 = \frac{1}{\pi R} \int_{\alpha+\gamma}^{\pi+\alpha} V_{SM} \sin(\omega t) d(\omega t) = \frac{V_{SM}}{\pi R} [\cos(\alpha + \gamma) + \cos \alpha].$$

During the commutation process, all four thyristors are conducting so the voltage across the inductance L_s is equal to the source voltage v_s , i.e.,

Fig. 7.25 Full-wave rectifier with the effect of source inductance



$$v_{Ls} = v_s \text{ for } \alpha \leq \omega t \leq \alpha + \gamma.$$

The current through the inductance L_s can be determined following the Eq. (7.11)

$$i_{Ls}(\omega t) = \frac{1}{\omega L_s} \int_{\alpha}^{\omega t} V_{SM} \sin(\omega t) d(\omega t) - I_o. \quad (7.61)$$

The commutation will be finished when the current through the inductance L_s becomes equal to the load current, i.e.

$$i_{Ls}(\alpha + \gamma) = I_o = \frac{V_{SM}}{\omega L_s} [\cos \alpha - \cos(\alpha + \gamma)] - I_o. \quad (7.62)$$

From (7.62) the angle of commutation is

$$\cos \alpha - \cos(\alpha + \gamma) = \frac{2\omega L_s I_o}{V_{SM}} \Rightarrow \cos(\alpha + \gamma) = \cos \alpha - \frac{2\omega L_s I_o}{V_{SM}}. \quad (7.63)$$

From (7.62) and (7.63), the average load current is (Figs. 7.26, 7.27)

$$I_o = \frac{2V_{SM}}{\pi R} \left[\cos \alpha - \frac{\omega L_s I_o}{V_{SM}} \right] = \frac{2V_{SM}}{\pi R} \cos \alpha - \frac{2\omega L_s I_o}{\pi R},$$

and

$$I_o = \frac{2V_{SM} \cos \alpha}{\pi R + 2\omega L_s} = \frac{2 \times 311 \times 0.5}{10\pi + 4\pi \times 50 \times 0.01} = 8.25 \text{ A}.$$

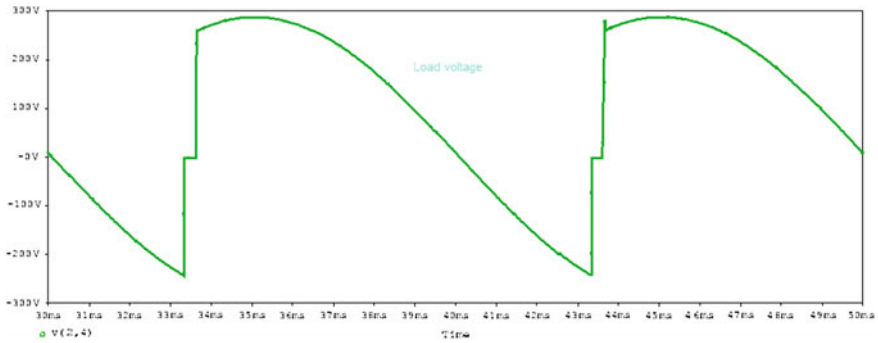


Fig. 7.26 Waveform of the load voltage for the rectifier shown in Fig. 7.25

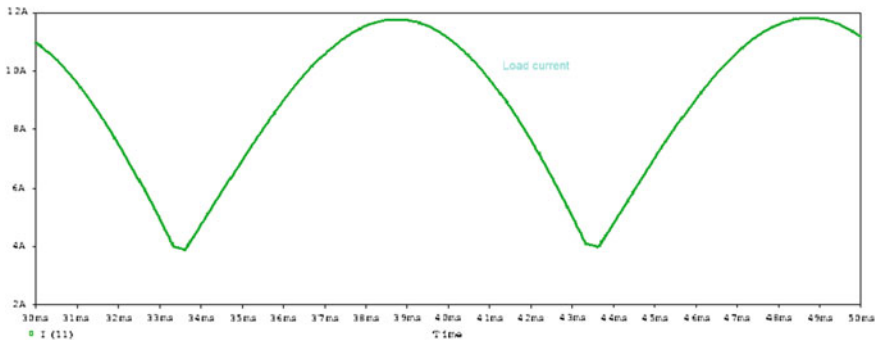


Fig. 7.27 Waveform of the load current for the rectifier shown in Fig. 7.25

7.6.2 Three-Phase Thyristor Bridge Rectifiers

The topology of the thyristor bridge rectifier (Fig. 7.28a) is the same as that of the corresponding diode rectifier. The difference in the principle of operation is that the diodes are conducting when forward biased and the thyristors conduct if a triggering pulse is present in the gate circuit together with the forward bias. This is the way of controlling the angle of conduction and consequently the average value of the output voltage. If the angle of triggering is α , the output voltage waveform is as shown in Fig. 7.28b and its average value is determined by

$$V_o = \frac{1}{\pi/3} \int_{\pi/3+\alpha}^{2\pi/3+\alpha} V_{LLM} \sin(\omega t) d(\omega t) = \frac{3V_{LLM}}{\pi} \cos \alpha. \quad (7.64)$$

Compared to V_o of the three-phase diode rectifier (7.45) the factor $\cos \alpha$ is present here. If the angle of triggering is greater than $\pi/3$ ($\alpha > \pi/3$), the rectifier operates in the discontinuous mode of the load current. Then the average value of the output voltage is determined by

$$V_o = \frac{1}{\pi/3} \int_{\pi/3+\alpha}^{\pi} V_{LLM} \sin(\omega t) d(\omega t) = \frac{3V_{LLM}}{\pi} [1 + \cos(\pi/3 + \alpha)]. \quad (7.65)$$

Example 7.5 For the battery charger realized with a three-phase thyristor bridge rectifier (Fig. 7.29)

- Determine the change in the angle of triggering the thyristors so the load current is held constant during charging of the battery s (for the minimum battery voltage, the angle of thyristor triggering is $\alpha = 45^\circ$).
- Draw the waveform of the load voltage if the angle of thyristor triggering is $\alpha = 45^\circ$ using PSPICE software package.

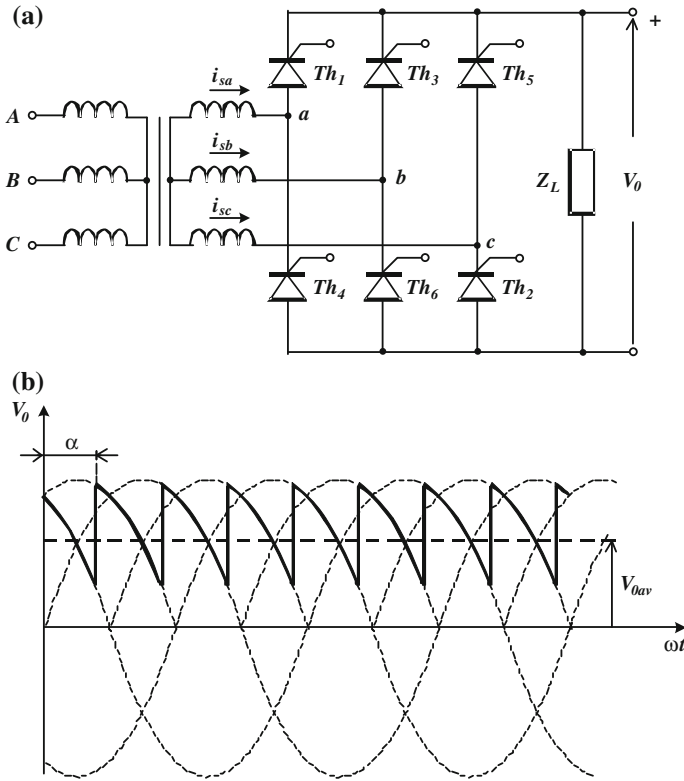
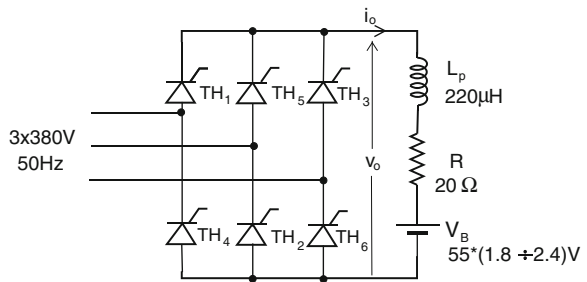


Fig. 7.28 A three-phase thyristor bridge rectifier (a) and the output voltage waveforms for a resistive load (b)

Fig. 7.29 Battery charger with three-phase thyristor bridge rectifier



(a) The average value of the battery charging current is

$$I_o = \frac{V_o - V_{\text{bat}}}{R}.$$

If the voltage of the battery cell at the beginning of charging is 1.8 V, and the angle of thyristor triggering is $\alpha = 45^\circ$, then the average charging current is equal to

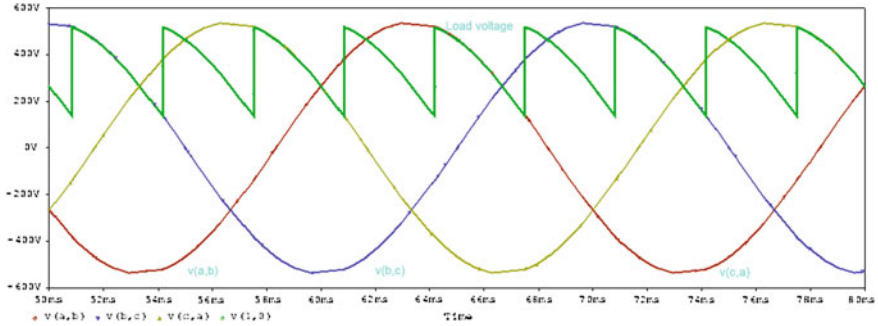


Fig. 7.30 Line to line input voltages and load voltage for the rectifier from Fig. 7.29

$$I_o = \frac{(3V_{LLM}/\pi) \times \cos(\pi/4) - (1.8 \times 55)}{20} = 13.23 \text{ A.}$$

When the batteries are full, the cell voltage is 2.4 V. To ensure the same charging current, the thyristor triggering angle is equal to

$$a = \arccos\left(\frac{R \times I_o + (55 \times 2.4)}{3V_{LLM}/\pi}\right) = 0.623 \text{ rad} \approx 36^\circ.$$

The change in the angle of triggering the thyristors during the battery charging is $\Delta\alpha = 45^\circ - 36^\circ = 9^\circ$ (Fig. 7.30).

(b) See Fig. 7.30.

7.7 Twelve-Pulse Rectifiers

In the cases when the primary power source is three-phase and a higher DC output voltage is required multipulse rectifiers are used. The twelve-pulse rectifiers have found practical applications. Such a rectifier consists of 2 six-pulse three-phase rectifier rectifiers connected in series. One six-pulse rectifier is supplied through a Y-Y transformer, and the other through a Y- δ transformer (Fig. 7.31). So, the two rectifier output voltages have a phase shift of $\pi/6$.

The highest average value of the output voltage is obtained if $\alpha = 0$, i.e., if the rectifiers behave as a diode rectifier

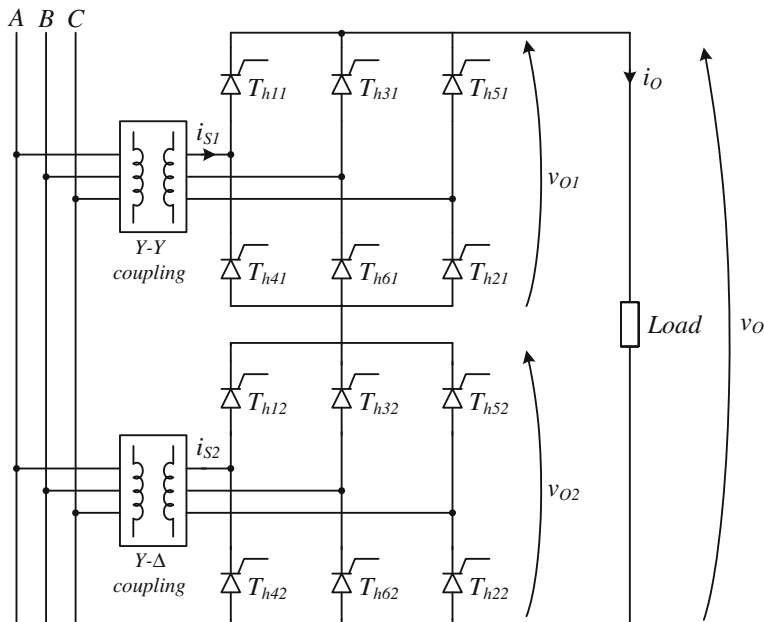


Fig. 7.31 Twelve-pulses thyristor rectifier

$$\begin{aligned}
 V_{o\max} &= V_{LLM} \sin\left(\frac{\pi}{6} + \frac{\pi}{3}\right) + V_{LLM} \sin\left(\frac{\pi}{6} + \frac{\pi}{4}\right) \\
 &= V_{LLM} \sin\left(\frac{7\pi}{12}\right) + V_{LLM} \sin\left(\frac{5\pi}{12}\right) = 2V_{LLM} \cos\left(\frac{\pi}{12}\right) = 1.932V_{LLM}.
 \end{aligned}
 \tag{7.66}$$

In the general case, the average value of the output voltage is (Fig. 7.31):

$$V_o = V_{o1} + V_{o2} = \frac{3V_{LLM}}{\pi} \cos \alpha + \frac{3V_{LLM}}{\pi} \cos \alpha = \frac{6V_{LLM}}{\pi} \cos \alpha.
 \tag{7.67}$$

Besides the average value (zero harmonic), the spectrum of the six-pulse three-phase rectifier output voltage contains harmonics with a frequency equal to the product of the frequency of the source and the number $n = 6k$, $k \in N$.

The output voltage of a twelve-pulse rectifier has harmonic frequencies, which are multiples of 12 times the frequency of source $12k\omega_1$, $k \in N$, where ω_1 is the frequency of source.

It is interesting to make a similar analysis of the input currents at six pulses and twelve-pulses rectifiers. Besides the harmonic at the frequency of source, the input current of a six-pulses rectifier contains harmonics (Fig. 7.32)

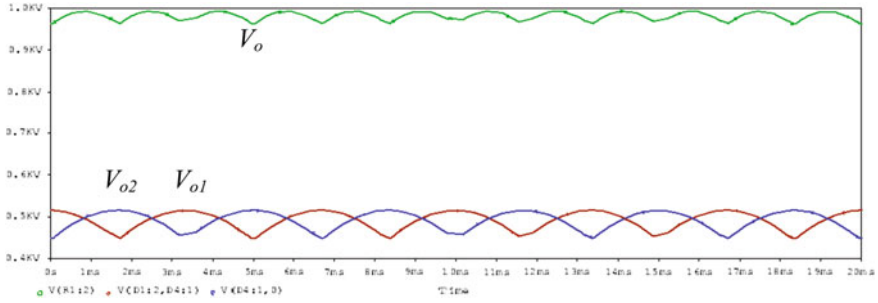


Fig. 7.32 Waveforms of three-phase rectifier output voltages and output voltage of twelve-pulse rectifier when input voltage is 3×380 V, 50 Hz

$$I_{sn} = \frac{I_{s1}}{n}, I_{s1} = 2\sqrt{3}I_0, n = 6k + 1 \quad (\text{Sect. 7.6})$$

The input current of the twelve-pulse rectifier from Fig. 7.31 is

$$i_s = i_{s1} + i_{s2} \quad (7.68)$$

where

$$\begin{aligned} i_{s1} &= \frac{2\sqrt{3}}{\pi} I_0 \left(\cos \omega_1 t - \frac{1}{5} \cos 5\omega_1 t + \frac{1}{7} \cos 7\omega_1 t - \frac{1}{11} \cos 11\omega_1 t + \frac{1}{13} \cos 13\omega_1 t - \dots \right) \\ i_{s2} &= \frac{2\sqrt{3}}{\pi} I_0 \left(\cos \omega_1 t + \frac{1}{5} \cos 5\omega_1 t - \frac{1}{7} \cos 7\omega_1 t - \frac{1}{11} \cos 11\omega_1 t + \frac{1}{13} \cos 13\omega_1 t + \dots \right). \end{aligned} \quad (7.69)$$

From (7.68) and (7.69) it is obtained that

$$i_s = \frac{4\sqrt{3}}{\pi} I_0 \left(\cos \omega_1 t - \frac{1}{11} \cos 11\omega_1 t + \frac{1}{13} \cos 13\omega_1 t - \dots \right) \quad (7.70)$$

Besides the harmonic at the frequency of source, the input current of the twelve-pulse rectifier contains harmonics $n = 12k \pm 1$, $k \in N$.

Based on the foregoing it can be concluded that the twelve-pulse rectifier compared to a six-pulse rectifier has:

- higher average value of the output voltage,
- less ripple of the output voltage,
- less influence of higher harmonics to the output voltage and the supply current.

A power system has the practical limitation of 12 pulses, because of the large expense of producing high-voltage transformers with an appropriate phase shift. In industrial applications, such rectifiers are realized up to 48 pulse.

7.8 Rectifiers with Circuit for Power Factor Correction

Rectifiers are often the input stage of many power electronic devices, such as indirect AC/AC frequency converters, uninterruptible power supply sources, converters in AC electrical drives, etc.

On the other side, the previously discussed rectifiers have an input current that significantly deviates from the sinusoidal shape and its spectrum is rich with harmonics that are close to the fundamental harmonic. Diode and thyristor rectifiers are nonlinear loads, and as such they are a source of harmonics in the input current. These harmonics cause problems in the distribution network as well as an increase of reactive power, higher losses in the transmission network, voltage distortion, higher EMI, etc.

In order to better understand the problems, a single-phase diode rectifier is observed. Seen from the input, the characteristics of the rectifier should be such that the input current has a sinusoidal shape and in a phase with the input voltage. In other words, the rectifier should behave as a pure resistance load (Fig. 7.33). The resistance R_e in Fig. 7.33 is not a real resistance, but shows how the power of an AC source should be delivered to a DC load. This resistance is known as the Loss Free Resistor (LFR) [1].

Since the control of the rectifier output variable is required, the resistance R_e is controlled by the signal v_c . The waveform of voltage at the output of the Graetz bridge and its desired shape are shown in Fig. 7.34a, b, respectively.

The output voltage of the Graetz bridge and its desired shape are purely DC, so the DC/DC converter with the output-to-input voltage ratio as shown in Fig. 7.35 should be put between the rectifier and the load. Therefore, it is necessary that the DC/DC converter be regulated by a controller. The input variables of the controller are i_G and v_G (voltage and current of the Graetz bridge) and its output variable in the simplest realization is the duty ratio of the switching transistor $D(t)$. The voltage transfer ratio of the DC/DC converter (Fig. 7.35) is $1:M(D(t))$, where

$$M(D(t)) = \frac{V}{V_{SM}|\sin(\omega t)|}. \quad (7.71)$$

In this way, the rectifier topology shown in Fig. 7.36 is obtained. Based on the obtained relationship between the output and the input voltage of the DC/DC converter it is concluded that its transmission ratio changes from V/V_{SM} to infinity.

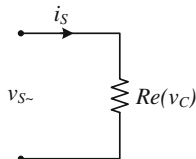


Fig. 7.33 Loss free resistor

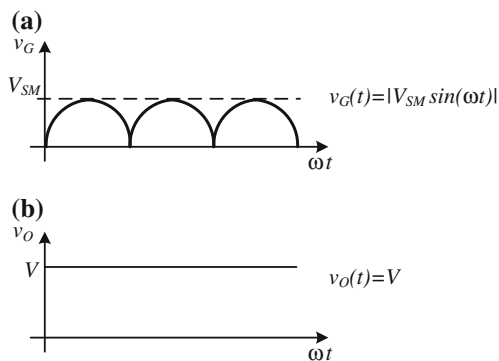


Fig. 7.34 Waveform of voltage at output of Graetz bridge rectifier (a) and its desired shape (b)

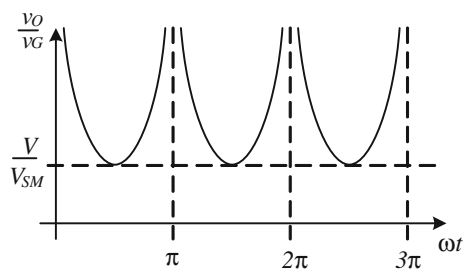


Fig. 7.35 Waveform of DC/DC converter output voltage in rectifier with circuit for power factor correction

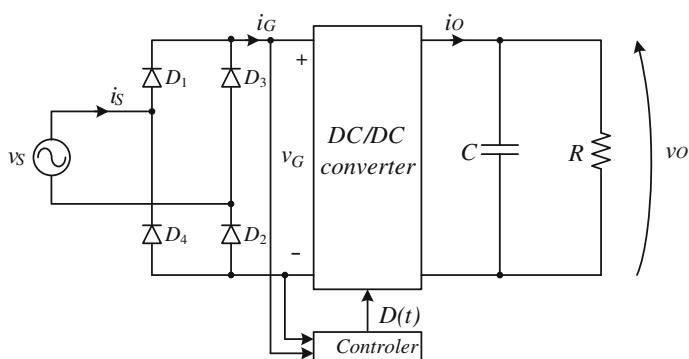


Fig. 7.36 DC/DC converter for power factor correction connected to the output of Graetz bridge rectifier

One of the converters that can provide such a transmission ratio is the boost converter, on condition that $V/V_{SM} \geq 1$.

If power losses in the rectifier are neglected, the output power is equal to the input power,

$$p_s(t) = v_s(t)i_s(t) = v_G(t)i_G(t) = v_o(t)i_o(t) \quad (7.72)$$

$$i_o(t) = \frac{V_{SM}^2 \sin^2(\omega t)}{VR_e} = \frac{V_{SM}^2 (1 - \cos 2\omega t)}{2VR_e}. \quad (7.73)$$

By filtering the current i_o , which is a function of the capacitance C connected in parallel with the load, the average value of the current through the load R is

$$I_o = \frac{V_{SM}^2}{2VR_e} \quad (7.74)$$

The topology of the rectifier with a circuit for power factor correction based on the use of a boost DC/DC converter is shown in Fig. 7.37 [1]. The boost converter, depending on the working conditions, can be in continuous or discontinuous current mode.

If the boost converter works in continuous mode and the inductance L has negligible influence to low order harmonics then the duty ratio can be written in the following form

$$M(D(t)) = \frac{1}{1 - D(t)}. \quad (7.75)$$

From (7.71) and (7.75) it is obtained that

$$D(t) = 1 - \frac{v_g}{V}. \quad (7.76)$$

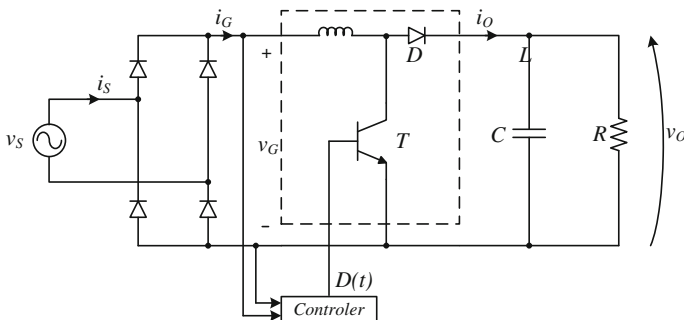


Fig. 7.37 Rectifier with boost converter for power factor correction [1]

The condition that the boost converter works in continuous mode is that the average value of the current through the inductance L is greater than a half of its changes, i.e.,

$$\begin{aligned} I_G &> \frac{\Delta i_G}{2}, \\ I_G &= \frac{V_G}{R_e}, \quad \frac{\Delta i_G}{2} = \frac{V_G}{2L} D(t) T, \end{aligned} \quad (7.77)$$

where V_G is the average value of the voltage v_g . From (7.76) and (7.76) the condition for the CCM work of converter is obtained

$$\frac{V_G}{R_e} > \frac{V_G}{2L} \left(1 - \frac{v_g}{V}\right) T \Rightarrow R_e < \frac{2L}{T(1 - \frac{v_g}{V})}. \quad (7.78)$$

The right side of expression (7.78) has the maximum value if $v_G = V_{SM}$, so DCM will be reached if

$$R_e > \frac{2L}{T(1 - \frac{v_{SM}}{V})}. \quad (7.79)$$

If R_e has a value between the values given in Eqs. (7.78) and (7.79) the boost converter will operate in DCM if v_G is small, or if v_G is approaching V_{SM} the converter will work in CCM. It should be noted that for the discontinuous mode the effective resistance of the boost converter $R_{eff} = \frac{2L}{TD^2(t)}$ does not necessary coincide with the emulated resistance R_e , and in this case is necessary to modify the inequalities which define the boundary between the continuous and the discontinuous modes.

Also, some other topologies of DC/DC converters giving the appropriate ratio 1: $M(D(t))$, such as buck-boost, Ćuk, SEPIC, or their variations with pulse transformer in some designs, can be used for the realization of the rectifier with circuit for power factor correction.

7.9 Active Rectifier

Inactive rectifier techniques, diodes and thyristors are replaced with actively controlled switches such as transistors, usually MOSFET or IGBT, or with fully controlled thyristor units such as GTO or IGCT.

Active rectifiers are often used for power factor correction, so the input current follows the input voltage, thereby eliminating the input reactive currents, and eventually increasing the efficiency of the system.

They can be realized as single-phase or poly-phase (usually three-phase), voltage or current rectifiers. A variety of linear and nonlinear techniques were developed for their control.

The active rectifier with a hysteresis controller and the PWM rectifiers has found significant application.

7.9.1 Active Rectifier with Hysteresis Current Controller

The active rectifier with a hysteresis current controller is a converter whose realization is simple from the standpoint of regulation, and which gives a good performance in terms of power factor correction and input current shape. An active single-phase boost rectifier with a current controller is shown in Fig. 7.38 [2].

The switches S_1 , S_2 , S_3 and S_4 are usually MOS transistors, or IGBTs, but it is also possible to use fully controlled thyristors. This rectifier operates as follows. The reference input current i_s^* is obtained by scaling the input voltage v_s , so that it is in phase with the input voltage and has a sinusoidal shape. The current i_s^* is compared with the measured current i_s and the difference $\Delta i_s = i_s^* - i_s$ is fed to the hysteresis controller.

If $\Delta i_s > 0$, the current i_s is lower than the reference, and it should be increased. For an input voltage $v_s > 0$ the current i_s will increase if $v_s > v_{ab}$. This condition can be achieved if $v_{ab} = -v_o$, S_3 and S_4 are turned on (Figs. 7.39 and 7.40), or $v_{ab} = 0$, S_4 and D_2 are turned on (Fig. 7.41), and in the case when S_3 and D_1 (Fig. 7.41) are turned on.

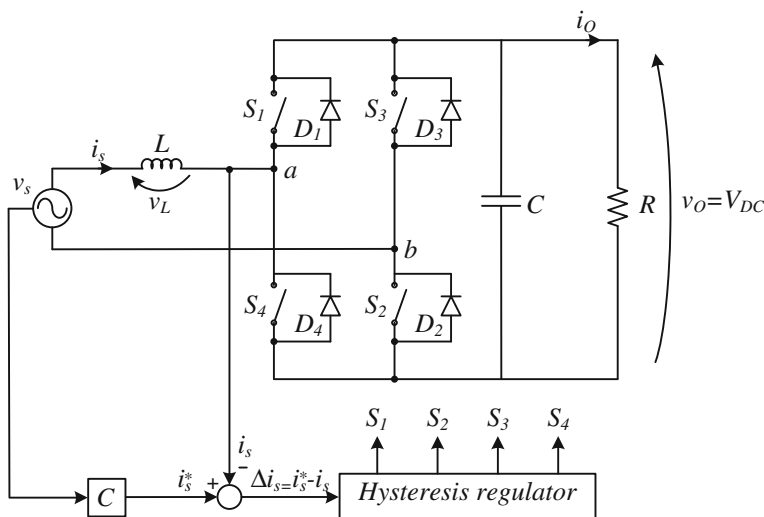


Fig. 7.38 Active single-phase boost rectifier with hysteresis controller

Fig. 7.39 Increasing the current i_s when $v_s > 0$ so that two switches S_3 and S_4 are turned on

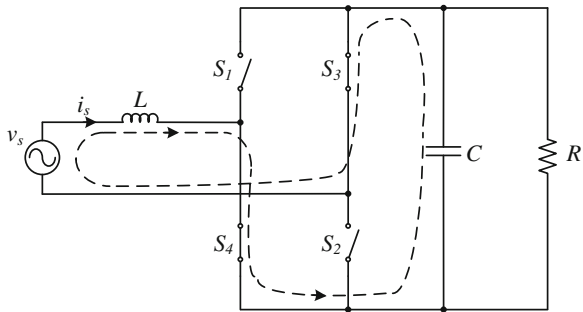


Fig. 7.40 Increasing the current i_s , when $v_s > 0$ so that one switch S_3 and diode D_1 are turned on

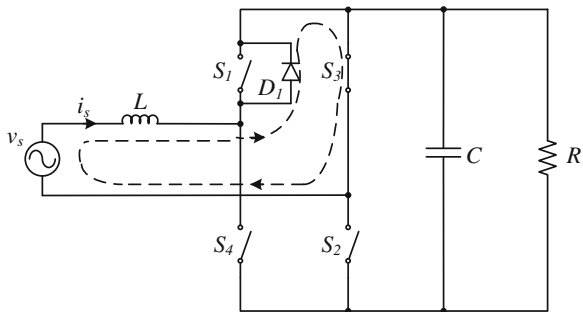
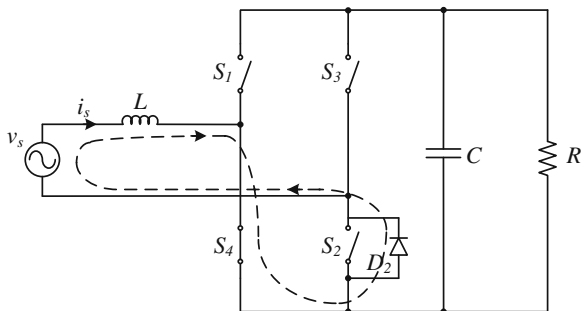


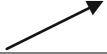
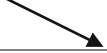
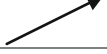
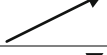
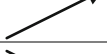
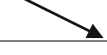
Fig. 7.41 Increasing the current i_s , when $v_s > 0$ so that one switch S_4 and diode D_2 are turned on



Analogously, during the negative half-cycle of the input voltage v_s the current i_s has the opposite direction, so the current i_s increases if $v_s < v_{ab}$. This condition is achieved if $v_{ab} = v_o$, the switches S_1 and S_2 are turned on, or $v_{ab} = 0$, the switch S_1 , and the diode D_3 are turned on, or the switch S_2 and the diode D_4 are turned on.

If $\Delta i_s < 0$, the current i_s is greater than the reference, so it should be reduced. For the positive half-cycle of the input voltage v_s it will be achieved if $v_s < v_{ab}$ i.e. $v_{ab} = v_o$. This corresponds to the case when all the transistor switches are turned off, and the current contour is closed through the diodes D_1 and D_2 . During the negative half-cycle of the input voltage v_s the current i_s will decrease if $v_s > v_{ab}$ i.e. $v_{ab} = -v_o$. This will be achieved if all the transistor switches are turned-off, and the current contour is closed through the diodes D_3 and D_4 .

Table 7.1 Control of switches in rectifier with hysteresis current controller

Polarity v_s	Turned-on switches	Voltage v_{ab}	Current flow i_s
+	S_3, S_4	$-V_{DC}$	
+	S_3, D_1	0	
+	S_4, D_2	0	
+	D_1, D_2	$+V_{DC}$	
-	S_1, S_2	$+V_{DC}$	
-	S_1, D_3	0	
-	S_2, D_4	0	
-	D_3, D_4	$-V_{DC}$	

The switching control sequences of the rectifier from Fig. 7.38 are shown in Table 7.1, and the waveforms of the input current and its reference are shown in Fig. 7.42.

Based on the state of the switches that define the flow of electrical current, it can be concluded that the increase of current can be achieved for both polarities of the input voltage if either the two transistors are turned on, or one transistor and a diode. If two transistors are turned on, the voltage applied to the inductance is larger, so the increase of current is higher.

The state when the two diodes D_1 and D_2 are turned on while $v_s > 0$, or the diodes D_3 and D_4 are turned on while $v_s < 0$, corresponds to the work of the diode rectifier and in these intervals the output capacitance C_o is charged.

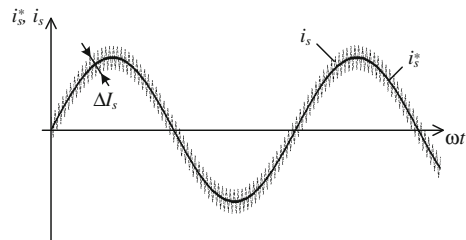
The advantages of such a rectifier realization are reflected in the following:

- (1) power factor close to 1 and
- (2) less current harmonics.

Disadvantages are:

- (1) higher switching losses and
- (2) variable switching frequency.

Fig. 7.42 Waveforms of input current and its reference



The selected strategy has a significant effect on the rectifier features (one or two transistor switches are turned on when the current i_s increases), the inductance L and the extent of the current hysteresis.

7.10 PWM Rectifiers

PWM rectifiers have many advantages compared to the conventional diode or thyristor rectifiers, so in recent years they have found significant application. Transistors, thyristors, or completely controlled thyristors are used as switching components. Today, two basic rectifier topologies are widely accepted, boost rectifier with voltage output (Fig. 7.43) and buck rectifier with current output (Fig. 7.44) [3].

Besides the power factor correction and a near-sinusoidal input current shape compared to the conventional diode and thyristor rectifiers, the PWM rectifiers have the following advantages:

- stabilization and regulation of DC link voltage (current)
- lower harmonic distortion of line current,
- bidirection power flow from the primary source to load and back from load to the source.

The last characteristic is very important for application of the rectifiers in electric drives. Besides the advantages, the PWM rectifiers have certain disadvantages compared to the diode (thyristor) rectifiers. These disadvantages are primarily related to complex regulation and higher switching losses. Also, due to electromagnetic interference, it is necessary to use a low pass filter between the power lines and the PWM rectifiers. The voltage boost three-phase PWM rectifier has

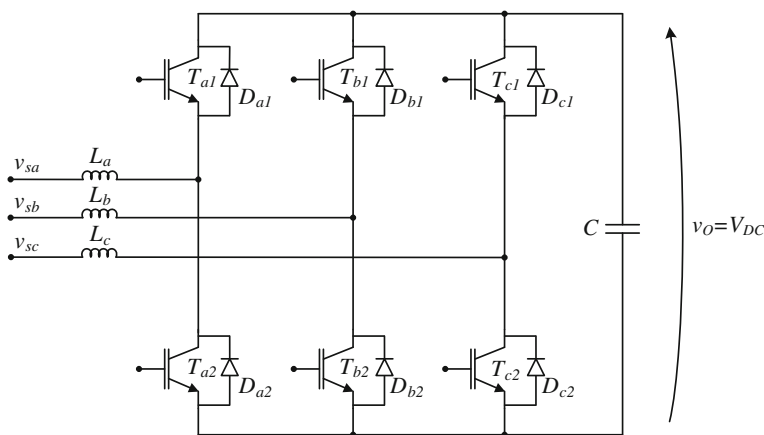


Fig. 7.43 Three-phase PWM boost rectifier

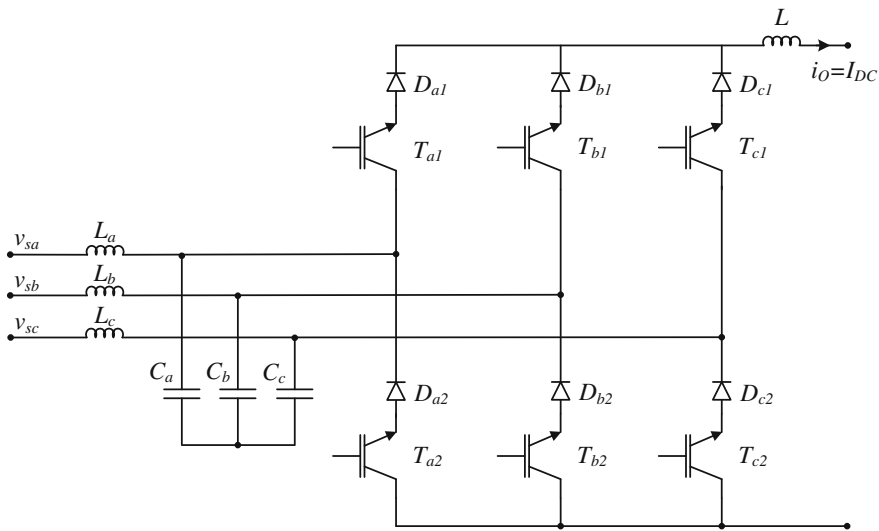


Fig. 7.44 Three-phase PWMbuck rectifier

found the widest application among the PWM rectifier topologies. The main function of a rectifier is to maintain the output voltage V_{DC} on a pre-defined DC value. To achieve this, it is necessary to implement the feedback contour by the output voltage (Fig. 7.45). The output voltage V_{DC} is compared with the referent voltage V_{DC}^* . The error information is introduced in the controller. This controller controls the switches, defines on and off states of switches, in the by way of the current i_o or the voltage v_o , to maintain the output voltage on the reference value (V_{DC}^*). The current i_o can have both directions, one that corresponds to the rectifier workingmode, current flows from the AC source to the DC load and the capacitor C_o is charged, and the opposite direction that corresponds to the inverter working mode, current flows from the load to the AC source, when the capacitor C_o is overcharged.

Besides this regulatory contour, usually there is also an internal, mostly current controlled contour.

The converter from Fig. 7.45 is four-square and it can work as a (Fig. 7.46) [4]

- rectifier with unity power factor,
- inverter with unity power factor,
- capacitive source with zero power factor, and
- reactive source with zero power factor.

From the practical side, the most important application of this converter is as a rectifier and inverter with a low content of input current harmonics and a power factor close to one.

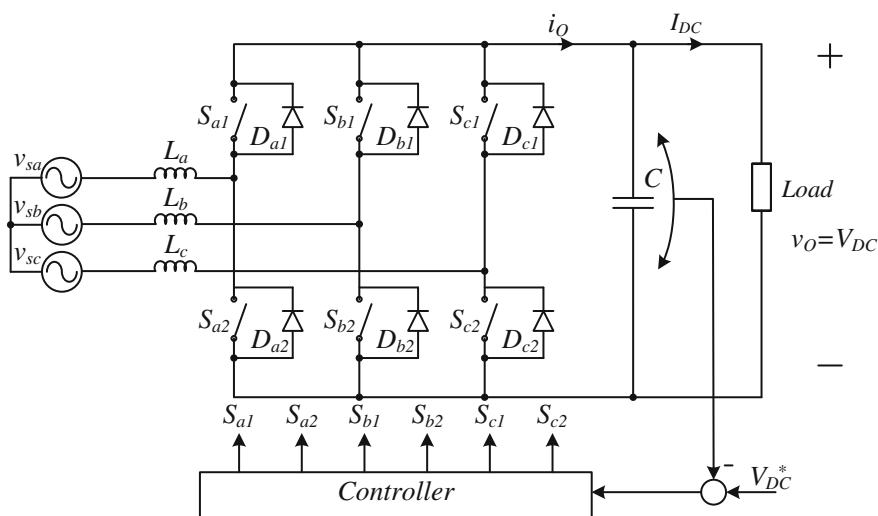


Fig. 7.45 Three-phase PWM boost rectifier with control structure by the output voltage

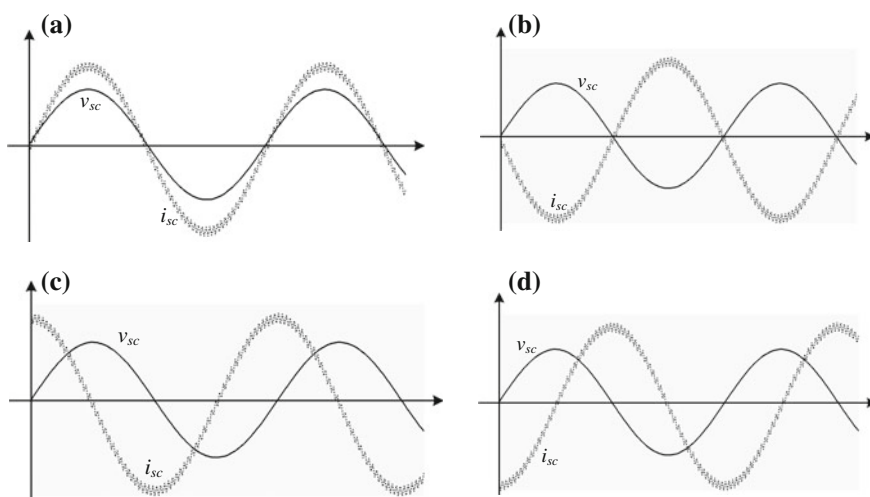


Fig. 7.46 Four operation modes of voltage PWM rectifier

The control of switches in a rectifier bridge is similar to that of the active rectifier with a hysteresis current regulator. To that purpose one branch of the single-phase rectifier from Fig. 7.47 is observed with the PWM generated control signals and the reference signal with the frequency of 50 Hz (Fig. 7.48).

If the direction of the phase current is as shown in Fig. 7.47, the switch S_{b2} , or the diode D_{b1} can be turned on. If the switch S_{b2} is turned on, the current contour

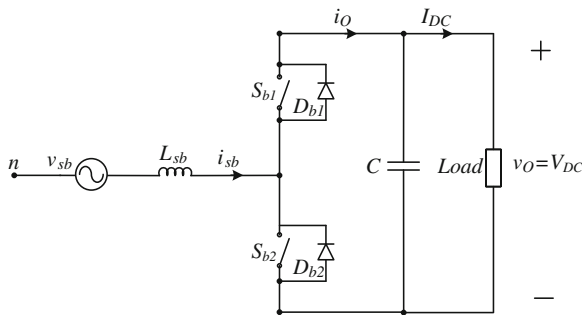


Fig. 7.47 One branch of the single-phase PWM rectifier from Fig. 7.45

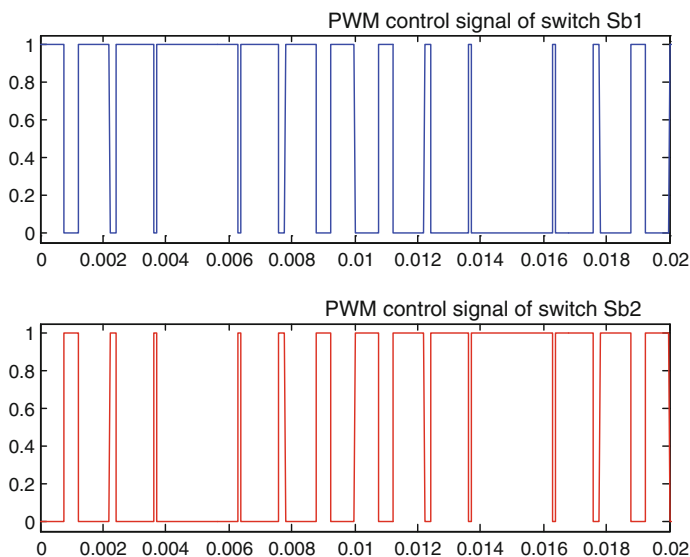


Fig. 7.48 One phase of three-phase boost rectifier with PWM control signals that lead to switches S_{b1} and S_{b2}

can be closed over one of the lower diodes, a or c phase, or through one of the above switches, a or c phase (inverter operation mode, the current direction is opposite compared to that in Fig. 7.47). If the diode D_{b1} and one lower diode are turned on, the capacitor C_o is charged. For this operation of the rectifier the inductance L_{sb} is very important, because the voltage induced on it allows turning on the diode D_{b1} .

Analogously, for the opposite direction of the current i_{sb} the transistor S_{b1} or the diode D_{b2} is turned on.

To ensure complete control of the inverter, the diode can conduct only if one transistor in the bridge is turned on. This is achieved if the voltage on the capacitor

is greater than the maximum line to line voltage. Otherwise it may happen that the PWM rectifier works as a three-phase diode bridge rectifier.

One control scheme of three-phase boost PWM rectifier with voltage external and current internal loop is shown in Fig. 7.49.

The reference values of the phase currents are compared to the measured values and their difference is kept in a PWM controller. A particular phase current should be increased or decreased in order to maintain the DC link voltage at a given value and keep the appropriate phase position between the input current and voltage phase.

Depending on the current direction, this converter can operate as a boost rectifier, when power flows from the source to the load (the direction of the current i_o is to the load) or as a buck inverter, when power flows from the load to the source (the direction of the current i_o is from the load). This method of rectifier control has certain drawbacks. Control is realized by the present value of current references that are sinusoidal. In this case the current regulator must be fast. It is usually implemented as a hysteresis controller, or with the periodic sampling, characterized by a variable frequency of the control signal. The result is the appearance of low frequency subharmonics. Also, the three-phase currents in the steady state are time-variable functions, they are linearly dependent and instead of regulation by the three, it is more practical to realize regulation by two linearly independent variables.

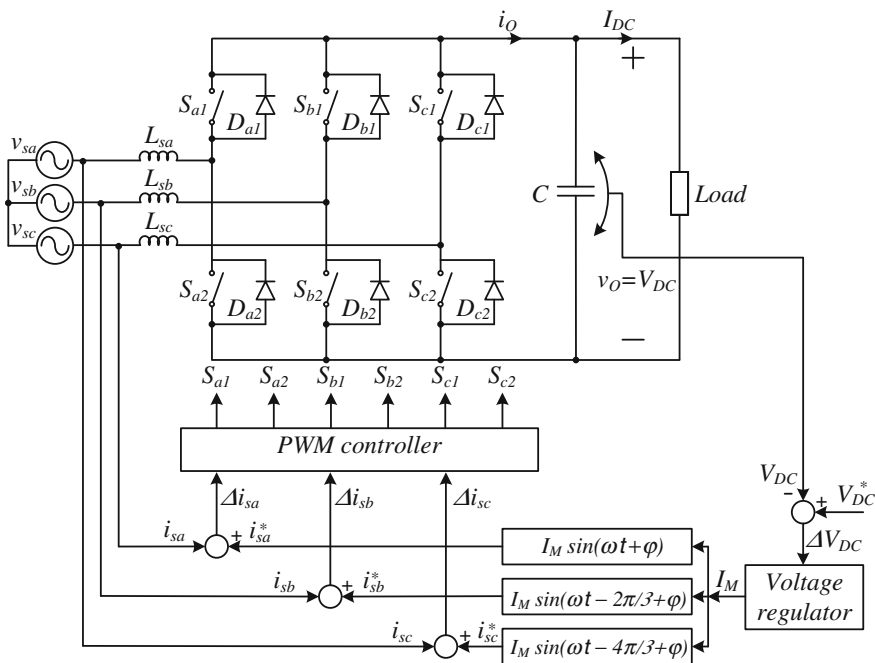


Fig. 7.49 Control of three-phase boost PWM rectifier with voltage external and current internal control loop [4]

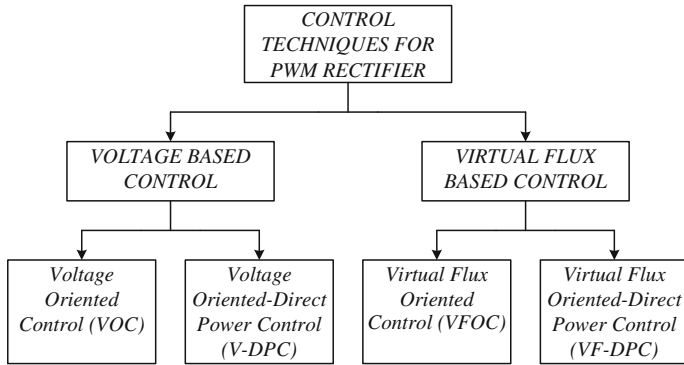


Fig. 7.50 Control strategies for PWM rectifier

7.10.1 Advanced Control Techniques of PWM Rectifiers

Control techniques for PWM rectifiers are extensively researched. Depending on the mapping of control variables from a stationary to a rotational coordinate system they can be classified into two categories (Fig. 7.50) [3]:

1. Voltage oriented control—VOC
2. Virtual flux oriented control—VFOC

Input currents in the d, q rotating system (VOC, VFOC), or the information about the active and reactive power at the DPC technique are used as control variables.

7.10.1.1 Orientation of Rotating D, Q Coordinate System Toward the Line Voltage Vector (VOC-Voltage Oriented Control)

The principle of orientation of the d, q rotating coordinate system toward the line voltage is shown in Fig. 7.51. The first three-phase independent voltages are transformed in two independent voltages (Clarke transformation) and then used to determine the position of the d, q coordinate system (ϑ_e) relative to the stationary α, β coordinate system (Fig. 7.52).

$$\begin{aligned}
 v_{sz} &= |v_s| \cos(\vartheta_e) \\
 v_{s\beta} &= |v_s| \sin(\vartheta_e) \\
 \vartheta_e &= \arctg\left(\frac{v_{s\beta}}{v_{sz}}\right)
 \end{aligned} \tag{7.80}$$

The assumptions for phase resistance and phase inductance are: $R_a = R_b = R_c = R$ and $L_a = L_b = L_c = L$.

Fig. 7.51 Procedure for determining the position of line voltage vector

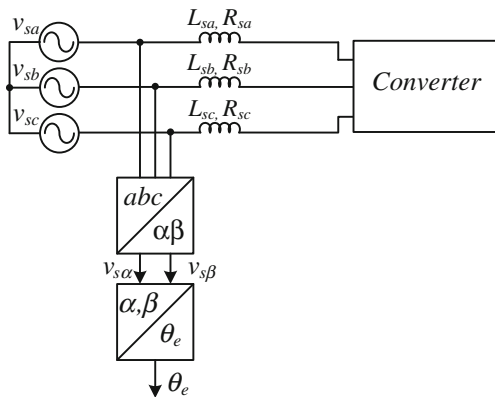
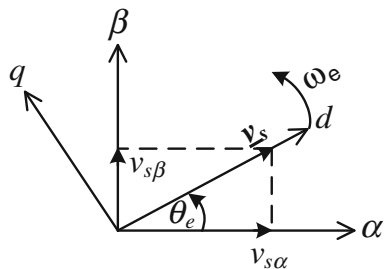


Fig. 7.52 Orientation of d , q coordinate system toward the line voltage vector—VOC



7.10.1.2 Orientation of Rotating D,Q Coordinate System Toward the Virtual Flux Vector—VFOC

This technique for positioning the rotational d , q coordinate system is most simply explained so the resistance $R_a = R_b = R_c = R$ and inductance $L_a = L_b = L_c = L$ are observed like the stator resistance and the stator inductance of a virtual AC motor, whose line voltages v_{ab} , v_{bc} and v_{ca} are induced, due to the effects of a virtual magnetizing flux (Fig. 7.53).

Let the $\Psi_{\alpha L}$ and $\Psi_{\beta L}$ be the components of the virtual flux vector in the stationary α , β coordinate system. Denote with $\underline{v}_L$ the input voltage vector of the converter, $\underline{v}_s$ —is the vector of induced voltage, $\underline{i}_s$ —is the vector of induced current, and $\underline{v}$, $\underline{\Psi}$ are vectors of the voltage and the flux of the inductance L , respectively (Fig. 7.54). For the vectors of the virtual voltage and the flux it can be written that

$$\begin{aligned}\underline{\Psi}_L &= \underline{\Psi}_s + \underline{\Psi} \\ \frac{d\underline{\Psi}_L}{dt} &= \underline{v}_s + L \frac{d\underline{i}_s}{dt}\end{aligned}\quad (7.81)$$

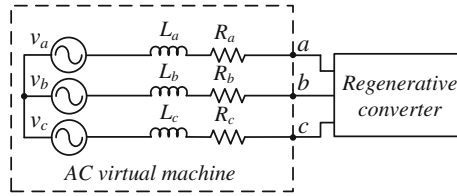


Fig. 7.53 Model to determine the virtual flux

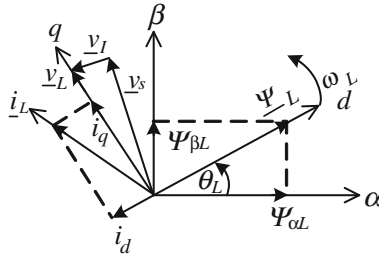


Fig. 7.54 Orientation of d, q coordinate system toward virtual flux—VFOC

If the vector equation in (7.81) is expressed over the components in the α, β coordinate system, the following equations are obtained

$$\begin{aligned} \frac{d\Psi_{\alpha L}}{dt} &= v_{s\alpha} + L \frac{di_{s\alpha}}{dt} \\ \frac{d\Psi_{\beta L}}{dt} &= v_{s\beta} + L \frac{di_{s\beta}}{dt} \end{aligned} \quad (7.82)$$

or

$$\begin{aligned} \Psi_{\alpha L} &= \int \left(v_{s\alpha} + L \frac{di_{s\alpha}}{dt} \right) dt \\ \Psi_{\beta L} &= \int \left(v_{s\beta} + L \frac{di_{s\beta}}{dt} \right) dt \\ \vartheta_L &= \arctg \left(\frac{\Psi_{\beta L}}{\Psi_{\alpha L}} \right) \end{aligned} \quad (7.83)$$

The rotational d, q coordinate system is oriented so that the virtual flux vector coincides with the d axis, and the angular speed ω_L of the coordinate system is equal to the virtual flux angular speed. Position of the rotational d, q coordinate system relative to stationary α, β is equal to angle ϑ_L (Fig. 7.54). One of the most frequently applied control techniques for PWM rectifiers is *VOC* (Fig. 7.55). The current controller is realized in the d, q coordinate system, usually as a linear PI controller.

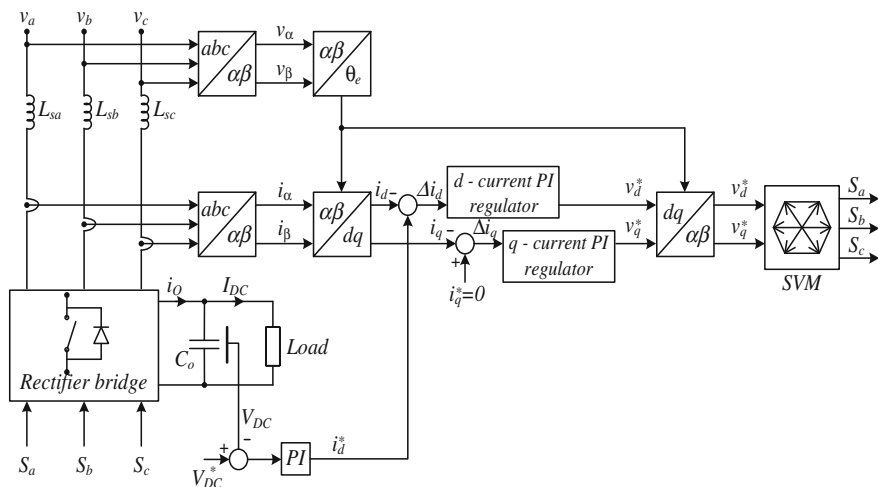


Fig. 7.55 Voltage PWM rectifier with VOC control circuit

The outputs of the controller are the output references that are led to the PWM modulator. The modulator is usually implemented as a sine-wave, or SV modulator. The waveforms of the input current and their spatial vector are shown in Fig. 7.56. Based on the space vector of the input currents, it can be concluded that there is a certain asymmetry between the vector components in a real system, as well as the presence of higher harmonics. It is therefore desirable to filter the input current, especially if it is used in the control algorithm (Fig. 7.55).

A comparative review of techniques for the control of PWM rectifiers is shown in Table 7.2. Besides the previously described technique for the control of PWM rectifiers, there are the other techniques (Fig. 7.50). Each of them has advantages

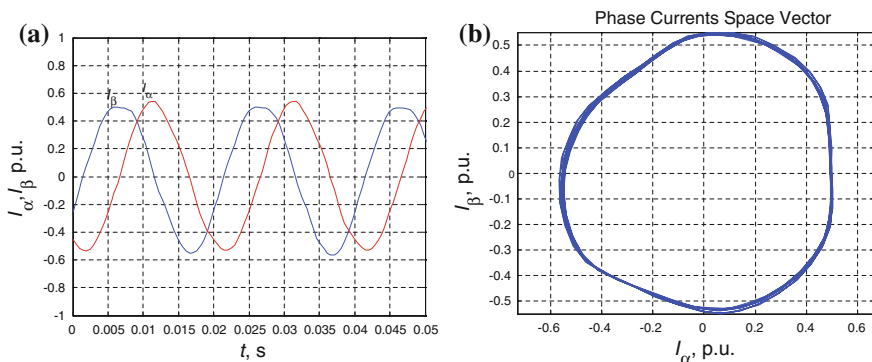


Fig. 7.56 Waveforms of α and β components of input current vector (a), Space vector of input currents (b)

Table 7.2 Comparative overview of techniques for the control of PWM rectifiers [5]

Control technique	Advantages	Drawbacks
VOC	Fixed switching frequency Advanced PWM strategies can be used Simple A/D converters can be used	Power factor is lower than for DPC Complex algorithm Coordinate transformation is required
DPC	Good dynamic characteristics No inner current regulation loop No coordinate transformation Decoupled active and reactive power control	Variable switching frequency Fast microprocessors and A/D converters required High inductance and sample frequency needed
VFOC	Fixed switching frequency (simple input filter) Advanced PWM strategies can be used Simple A/D converters can be used	Input power factor is less than for VF-DPC Complex algorithm Coordinate transformation is required
VF-DPC	Simple power estimation algorithm (easy to implement in a DSP) Lower sampling frequency than for DPC Good dynamic characteristics No inner current regulation loop No coordinate transformation Decoupled active and reactive power control	Variable switching frequency Fast microprocessors and A/D converters required

and disadvantages and the choice of a particular technique depends on the specific characteristics required from the PWM rectifier.

Generally, the DPC techniques have many advantages, particularly the VF-DPC. They give better a input power factor than the VOC and VFOC techniques, they are simpler and do not require an internal current control loop. Their general deficiency is a variable switching frequency, thus for applications where a fixed switching frequency is required, the VOC or VFOC techniques have to be used.

7.10.2 PWM Rectifier with Current Output

The PWM rectifier with current output should be realized so that the desired value of load current is $i_o = I_{DC}$. The input is connected to an AC power source, usually a symmetrical three-phase AC power supply system. A PWM current rectifier with related control logic is shown in Fig. 7.57. Unlike the PWM rectifier with voltage output, the rectifier with the current output does not have an output capacitive filter, but has a capacitive input filter. The function of this filter is to remove the higher current harmonics which appear as consequence of the applied PWM control techniques, so the input current i_s has a shape close to sinusoidal.

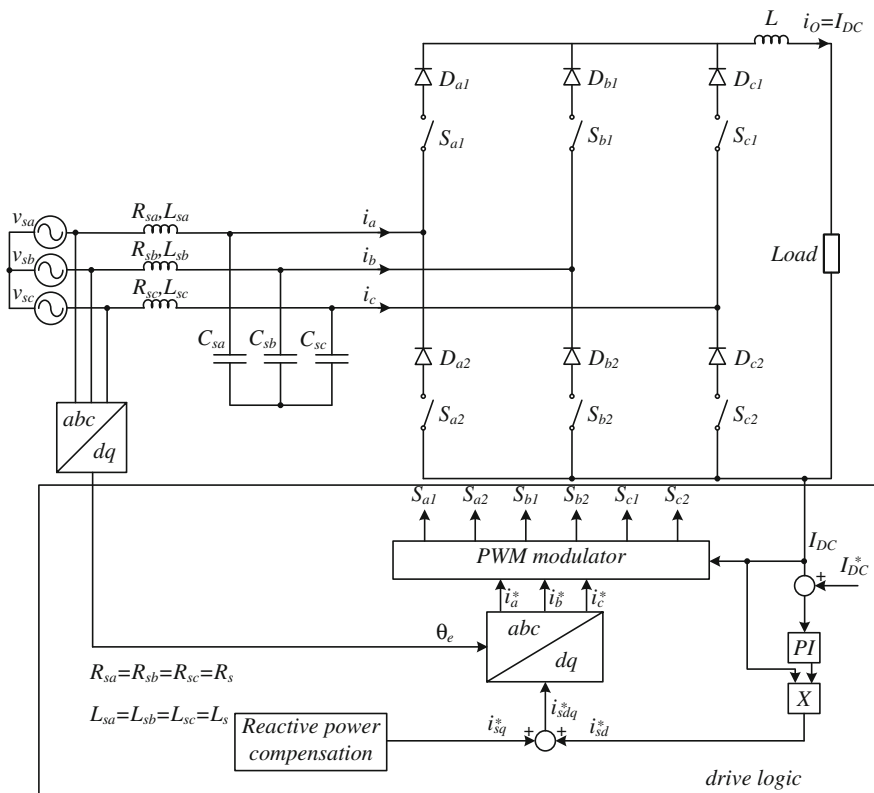


Fig. 7.57 PWM current rectifier with control logic

In the realization of the PWM rectifier control circuit with current output certain peculiarities must be taken into account. The AC input has a predominantly capacitive character, so that the input side must not be short connected and at one moment only one upper (S_{a1}, S_{b1}, S_{c1}) and one lower switch (S_{a2}, S_{b2}, S_{c2}) can conduct. On the other side, the DC bus has current character, so the current circuits must not be broken at any moment. At least one upper and one lower switch must be turned on. The permissible states of the PWM rectifier switches and the values of the input currents that correspond to these states are shown in Table 7.3.

Usually, besides the basic functions of control circuit to maintain output current on desired value, it is also required that the input current be synchronized with the input voltage, i.e. to achieve an appropriate phase shift between the input phase currents and voltages.

To control the PWM rectifier with current output similar techniques are used as those for the PWM rectifier with voltage output. The voltage oriented control technique with control of active and reactive power applied to the PWM rectifier with current output is shown in Fig. 7.57. The orientation of the d, q system is along the vector of input line voltages (Fig. 7.52).

Table 7.3 Permissible states of PWM rectifier switches and values of input currents that correspond to these states

Switch						State	Input current		
S_{a1}	S_{b1}	S_{c1}	S_{a2}	S_{b2}	S_{c2}		i_a	i_b	i_c
1	0	0	0	0	1	1	I_{DC}	0	$-I_{DC}$
0	1	0	0	0	1	2	0	I_{DC}	$-I_{DC}$
0	1	0	1	0	0	3	$-I_{DC}$	I_{DC}	0
0	0	1	1	0	0	4	$-I_{DC}$	0	I_{DC}
0	0	1	0	1	0	5	0	$-I_{DC}$	I_{DC}
1	0	0	0	1	0	6	I_{DC}	$-I_{DC}$	0
1	0	0	1	0	0	7	0	0	0
0	1	0	0	1	0	8	0	0	0
0	0	1	0	0	1	9	0	0	0

The expressions for active and reactive power in the rotating d, q system for the system invariant in amplitude are

$$\begin{aligned} p &= \frac{3}{2} (v_{sd} i_{sd} + v_{sq} i_{sq}) \\ q &= \frac{3}{2} (v_{sq} i_{sd} - v_{sd} i_{sq}) \end{aligned} \quad (7.84)$$

Since the orientation of the vector $\underline{v}_s$ is such that it coincides with the d axis, from (7.84) it follows that

$$\begin{aligned} p &= \frac{3}{2} v_{sd} i_{sd} \\ q &= -\frac{3}{2} v_{sd} i_{sq} \end{aligned} \quad (7.85)$$

Assuming that $|\underline{v}_s| = \text{const.}$ from (7.85) it can be concluded that the active power is controlled by the d component of the input current (i_{sd}) and the reactive power by the q component (i_{sq}).

Example 7.6 To control a PWM rectifier, the VFO technique is used. The amplitude of the virtual flux vector is 1.52 Wb, and its frequency is 50 Hz. The vector of line current has an amplitude equal to 12 A and a phase displacement of 135° . Determine the instantaneous active and reactive power at the input of the three-phase PWM voltage rectifier.

Instantaneous power at the input of PWM rectifier can be calculated using complex notation:

$$\begin{aligned} p &= \text{Re}(\underline{v_L} \times \underline{i_L}^*) \\ q &= \text{Im}(\underline{v_L} \times \underline{i_L}^*) \end{aligned} \quad (7.86)$$

The line voltage vector in the d, q rotating coordinate system oriented toward the virtual flux vector is

$$\underline{v_L} = \frac{d\underline{\Psi_L}}{dt} + j\omega L \underline{\Psi_L}. \quad (7.87)$$

The instantaneous power can be calculated as:

$$\underline{v_L} \times \underline{i_L}^* = \frac{d\underline{\Psi_L}}{dt} \underline{i_L}^* + j\omega L \underline{\Psi_L} \underline{i_L}^*. \quad (7.88)$$

Since the coordinate system is oriented toward the virtual flux vector, it follows that

$$\Psi_{Lq} = 0 \quad \text{i.e.} \quad \underline{\Psi_L} = \Psi_{Ld} \quad (7.89)$$

For sinusoidal and symmetrical line voltage in steady state it is

$$\frac{d\underline{\Psi_{Ld}}}{dt} = 0. \quad (7.90)$$

The components of the line current vectors are

$$\begin{aligned} i_{Ld} &= |\underline{I_L}| \cos \vartheta = 3.1 \text{ A and} \\ i_{Lq} &= |\underline{I_L}| \sin \vartheta = 11.59 \text{ A.} \end{aligned} \quad (7.91)$$

From (7.87), (7.88) and taking into account Eqs. (7.89) (7.90) and (7.91) it can be written

$$\begin{aligned} \underline{v_L} \cdot \underline{i_L}^* &= j\omega \Psi_{Ld} (i_{Ld} - ji_{Lq}) = \omega \Psi_{Ld} i_{Lq} + j\omega \Psi_{Ld} i_{Ld} \\ p &= \omega \Psi_{Ld} i_{Lq} = 5.534 \text{ kW} \\ q &= \omega \Psi_{Ld} i_{Ld} = 1.48 \text{ kVar} \end{aligned}$$

The reference current $i_{sd}(i_{sd}^*)$ is obtained from the controller of the DC link current which is typically realized as a linear PI controller (Fig. 7.57). Based on the reference of the reactive power and a new reference of the q component the input current vector i_{sq}^* is generated. The inverse Park's transformation is used to get the reference of the input current vector $\underline{i_s}^*$ which is utilized as a control variable in the

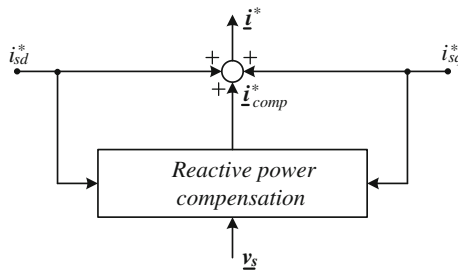


Fig. 7.58 Compensation of input current vector [6]

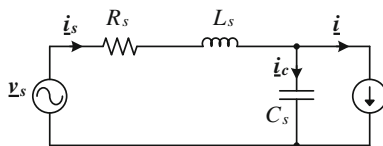


Fig. 7.59 Circuit for determination of compensating current vector

PWM modulator. To generate control signals different modulation techniques can be used: sinusoidal modulation, selective harmonic elimination, space vector modulation, etc.

The input filter generates an error in the reference input current vector, and it is necessary to make its compensation. This compensation can be realized according to the scheme shown in Fig. 7.58, from the equation of the input circuits in steady state (Fig. 7.59):

$$\begin{aligned} \underline{i}_s &= \underline{i}_c + \underline{i} \\ \underline{v}_s &= R_s \underline{i}_s + L_s \frac{d\underline{i}_s}{dt} + \frac{1}{C_s} \int (\underline{i}_s - \underline{i}) dt \end{aligned} \quad (7.92)$$

The compensating current vector $\underline{i}_{comp}^*$ is added to the reference current vector $\underline{i}_s^*$ which gives the vector $\underline{i}^*$

$$\begin{aligned} \underline{i}_d^* &= \underline{i}_{sd}^* + \underline{i}_{compd}^* \\ \underline{i}_q^* &= \underline{i}_{sq}^* + \underline{i}_{compq}^* \end{aligned} \quad (7.93)$$

and it leads to the PWM modulator.

Besides the described one, there are many other control techniques for PWM rectifiers that differ the complexity of the control algorithm and that relate to the quality of the output current, the possibility of power factor correction, filtering the input current, etc.

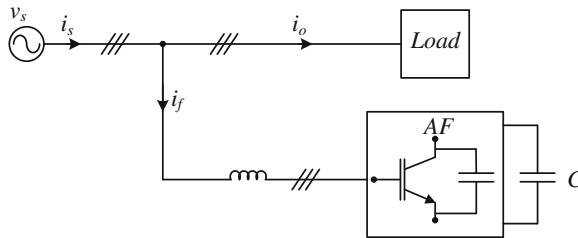


Fig. 7.60 Three-phase active shunt filter with nonlinear load

7.10.3 PWM Rectifiers in Active Filters

PWM rectifier can be used in the circuit for active filtering. An example is a the shunt active filter shown in Fig. 7.60 [7]. The active filter is realized as a three-phase, two level PWM rectifier with a voltage output. This filter provides a controlled current i_f which is added to the current i_o (due to nonlinear loads this current can deviate significantly from the sinusoidal shape) in order to obtain a sinusoidal shape of the line current $i_s = i_f + i_o$.

The advantages of thus realized active filter are:

- load balancing, and
- harmonic compensation.

Besides the good features, active filters have certain disadvantages, such as the complex control, higher switching losses, as well as problems related to electromagnetic interference. Due to the occurrence of electromagnetic interference (switching noise that exists in the input currents), it is necessary to use small low-pass filter between the power line and the active filter.

7.10.4 Some Topologies of PWM Rectifiers

In the previous exposition of PWM rectifiers attention was given to those topologies that have found the most practical applications and to the techniques for the control of such rectifiers. Besides those described, there are rectifier topologies for specific applications.

A three-phase boost rectifier is presented in Fig. 7.61. Its main advantage is a possibility to increase the output voltage. Furthermore, this topology provides a stable output voltage with very small variations, and it can be used for power factor correction.

A Vienna rectifier is presented in Fig. 7.62. This rectifier belongs to the class of AC/DC converters with current input and voltage output.

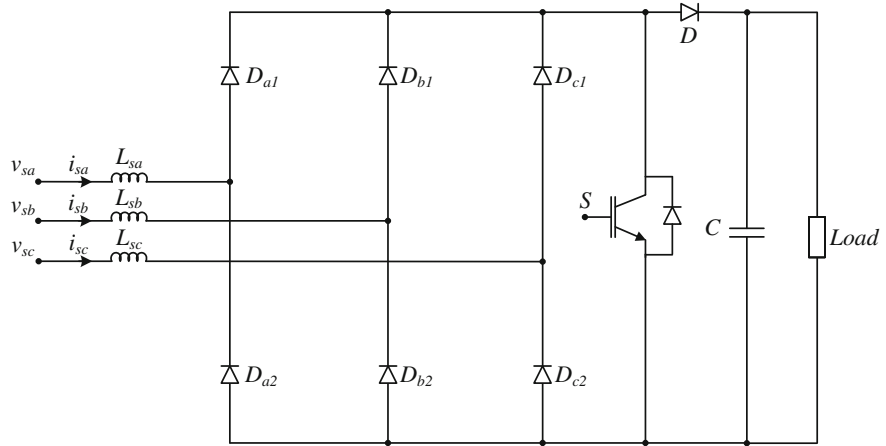


Fig. 7.61 Three-phase boost rectifier

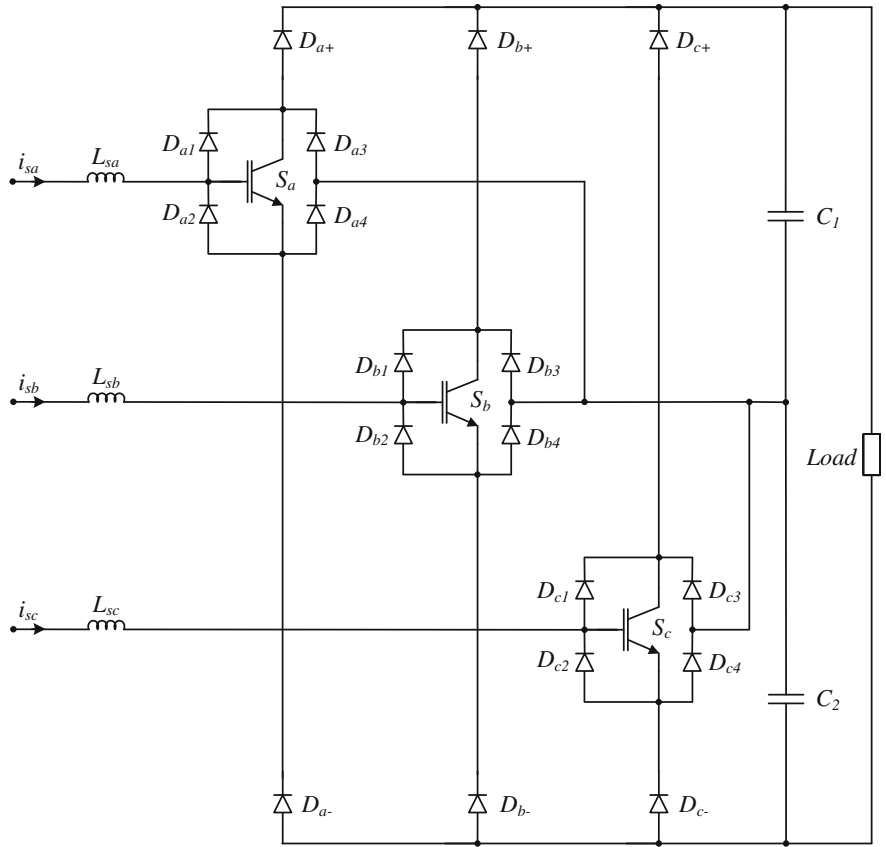


Fig. 7.62 Vienna rectifier

Unlike the three-phase PWM rectifier with voltage output (Fig. 7.43) Vienna rectifier has only three controlled switches, so its control is simplified. This rectifier forces less stress on the switches compared to the PWM rectifiers with voltage output. To control the rectifier directly the current control is usually applied, but also other control techniques such as space vector modulation can be utilized.

The advantages of this rectifier are that it is an inexpensive and robust converter that meets the requirements for the “Clean Power Conversion” considering the possibility of the converter in the input power factor correction [8]. The drawback of this converter is reflected primarily in the fact that this is a one-way converter which only can work in the rectifier mode.

7.10.5 Applications of PWM Rectifiers

PWM rectifiers have found wide use in the realization of modern converters. The most commonly used is the three-phase PWM rectifier with a voltage output (Fig. 7.43) and the PWM rectifier with a current output (Fig. 7.44). In this section only some of many applications of the PWM rectifiers are presented. A drive converter for three-phase induction motors is shown in Fig. 7.63.

Symmetrical three-phase voltage is fed to the input of the PWM rectifier which provides a stable DC voltage and input power factor control. Over the three-phase DC/AC converter one obtains a three-phase voltage with the required amplitude and frequency for supplying the induction motor.

The use of the PWM rectifier enables power flow from the motor to the source (energy recuperation) which is important if the motor works in generator mode.

The power supply system for a traction induction motor is shown in Fig. 7.64. The motor is powered by a primary three-phase power source. In generator mode, it behaves as a source of electrical energy and the drive converter operates as a PWM rectifier and charges the battery. In a case of primary power failure, the converter operates as a PWM inverter and the motor is supplied from the battery.

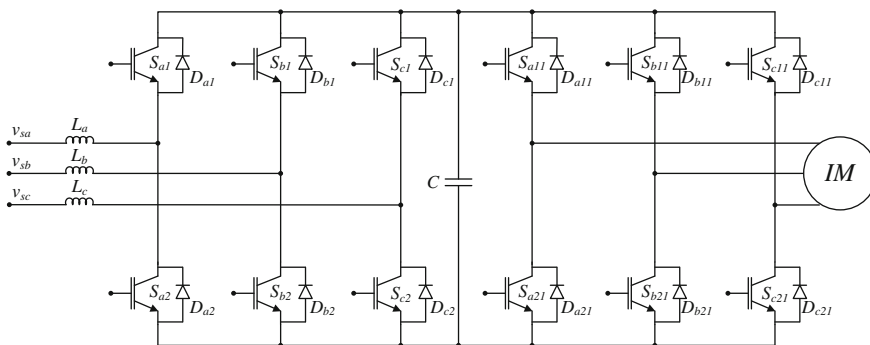


Fig. 7.63 Application of three-phase PWM voltage rectifier in the induction motor drive converter

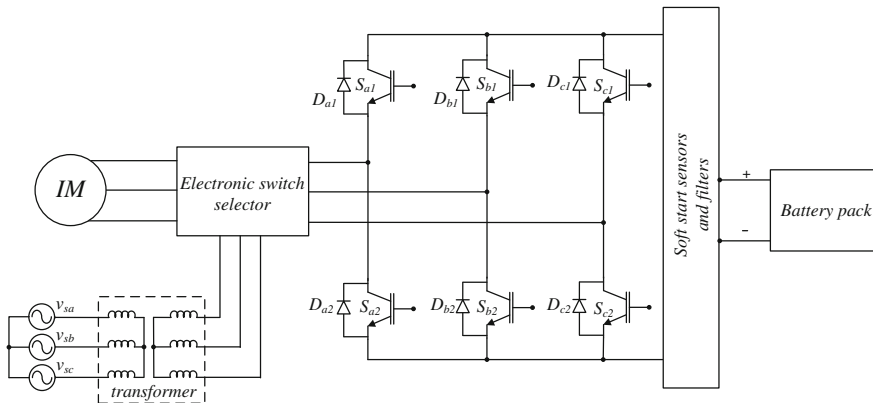


Fig. 7.64 Electric “Bus” system for power supplying of induction motor with the possibility of regenerative braking and battery supplying [4]

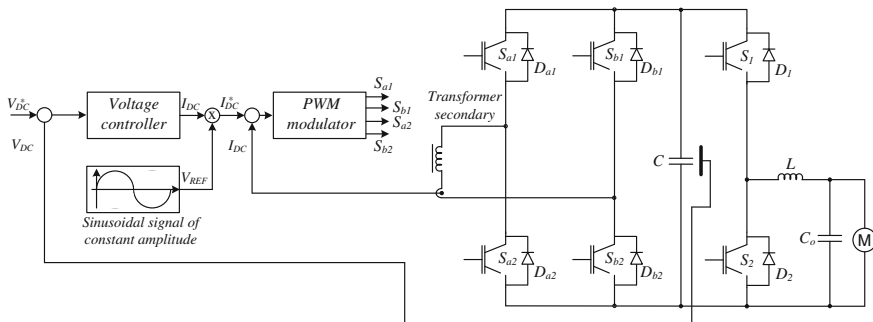


Fig. 7.65 PWM rectifier for power supply of DC traction motor

A PWM rectifier with control logic for aDC traction motor is shown in Fig. 7.65. The voltage on the secondary winding is rectified by the PWM rectifier. Additional filtering and the motor voltage regulation is achieved by using the buck DC/DC converter. This topology allows energy recuperation during the generator mode as well as dynamic braking. The control logic consists of the external voltage contour which provides DC voltage at the desired value and the inner contour with the current controller and the PWM modulator (Sect. 7.10.1).

These are just some of the PWM rectifier applications, which have found their place as converters in renewable energy sources, uninterruptible power supply devices, drive inverters, multilevel converters, etc.

Problems

- 7.1 A single-phase diode bridge rectifier (Fig. 7.4b) has an R - L load with $R = 10\ \Omega$ and $L = 50\text{ mH}$. The AC source is $v_s(t) = 220\sqrt{2}\sin(2\pi 50t)$. Determine
- the average load current, and
 - the power factor.
- 7.2 The full-wave diode bridge rectifier (Fig. 7.4b) has a load with a serial connection of $R = 10\ \Omega$, $L = 50\text{ mH}$ and $V_{DC} = 100\text{ V}$. The AC source is $v_s(t) = 220\sqrt{2}\sin(2\pi 50t)$. Determine
- the power absorbed by the DC source,
 - the power absorbed by the resistor, and
 - the power factor.
- 7.3 The full-wave rectifier from Fig. 7.8a has a load resistance $R = 250\ \Omega$. The AC source is $v_s(t) = 220\sqrt{2}\sin(2\pi 50t)$. Determine the filter capacitance so that the peak to peak output voltage ripple is 2 % of the maximum output voltage.
- 7.4 A controlled single-phase bridge rectifier (Fig. 7.23a) has an R - L load with $R = 100\ \Omega$ and $L = 50\text{ mH}$. The AC source is $v_s(t) = 220\sqrt{2}\sin(2\pi 50t)$. The delay angle is $\alpha = 45^\circ$. Determine
- the average load current, and
 - the power factor
- 7.5 A three-phase diode bridge rectifier is supplied by a 380 V rms line to line 50 Hz voltage. The R - L load is a serial connection of a resistor $R = 50\ \Omega$ and an inductor $L = 25\text{ mH}$. Determine
- the average load current,
 - the rms source current, and
 - the power factor.
- 7.6 The six-pulse controlled three-phase rectifier shown in Fig. 7.28a has an R - L load with $R = 25\ \Omega$ and $L = 50\text{ mH}$. The delay angle is $\alpha = 45^\circ$. The AC source is a symmetrical 380 V rms line to line 50 Hz voltage. Determine
- the average load current, and
 - the amplitude of the sixth harmonic of the load current.
 - Draw the input line to line voltages and the output voltage
- 7.7 The twelve-pulse controlled three-phase rectifier shown in Fig. 7.31 has an R - L load with $R = 10\ \Omega$ and $L = 50\text{ mH}$. The delay angle is $\alpha = 30^\circ$. The AC source is a symmetrical line to line 380 V rms, 50 Hz voltage.
- Determine the average value of the output voltage.
 - Determine the average value of the load current.
 - Calculate the expression for the input AC current.
 - Draw the waveforms of the output voltages.

- 7.8 For the rectifier with PFC circuit from Fig. 7.37 determine the maximum value of the emulated resistance R_e so the converter works in CCM. The converter has $L = 10$ mH and an output voltage 48 V DC. The switching frequency is $f = 20$ kHz. The input voltage of the rectifier is AC 24 V rms, 50 Hz.
- 7.9 To control the PWM rectifier with current output shown in Fig. 7.44 the VOC technique is used. The input filter has $C = 1$ mF, $L = 100$ mH and $R = 10$ Ω . Determine the compensation current if the input voltage is three-phase AC with 380 V rms line to line, 50 Hz.

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Chapter 8

AC/AC Converters

AC/AC converters connect an AC supply to an AC load and thereby control the current, voltage, and rms power of the load. In essence, they convert AC voltage/current at one level to AC voltage/current at another level or AC voltage at one frequency to AC voltage at another frequency. Therefore, they are classified as:

- AC/AC voltage converters, and
- AC/AC frequency converters.

They can be single-phase or polyphase (mostly three-phase).

AC/AC voltage converters control the rms value of the load voltage at a constant frequency. Usually they are used for controlling the power for heaters or for starting AC motors.

AC/AC frequency converters change the frequency of the voltage/current of the load compared to the frequency of the source. They may be direct or indirect (having a DC internal stage). They are mainly used for controlling the speed of AC motors or for induction heating.

The main switching elements of the conventional AC/AC converters are thyristors and triacs.

8.1 Single-Phase AC/AC Voltage Converters

A single-phase voltage converter consists of a pair of anti-parallel (inverse-parallel) thyristors T_{h1} and T_{h2} and a control module CM (Fig. 8.1a). Instead of the thyristors T_{h1} and T_{h2} one triac TC may be used (Fig. 8.1b).

The thyristor T_{h1} is conducting during a part of the positive cycle, and the thyristor T_{h2} is conducting during the same part of the negative cycle of the input voltage. In principle, the angle of conduction, α , may be controlled within the limits $0 < \alpha < \pi$. Within each cycle the load current exists when one of the thyristors is on, i.e., for $\alpha \leq \omega t \leq \pi$ and $\pi + \alpha \leq \omega t \leq 2\pi$. In general, the angles of conduction of the

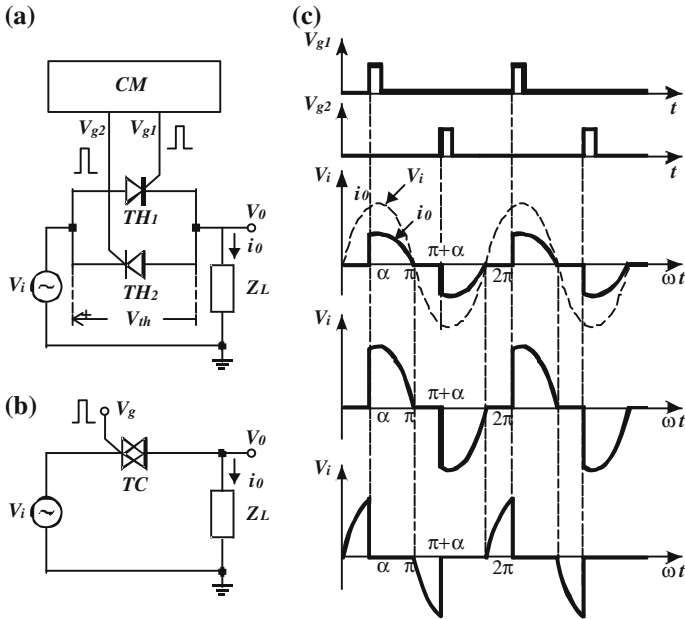


Fig. 8.1 Single-phase voltage converters (a and b) and voltage and current waveforms for a working (resistive) load (c)

thyristors do not have to be the same. The rms value of the load voltage or the load current is controlled by varying the angle of conduction α of the thyristors T_{h1} and T_{h2} . For this reason this principle of control is known as the phase method of converting an AC voltage.

The general conditions and characteristics of these converters can be summarized as follows:

- The thyristors must not be on simultaneously. One is conducting during a part of the positive, and the other during a part of the negative half-cycle of the input voltage. The conducting thyristor is switched off at zero crossing of the current during the change of its direction.
- The load voltage is equal to the input voltage during conduction of one of the thyristors, whereas while both thyristors are off the load voltage is equal to zero.
- The average values of the source and load currents are zero when the angles of conduction of the thyristors are equal.
- The voltages across the thyristors are equal to zero while one of the thyristors is conducting, whereas while they are off the voltages across them, V_{th} , are equal to the input voltage.
- The average value of the current of each thyristor is greater than zero because the thyristor conducts only in one direction. If the angles of conduction of the thyristors are the same, then the rms value of the current of each of them is $1/\sqrt{2}$ times the rms value of the load current.

The control module (CM), generates short pulses which trigger the thyristors via their gates. CM is synchronized so that a triggering pulse comes to the gate of the thyristor T_{h1} during the positive and to the gate of the thyristor T_{h2} during the negative half-cycle of the input voltage. Thus, the CM determines the angles of conduction of the thyristors. When these angles are equal, this is denoted as the symmetrical control.

Resistive load

In the case of a purely working (resistive) load the output voltage v_0 and the current i_0 are in phase (Fig. 8.1c). If the input voltage is a harmonic function of time $v_i = V_M \sin(\omega t)$, the output voltage during one cycle is

$$v_0(\omega t) = \begin{cases} V_M \sin(\omega t), & \alpha < \omega t < \pi, \alpha + \pi < \omega t < 2\pi \\ 0, & \text{otherwise.} \end{cases} \quad (8.1)$$

Since the control is symmetric, the average values of the source and the load currents are equal to zero. The average values of the thyristor currents are

$$I_{Th,av} = \frac{1}{2\pi} \int_{\alpha}^{\pi} \frac{V_M}{R_L} \sin(\omega t) d(\omega t) = \frac{V_M}{2\pi R_L} (1 + \cos \alpha), \quad (8.2)$$

where R_L is the load resistance.

Since the waveforms of the output voltage during the positive and negative half-cycles are symmetric, the rms value of this voltage is

$$V_{0,rms} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\pi} [V_M \sin(\omega t)]^2 d(\omega t)} = \frac{V_M}{\sqrt{2}} \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}}. \quad (8.3)$$

The dependence of the rms value of the output voltage on the angle of conduction is the control characteristic of an AC/AC voltage converter (Fig. 8.2). For $\alpha = 0$, the load voltage is a sine function equal to the rms value of the source voltage ($V_{0,rms} = V_M/\sqrt{2}$). If $\alpha = 180^\circ$, both thyristors are permanently off and the output voltage is equal to zero.

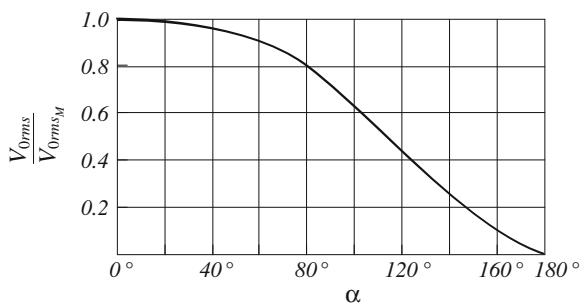
The rms values of the load and source currents are equal

$$I_{0,rms} = I_{i,rms} = \frac{V_{0,rms}}{R_L}. \quad (8.4)$$

Using (1.38), the load power factor is

$$PF = \frac{V_{0,rms}^2 / R_L}{V_{i,rms} (V_{0,rms} / R_L)} = \frac{\frac{V_M}{\sqrt{2}} \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}}}{V_M / \sqrt{2}} = \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}}. \quad (8.5)$$

Fig. 8.2 Normalized control characteristic of a phase AC/AC voltage converter



Since each of the thyristors is conducting one half of the symmetric load current, the rms value of the thyristor current is

$$I_{Th,rms} = \frac{I_{0,rms}}{\sqrt{2}}. \quad (8.6)$$

The inverter currents are not sinusoidal, but complex periodic functions of time. In view of (1.22), (8.2), and (8.6) the form factor is:

$$k = \frac{I_{Th,rms}}{I_{Th,av}} = \frac{\pi \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}}}{1 + \cos \alpha}. \quad (8.7)$$

Example 8.1 An AC/AC voltage converter made of two thyristors in anti-parallel connection (Fig. 8.1a) and driven by a harmonic 220 V, 50 Hz voltage is loaded by a resistor $R_L = 2.2 \, \Omega$. The holding voltage of the thyristors is $V_H = 1 \, \text{V}$ and the resistance while conducting $r_d = 5 \, \text{m}\Omega$. If the required power of the load (heater) is $P_L = 11 \, \text{kW}$, determine:

- angle of conduction of the thyristors,
- load power factor,
- power of dissipation in one of the thyristors, and
- form factor of the thyristor current.

(a) The rms value of the load voltage is determined by

$V_{0,rms} = \sqrt{P_L R_L} = \sqrt{11 \times 10^3 \times 2.2} = 155.56 \, \text{V} = 220 \, \text{V} / \sqrt{2}$, so taking into account (8.3)

$$\frac{220}{\sqrt{2}} = 220 \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}},$$

where from it turns out that $\alpha = \pi/2$.

(b) From (8.5) it follows that for $\alpha = \pi/2$ the power factor is $\text{PF} = \sqrt{0.5} = 0.707$.

(c) The power of dissipation in one of the thyristors is determined by

$$P_D = V_H I_{Th,av} + r_d I_{Th,rms}^2, \text{ and in view of (8.2), (1.30), and (8.4)}$$

$$P_D = V_H \frac{\sqrt{2} V_{L,rms}}{2\pi R_L} (1 + \cos \alpha) + r_d \frac{(\sqrt{2} V_{L,rms})^2}{2R_L^2} \left(1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi} \right) = 35 \text{ W}.$$

(d) From (8.7) it follows that the form factor of the thyristor current is

$$k = \frac{\pi \sqrt{1 - \frac{\pi/2}{\pi} + \frac{\sin(2\alpha)}{2\pi}}}{1 + \cos(\pi/2)} = \frac{\pi \sqrt{1/2}}{2} = 0.35 \pi.$$

Predominantly inductive load

A predominantly inductive load implies an R - L load (Fig. 8.3) where the influence of the inductance is predominant. The inductance changes the character of the load current and voltage. Compared to a purely resistive load, where the current and the voltage are in phase, here the inductance slows down the variations of the load current (Fig. 8.3b). For this reason there exists a phase delay of the load current compared to the phase of the load voltage. In other words, the current i_0 flows through the load and the corresponding thyristor after the source voltage has crossed zero, reaching the zero value at an angle $\omega t = \beta$ in the next half-cycle of the input voltage, V_i (Fig. 8.3b). Owing to this the angle of thyristor conduction is increased to $\beta - \alpha$, and the output voltage exhibits both positive and negative abrupt changes during one half-cycle (Fig. 8.3b).

Let a positive triggering pulse be applied to the gate of the thyristor T_{h1} at $\omega t = \alpha$. Then T_{h1} turns on. By neglecting the voltage drop across T_{h1} one may write

$$v_i = V_M \sin(\omega t) = R i_0(t) + L \frac{di_0(t)}{dt}. \quad (8.8)$$

The solution of (8.8) is

$$i_0(t) = \begin{cases} \frac{V_M}{Z} \left[\sin(\omega t - \Theta) - \sin(\alpha - \Theta) e^{(\alpha - \omega t)/(\omega \tau)} \right], & \alpha < \omega \tau < \beta, \\ 0, & \text{otherwise.} \end{cases} \quad (8.9)$$

where

$$Z = \sqrt{R^2 + (\omega L)^2}, \quad \Theta = \tan^{-1}(\omega L/R) \text{ and } \tau = L/R. \quad (8.10)$$

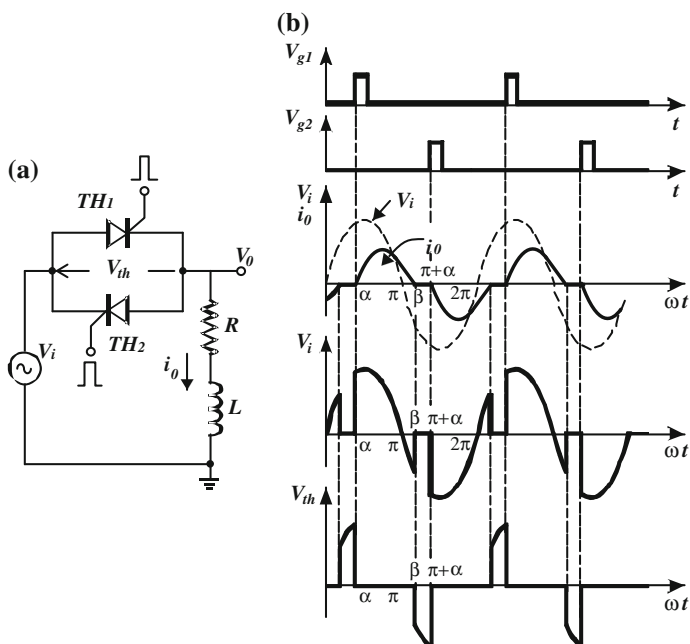


Fig. 8.3 Single-phase AC/AC converter having an R - L load (a) and the corresponding voltage and current waveforms (b)

The angle $\omega t = \beta$, at which the load current crosses zero is determined from the condition:

$$i_o(\beta) = \frac{V_M}{Z} \left[\sin(\beta - \Theta) - \sin(\alpha - \Theta)e^{(\alpha - \beta)/(\omega\tau)} \right] = 0. \quad (8.11)$$

The rms value of the load voltage is determined by

$$V_{0,\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\beta} V_M^2 \sin^2(\omega t) d(\omega t)} = \frac{V_M}{\sqrt{2}} \sqrt{\frac{1}{\pi} \left[\beta - \alpha + \frac{1}{2} \sin(2\alpha) - \frac{1}{2} \sin(2\beta) \right]}. \quad (8.12)$$

This voltage has the highest value if the angle α is such that the corresponding thyristor is turned on when the other is turned off. This angle is called the critical control angle:

$$\alpha_c = \beta - \pi. \quad (8.13)$$

Example 8.2 For a single-phase AC/AC converter having an R - L load (Fig. 8.3a) it is known that $R = 1.73 \, \Omega$, $L = 3.185 \, \text{mH}$, and that the source voltage is harmonic with $V_{s,\text{rms}} = 220 \, \text{V}$ and $f = 50 \, \text{Hz}$. One should determine:

- (a) the critical conduction angle, α_c ,
- (b) the turning off angle, β , and the power factor at $\alpha = \pi/4$.

(a) From (8.11) and (8.13) it follows that

$$\alpha_c = \arctg(\omega L/R) = \pi/6.$$

(b) The turning off angle β of the thyristor is a function of the angle of conduction control, α , and it is determined from (8.11), i.e.

$$\sin(\beta - \Theta) - \sin(\alpha - \Theta)e^{(\alpha - \beta)/(\omega L/R)} = 0,$$

or from: $\frac{\beta - \alpha}{\omega L/R} + \ln[\sin(\beta - \Theta)] = \ln[\sin(\alpha - \Theta)]$, for $\alpha = \pi/4$, $\beta = 210^\circ$

In order to determine the load power factor, it is necessary to determine the rms value of the load voltage or current. The rms value of the current is

$$I_{0,\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\alpha}^{\beta} i_0^2(\omega t) d(\omega t)},$$

and, taking into account (8.9)

$$\begin{aligned} I_{0,\text{rms}}^2 &= \frac{I_M^2}{\pi} \int_{\alpha}^{\beta} \left[\sin(\omega t - \Theta) - \sin(\alpha - \Theta)e^{(\alpha - \omega t)/(\omega L/R)} \right]^2 d(\omega t) = \frac{I_M^2}{\pi} (I_1 - I_2 + I_3), \\ I_2 &= 2 \int_{\alpha}^{\beta} \sin(\omega t - \Theta) \sin(\alpha - \Theta) e^{(\alpha - \omega t)/(\omega L/R)} d(\omega t) \\ &= \frac{2(\omega L/R) \sin(\alpha - \Theta)}{\sqrt{1 + (\omega L/R)^2}} (\sin \alpha - \sin e^{(\alpha - \beta)/(\omega L/R)}) \text{ and} \\ I_1 &= \int_{\alpha}^{\beta} \sin^2(\omega t) d(\omega t) = \frac{\beta - \alpha}{2} - \frac{1}{2} \cos(\beta + \alpha - 2\Theta) \sin(\beta - \alpha), \\ I_3 &= \int_{\alpha}^{\beta} \sin^2(\alpha - \Theta) e^{2(\alpha - \omega t)/(\omega L/R)} d(\omega t) = \frac{\omega L/R}{2} \sin^2(\alpha - \Theta) [1 - e^{2(\alpha - \beta)/(\omega L/R)}]. \end{aligned}$$

Since $\alpha = \pi/4$ and $\beta = 210^\circ$, then $I_1 = 1.56 \, \text{A}$, $I_2 = 0.184 \, \text{A}$, and $I_3 = 0.02 \, \text{A}$. The rms value of the load current is

$$I_{0,\text{rms}} = \frac{\sqrt{2}V_{s,\text{rms}}}{\sqrt{R^2 + (\omega L)^2}} \sqrt{\frac{1}{\pi}(I_1 - I_2 + I_3)} = 103.8 \text{ A.}$$

The load power factor is

$$\text{PF} = \frac{I_{0,\text{rms}}R_L}{V_{s,\text{rms}}} = \frac{103.8 \times 1.73}{220} = 0.82.$$

At $\alpha = \alpha_c$, the angle of conduction of each thyristor is 180° , thus the variations of the current and the voltage are continuous and sinusoidal, so the rms value of the output voltage is $V_{0,\text{rms}} = V_M/\sqrt{2}$. The same mode also exists for $0 < \alpha < \alpha_c$. If $\alpha < \alpha_c$, the triggering pulse has to be sufficiently wide so that it is present at the instant β/ω when the other thyristor is turned off, i.e., $\Delta t > (\alpha_c - \alpha)/\omega$, where Δt is the width of the triggering pulse. If, however, $\Delta t < (\alpha_c - \alpha)/\omega$, the triggering pulse of the other thyristor ends before the currents stops flowing through the conducting thyristor. Consequently, this thyristor remains turned off, i.e., its turning on is skipped. At $\alpha \leq \alpha_c$ the rms value is equal to the rms value of the source, i.e., $V_{0,\text{rms}} = V_M/\sqrt{2}$. For this reason the range $\alpha \leq \alpha_c$ is called the uncontrolled range of the converter where the variation of α does not influence the variations of the rms values of the load voltage and current.

8.1.1 Time Proportional Control

In the time-proportional control of the AC/AC converters the thyristors are on for a number of cycles and are off for another number of cycles. The same circuits as those of the phase control (Figs. 8.1a and 8.3a) are used. The difference is in that in the phase control one thyristor conducts during a part of one half-cycle and the other thyristor conducts during a part of the other half-cycle. In the time proportional control during the time T_{on} the thyristors are conducting during full half-cycles of the AC voltage and during the time T_{off} they are off so the load current and voltage are equal to zero. During the time T_{on} at each zero crossing of the AC voltage the thyristors are synchronously turned on and off, so the load current retains the same form. On the other hand, during T_{off} the triggering pulses are not applied, the anti-parallel thyristors are off and the load is separated from the AC source.

The advantage of time-proportional control compared to phase control is in that the thyristors are conducting during a full half-cycle of the voltage. In this way any abrupt changes of the voltage and current, which arise when the switching is not at voltage zero crossing, are avoided.

The shortcoming of this method is that the energy from the mains is taken in pulses. The average power of the load is controlled by varying the ratio of conduction, T_{on} , and nonconduction, T_{off} , times of thyristors T_{h1} and T_{h2} . Namely

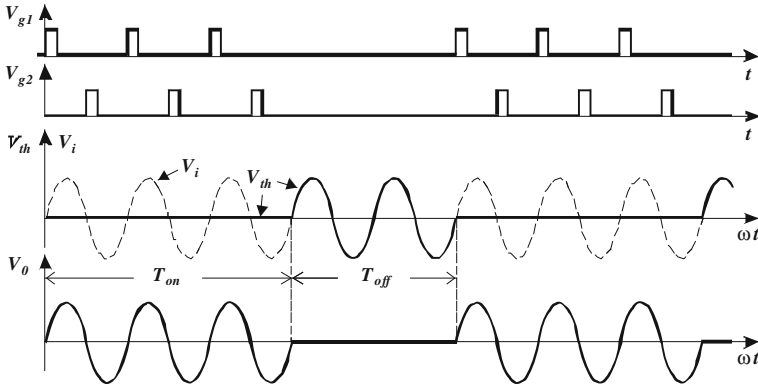


Fig. 8.4 The principle of the time proportional control

$$P_{L,av} = \frac{T_{on}}{T_{on} + T_{off}} P_{LM}, \quad (8.14)$$

where $P_{LM} = V_{s,rms}^2 / R_L$ is the maximum load power without applied control ($T_{off} = 0$). If the interval $T_{on} + T_{off}$ is kept constant, and the conduction time of the thyristors T_{on} is varied, the pulse-width method of control is carried out (Fig. 8.4).

Example 8.3 To the control thyristors in the circuit shown in Fig. 8.1a the TPC technique is applied. If the thyristors are turned on for $m = 25$ periods of input voltage and turned off for $n = 75$ periods determine:

- the rms value of the output voltage,
- the power factor, and
- the average and rms values of the thyristor current.

It is known that $V_{seff} = 220$ V, $f_s = 50$ Hz and $R_L = 10$ Ω .

$$\begin{aligned} (a) \quad V_{0,rms} &= \sqrt{\frac{m}{m+n} \frac{1}{\pi} \int_0^\pi (V_{SM} \sin(\omega t))^2 d(\omega t)} = \frac{V_{SM}}{\sqrt{2}} \sqrt{\frac{m}{m+n}} \\ &= V_{s,rms} \sqrt{\gamma} = 110 \text{ V}, \gamma = \frac{m}{m+n}. \end{aligned}$$

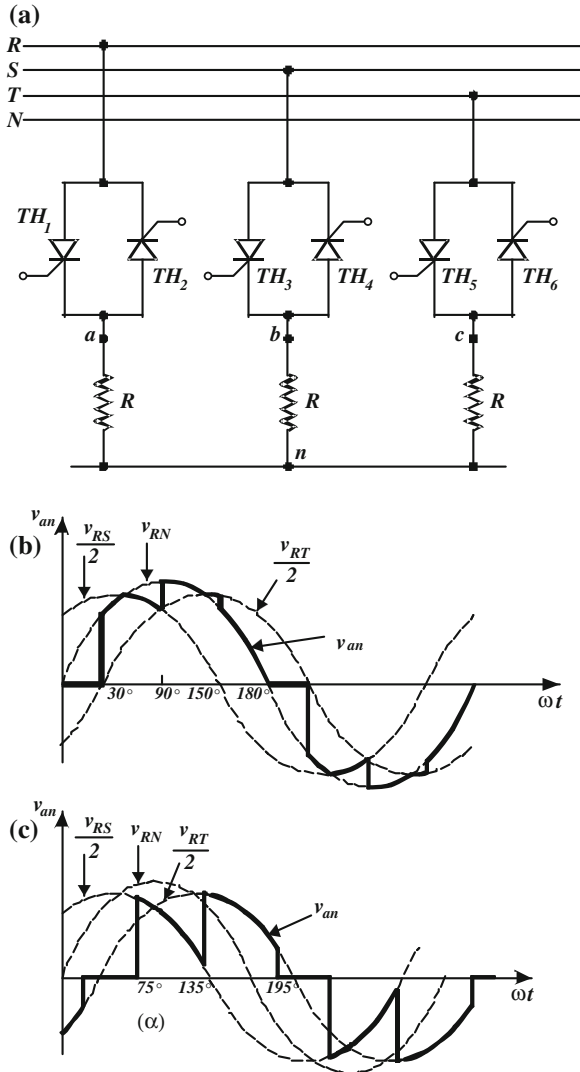
$$\begin{aligned} (b) \quad I_{0,rms} &= \frac{V_{0,rms}}{R} = 11 \text{ A}, \quad P_R = I_{0,rms}^2 R = 121 \times 10 = 1210 \text{ W}, \\ S &= I_{s,rms} V_{s,rms} = I_{0,rms} V_{s,rms} = 2420 \text{ W}, \quad \text{PF} = \frac{P_R}{S} = \sqrt{\gamma} = 0.5. \end{aligned}$$

$$\begin{aligned} (c) \quad I_{Th,av} &= \frac{m}{m+n} \frac{1}{2\pi} \int_0^\pi \frac{V_{SM}}{R} \sin(\omega t) d(\omega t) = 2.47 \text{ A}, \\ I_{Th,rms} &= \frac{I_{0,rms}}{\sqrt{2}} = 7.77 \text{ A}. \end{aligned}$$

8.2 Three-Phase Converters

Three-phase converters may be looked upon as a combination of three single-phase converters. The load can be either in a star (Fig. 8.5a) or in a triangle connection. The currents through the phase loads are controlled by the turn-on angle, α , of each thyristor. The instantaneous value of the voltage of each phase of the load depends upon which of the thyristors are on and that, again, depends on the turn-on angle of the thyristors. If $0 < \alpha < \pi/3$ two or three-phases are always conducting, if $\pi/3 < \alpha <$

Fig. 8.5 A three-phase AC/AC voltage converter having a resistive load Y -connected (a), the load voltage v_{an} for: $\alpha = 30^\circ$ (b) and $\alpha = 75^\circ$ (c)



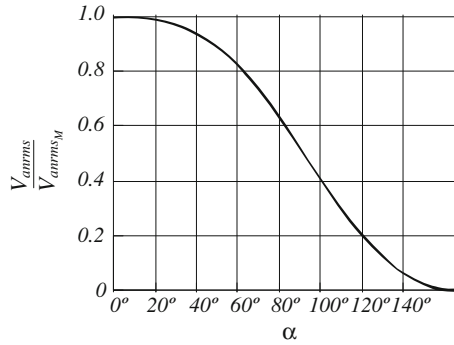


Fig. 8.6 The normalized rms value of the output voltage of a three-phase AC/AC converter having a resistive load as function of the turn-on angle

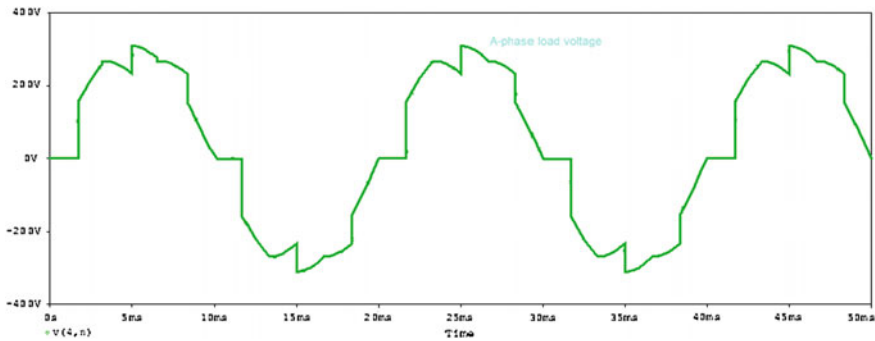


Fig. 8.7 A-phase load voltage for $\alpha = \pi/6$ and for converter shown in Fig. 8.5

$2\pi/3$ one or two phases are always conducting, and if $2\pi/3 < \alpha < \pi$ only one phase can be conducting.

The rms value of the output voltage varies from the maximum value, at $\alpha = 0$, which corresponds to a direct connection between the load and the source, to zero, at $\alpha = 150^\circ$ (Fig. 8.6). For $\alpha > 150^\circ$ there is no interval when any of the thyristors is forward biased while the triggering pulse is applied to the gate. Therefore, the output voltage is zero.

Example 8.4 The three-phase AC/AC converter shown in Fig. 8.5a has a resistive load $R = 20 \, \Omega$. The converter is supplied by three-phase voltage, $380 \, V_{rms}$, 50 Hz.

Draw the waveforms of the voltage at the resistor R (a -phase load) for $\alpha = \pi/6$ and $\alpha = \pi/2$ using PSPICE software package.

See Figs. 8.7 and 8.8.

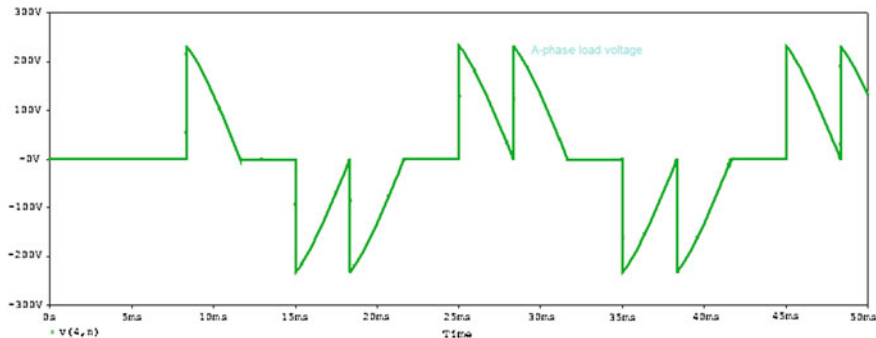


Fig. 8.8 A-phase load voltage for $\alpha = \pi/2$ and for converter shown in Fig. 8.5

8.3 Frequency Converters

The frequency converters can be:

- indirect, and
- direct (cycloconverters).

In the indirect frequency converters the input voltage of frequency f_1 is converted to a DC voltage first and then the DC voltage is converted to an AC voltage with a frequency $f_2 \gg f_1$. Therefore, these converters consist of AC/CD (rectifier) and DC/AC (inverter) converters (Fig. 8.9). C_F is the filter capacitor. The frequency and the rms value of the output voltage are controlled through the control input of the inverter. The frequency f_2 can be controlled over a wide range so that it can be either lower or higher than the source frequency. Any of the inverter types described in Chap. 9 can be used.

The basic shortcoming of the indirect frequency converters is the double energy conversion. This increases the size and reduces the coefficient of efficiency.

8.3.1 Direct Frequency Converters

Indirect frequency converters AC source is directly converted to an AC response whose frequency is, as a rule, lower than the source frequency. The basic block diagram of the simplest converter of this type (Fig. 8.10a) is the same as that of the phase voltage converter using anti-parallel thyristors (Fig. 8.1a). The difference is in the CM, or in the sequence of thyristor triggering.

Here, the CM during n voltage cycles of the source frequency f_1 generates the triggering pulses only for the thyristor T_{h1} , and then through the same number of cycles feeds the triggering pulses to the gate T_{h2} . The AC load voltage consists of $n + 1$ positive and the same number of negative half-cycles of the input voltage.

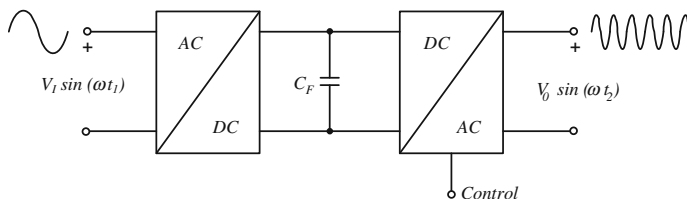


Fig. 8.9 The basic block diagram of an indirect frequency converter

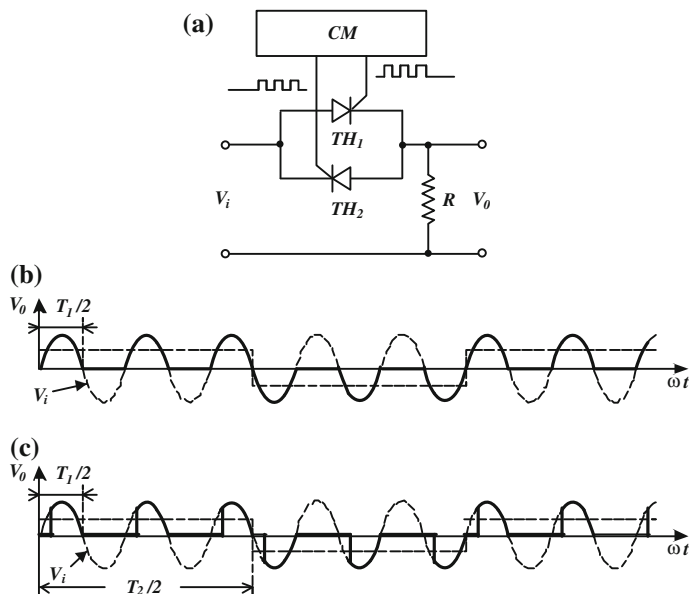


Fig. 8.10 A simple direct frequency converter (a) and output voltage V_0 for thyristor control angles: $\alpha = 0$ (b) and $\alpha > 0$ (c)

The half-cycle of the load voltage is

$$\frac{T_2}{2} = nT_1 + \frac{T_1}{2} = \frac{T_1}{2}(2n + 1), \quad (8.15)$$

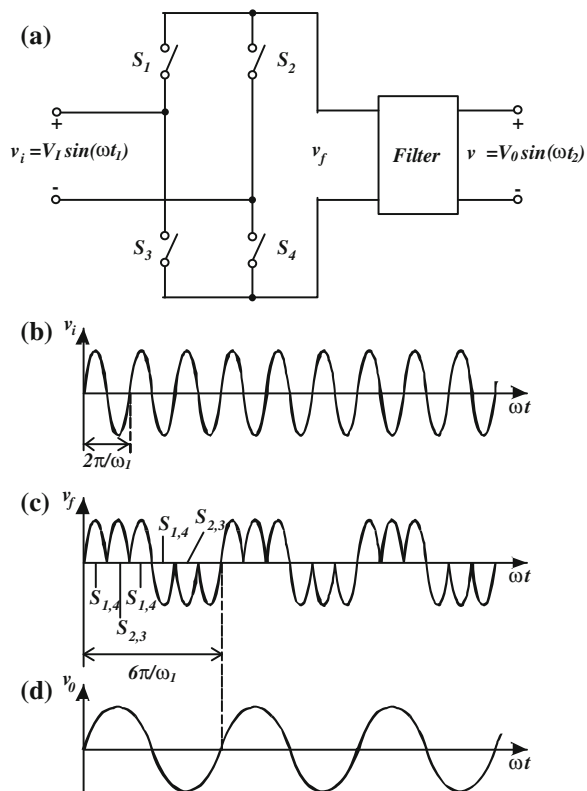
Therefore, it follows that the output voltage frequency is

$$f_2 = \frac{f_1}{2n + 1}. \quad (8.16)$$

The filter at the output eliminates higher harmonics. The rms value of the output voltage is controlled by varying the control angle of the thyristors (Fig. 8.10c).

The simplest direct converter (Fig. 8.10a) is based on the half-wave rectification of the input voltage. However, the use of more complex circuits based on the full-wave rectification (Fig. 8.11a) is more common. The switches S_1 – S_4 are bi-directional. In one half-cycle only the positive full-wave rectification is performed, whereas in the other half-cycle only the negative full-wave rectification is performed (Fig. 8.11b). The voltage at the input of the filter contains three positive half-cycles obtained through the rectification of the input voltage by means of turning on the switches sequentially per half-cycle: (S_1, S_4), (S_2, S_3), and (S_1, S_4). In the other half-cycle three negative half-cycles are generated by the same sequence of turning on the switches, which are now conducting in the opposite direction. The output voltage is the envelope of the voltage at the input of the filter. For this reason these converters are often called the direct envelope frequency converters. The frequency of the output voltage in the presented example (Fig. 8.11) is three times lower than the input voltage frequency. The rms value of the output voltage can be controlled by varying the control angle of the switches (thyristors and triacs).

Fig. 8.11 The basic circuit diagram of a direct envelope frequency converter (a) and voltage waveforms of the: input (b), non-filtered (c), and filtered output voltage (d)



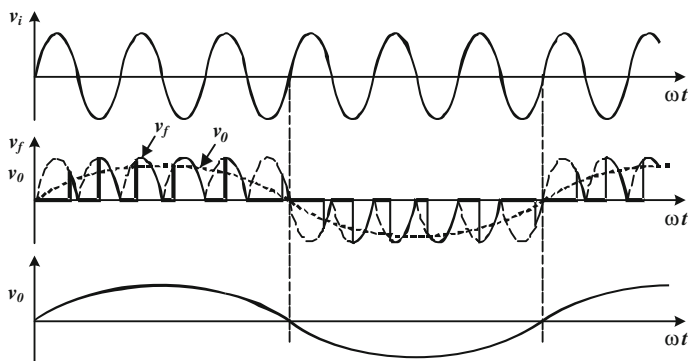


Fig. 8.12 The voltage waveforms of a phase controlled frequency converter

There are two modes of control. In the previously described envelope converter (Fig. 8.11c) the control angle, α , within one cycle is the same for all thyristors. In the second mode the angle of control, within each half-cycle, varies for each pair of thyristors, from a minimum to a maximum and again to the minimum value (Fig. 8.12b). These converters are called the phase controlled frequency converters. The output voltage of these converters is closer to the sine function. Consequently, the filters of the phase converters are simpler and smaller in size than those of the envelope converters. The direct envelope converters of a three-phase voltage of frequency f_1 and the single-phase converters of frequency $f_2 < f_1$ are often called the cycloconverters (Fig. 8.13). Their output voltages are closer to the sine function because the number of pulses within one cycle is higher.

The cycloconverters of Fig. 8.13 have two groups of thyristors. The group A conducts positive and group B conducts negative peaks of the phase voltages (Fig. 8.14).

During the first half-cycle, the cathode group (A) of the thyristors is enabled via the input E_A of the CM. T_{h1} , T_{h2} , T_{h3} and T_{h1} are turned on sequentially. In the next half-cycle the anode group (B) of the thyristors is enabled to conduct the negative peaks of the phase voltages. The number of peaks n of the positive and negative voltages depends on the width of the enable pulses E_A and E_B . The frequency of the load voltage of the three-phase converter is determined by

$$f_2 = \frac{3}{2n+1} f_1. \quad (8.17)$$

The rms value of the output voltage is controlled by the control angle α . Increasing this angle lowers the rms value of the output voltage. The output voltage becomes more irregular and enriched by higher harmonics. In some applications of cycloconverters a need appears for three-phase outputs. This can be accomplished by six-thyristor converters (Fig. 8.15).

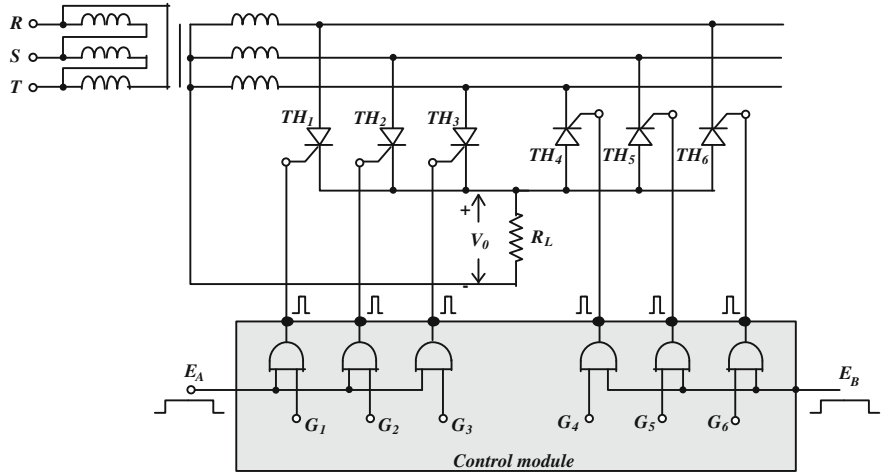
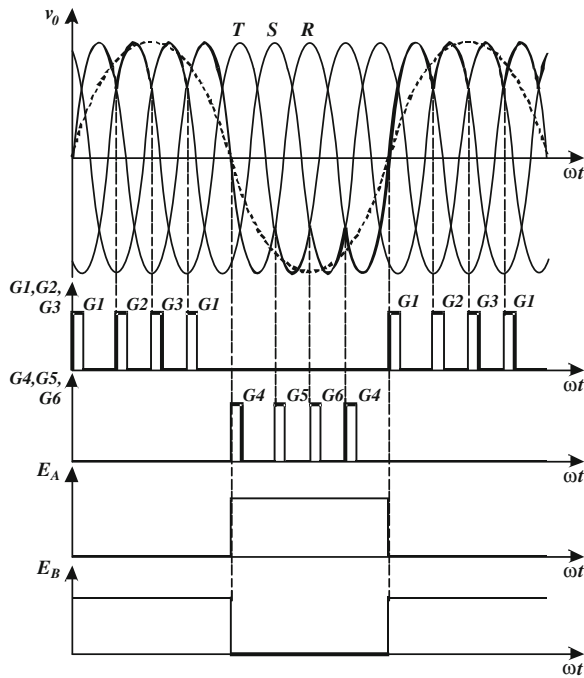


Fig. 8.13 The circuit diagram of a cycloconverter

Fig. 8.14 Load voltage waveforms of a three-phase cycloconverter and control pulses of the thyristor groups for zero control angle



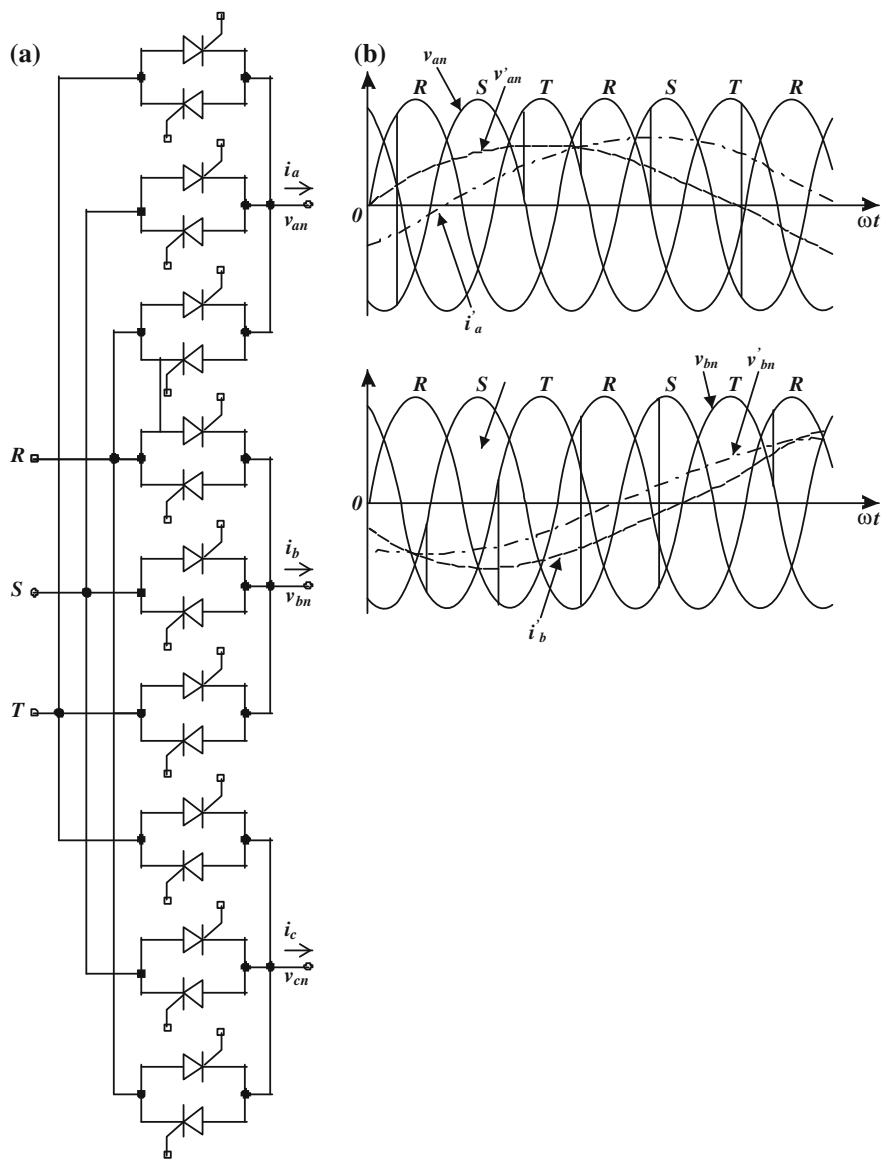


Fig. 8.15 A cycloconverter having a three-phase input and output (a) and the waveforms of the load voltage and current of the phases a and b (b)

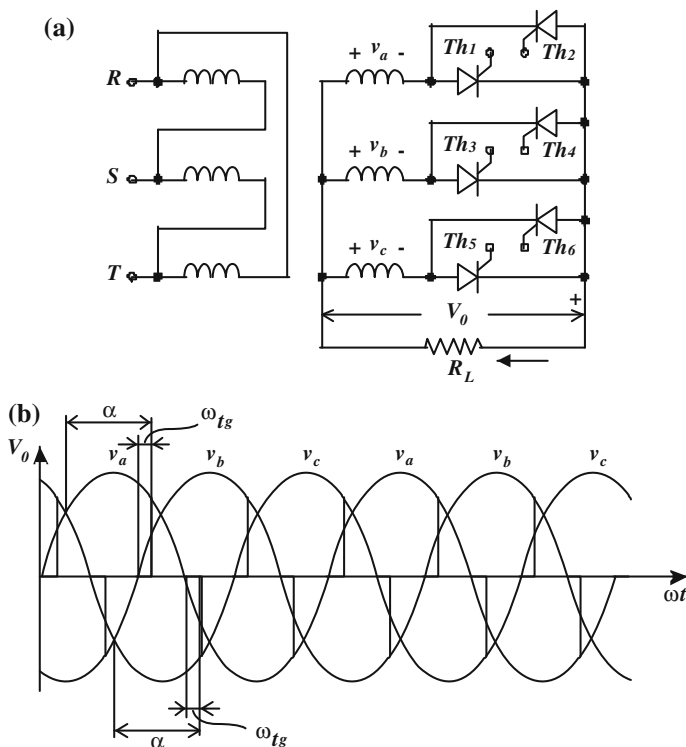


Fig. 8.16 A cycloconverter having enforced commutation (a) and the load voltage waveforms of a purely resistive load (b)

The control of the thyristor groups should be synchronized with the phase voltages. The control angle is equal for all phases. The frequency of the single-phase load voltage of a cycloconverter may be three times higher than that of the three-phase source. The cycle-converters having enforced commutation are used for this purpose (Fig. 8.16). The thyristors are controlled in such a way that during one cycle of the source voltage one part of the positive and one part of the negative half-cycle is transferred to the load (Fig. 8.16b). At any time during this transfer only one thyristor can be on. If the control angle is defined from the instant when the positive/negative voltages of two phases are equal until the instant when the corresponding thyristor is turned on to transfer a part of the positive/negative half-cycle of the third phase, then

$$\frac{\pi}{2} + \omega t_g \leq \alpha \leq \frac{5\pi}{6}, \quad (8.18)$$

where ωt_g is the angle of the reliable turn-off of the thyristor.

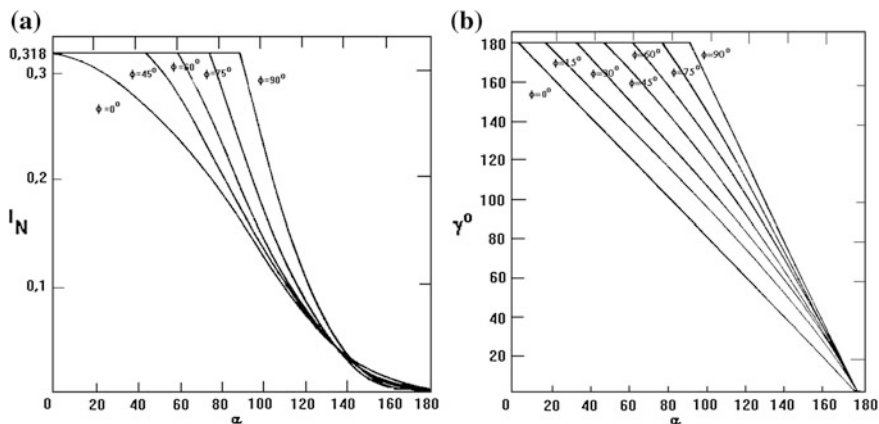


Fig. 8.17 Normalized average value of thyristor current I_N versus thyristor triggering angle α for different angles ϕ (a), relations between the angle of thyristor conduction γ and the angle of triggering α for different values of ϕ (b)

In most cases $\omega t_g \ll \pi/2$ (usually $\omega t_g < 5^\circ$), and α is calculated from the instant of the enforced commutation. The conducting thyristor is turned off at the instant when its current is about to change direction.

Example 8.5 The line-commutated frequency tripler shown in Fig. 8.16a has an R - L load and a frequency of three-phase AC source equal to 50 Hz. The thyristor turn-off time is 100 μ s. Determine the power factor for a Y - Y transformer with a transmission ratio n . The normalized average value of the thyristor current I_N versus thyristor triggering angle α for different angles ϕ and the relations between the angle of thyristor conduction γ and the angle of triggering α for different values of ϕ are shown in Fig. 8.17a, b, respectively.

In a given circuit only one thyristor leads at one moment. The existence of an interval t_q in which two phases are short-circuited across two thyristors with zero current enables proper function of the circuit. In this converter, the input frequency is multiplied with the factor which is a function of the number of the input phases m and an integer (optional). In this case, the output frequency is three times higher than the input. When a much higher output frequency is required, the consequences are a suboptimal input power factor and a lower degree of utilization efficiency of semiconductor components. Each input phase with the associated pair of thyristors can be considered a single-phase AC controller that supplies the load during a part of the period.

The waveforms of the load voltage are shown in Fig. 8.16b. The maximum allowed angle of conduction for thyristors in the tripler from Fig. 8.16a

$$\gamma_{\max} = \pi/3 - \omega_S t_q [\text{rad}], \quad (8.19)$$

where t_q is the thyristor turn-off time. An interval with zero current must exist, so the inequality $t_q \geq t_{\text{off}}$ is satisfied during the each commutation.

The required value for the angle α can be determined from the diagram shown in Fig. 8.17b (using only the subset of curves below the line $\gamma = \gamma_{\text{max}}$). The intersection of the lines and the curve gives an approximate value of the angle ϕ

$$\phi = \arctg \frac{\omega_s L}{R}, \quad (8.20)$$

where ω_s is the frequency of the power source determining the lower limit for the angle α . The upper limit for the angle α is 180° for all types of load.

If I_N is the normalized average value of the thyristor current and I_{RN} is the normalized rms value of the thyristor current, these currents can be read from the diagram (Fig. 8.17a) for any value of the angle α . The rms value of the load current for the tripler shown in Fig. 8.16a is

$$I_{0,\text{rms}} = \sqrt{3} \left(\sqrt{2} I_{RN} I_{\text{BASE}} \right) [A]. \quad (8.21)$$

The base load current is

$$I_{\text{BASE}} = \frac{\sqrt{2}V}{Z} [A] \quad (8.22)$$

and the impedance modulus is

$$Z = [R^2 + \omega_s^2 L^2]^{1/2} [\Omega], \quad (8.23)$$

so the rms value of load current can be expressed as

$$I_{0,\text{rms}} = \frac{2\sqrt{3} I_{RN} V}{Z} [A]. \quad (8.24)$$

The average value of the thyristor current is

$$I_{\text{Th,av}} = I_N \times I_{\text{BASE}} [A]. \quad (8.25)$$

An inverse voltage will appear at the nonconducting thyristor in the pair of thyristors connected in antiparallel. The maximum value of this voltage is

$$V_{AK,\text{PEAK}} = \sqrt{3} \times \sqrt{2} V [V]. \quad (8.26)$$

The current of the transformer secondary winding s supplies the converter, and its rms value is

$$I_2 = V_2 I_{RN} I_{BASE} = \frac{2V}{Z} I_{RN} [A], \quad (8.27)$$

The apparent power at the load is

$$S_2 = 3VI_2 = \frac{6V^2}{Z} I_{RN} [VA]. \quad (8.28)$$

The load current i_0 has a sequence in which it is equal to zero. As consequence, there is no energy transfer between the transformer windings at that time. If the transformer has a Y - Y connection and a turns ratio equal to n , then the rms current of the transformer primary is

$$I_1 = \frac{1}{n} \left[I_2^2 - \left(\frac{I_{0,\text{rms}}}{3} \right)^2 \right]^{1/2} [A]. \quad (8.29)$$

Substituting Eqs. (8.24) and (8.27) in (8.29) it is obtained

$$I_1 = \frac{I_2}{n} \left[1 - \frac{1}{3} \right]^{1/2} = \sqrt{\frac{2}{3}} \frac{I_2}{n} [A]. \quad (8.30)$$

The apparent power of the transformer primary is

$$S_1 = 3nVI_1 = \sqrt{6}VI_2 = \sqrt{\frac{2}{3}}S_2 [VA]. \quad (8.31)$$

The converter output power is

$$P_0 = RI_{0,\text{rms}}^2 = 12 \frac{V^2}{Z^2} I_{RN}^2 R [W]. \quad (8.32)$$

The power factor of the transformer primary is

$$\text{PF} = \frac{P_0}{S_1}. \quad (8.33)$$

Substituting (8.28), (8.31) and (8.32) into (8.33) is obtained

$$\text{PF} = \sqrt{2} I_{RN} \cos \phi \quad (8.34)$$

8.4 Introduction to AC/AC Matrix Converters

8.4.1 Basic Characteristics

Matrix converters can be used for all types of converters in which the primary source is DC or AC. On the other hand, the matrix converter topologies are commonly associated with the direct AC/AC converters. This is the reason why the basic characteristics of these converters will be given for three-phase AC/AC converters. The reason for the interest in matrix converters is that they have several advantages compared to the standard indirect AC/AC converters of the rectifier-inverter type.

These advantages are [1]:

- Sinusoidal waveforms of input and output values with a minimal presence of higher harmonics;
- Bidirectional flow of energy is enabled with full power factor control;
- Requirements for energy storage elements of significant dimensions and a short lifetime, such as capacitors are minimal.

On the other hand, the matrix converters have some drawbacks. These are:

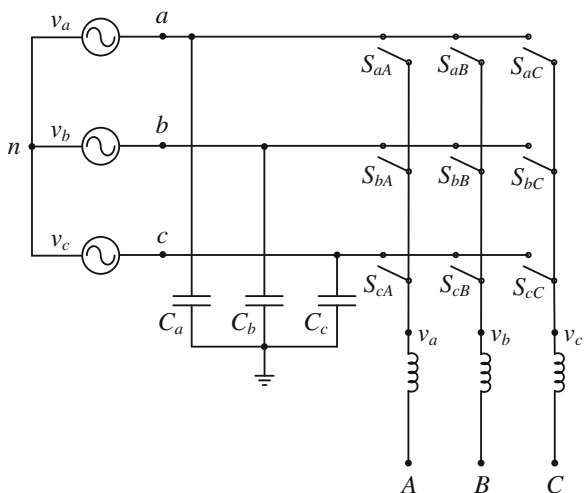
- A larger number of semiconductor components is required for their realization than for the conventional indirect AC/AC converters;
- Monolithic bidirectional switches are not produced, so a combination of unidirectional switches must be used as a bidirectional switch;
- They are sensitive to input voltage disturbances.

A matrix converter with a three-phase voltage input and a three-phase current output is shown in Fig. 8.18. The capacitive filter is on the input side and the inductive filter is on the output side. However, the matrix power converter consists of nine bidirectional switches that allow for any input to be connected with any output. The maximum number of switching states is $2^9 = 512$. The input terminals of the matrix converter shown in Fig. 8.18 must not be short-circuited. Also, the output terminals have inductive character and the output current contour must not be broken. With these limitations the maximum number of the allowed states for a 3×3 matrix converter is limited to 27.

Define a switching function of each switch as

$$S_{ij} = \begin{cases} 1, & \text{switch } S_{ij} \text{ on} \\ 0, & \text{switch } S_{ij} \text{ off} \end{cases} \quad i = \{a, b, c\}, j = \{A, B, C\} \quad (8.35)$$

Fig. 8.18 Three-phase AC/AC matrix converter with voltage inputs and current outputs



The previously described constraints can be presented by the following expression:

$$S_{aj} + S_{bj} + S_{cj} = 1, \quad j = \{A, B, C\} \quad (8.36)$$

Assume that the input and the output voltages are represented by input and output vectors

$$\underline{V}_i = \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix}, \quad \underline{V}_o = \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \quad (8.37)$$

The relationship between the input and the output voltage can be set by the transfer matrix that represents the states of switches in the matrix converter during the observed period.

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} S_{aA}(t) & S_{bA}(t) & S_{cA}(t) \\ S_{aB}(t) & S_{bB}(t) & S_{cB}(t) \\ S_{aC}(t) & S_{bC}(t) & S_{cC}(t) \end{bmatrix} \times \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \quad \underline{V}_o = \underline{S} \underline{V}_i \quad (8.38)$$

A relationship between the input and the output currents in matrix form can be established in a similar way.

$$\underline{I}_i = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}, \quad \underline{I}_o = \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \quad (8.39)$$

$$\underline{I}_i = \underline{S}^T \underline{I}_o$$

S^T is the transpose matrix of the matrix S . Equations (8.38) and (8.39) give relations between the input and the output values and these relationships are used as the basis for a modulation control strategy for the matrix converter. Assuming that the bidirectional switches operate at a much higher frequency than the frequency of the first harmonic, the desired amplitude can be obtained by choosing the duty factors of switches for the applied switching sequence. Let $m_{ij}(t)$ be a duty factor of the switch S_{ij} defined by $m_{ij} = t_{ij}/T$, where $0 < m_{ij} < 1$, $i = \{a, b, c\}$, $j = \{A, B, C\}$. If T is the period of the matrix converter switching sequence, then the low frequency transfer matrix M can be represented in the form

$$M = \begin{bmatrix} m_{aA}(t) & m_{bA}(t) & m_{cA}(t) \\ m_{aB}(t) & m_{bB}(t) & m_{cB}(t) \\ m_{aC}(t) & m_{bC}(t) & m_{cC}(t) \end{bmatrix}. \quad (8.40)$$

Through this matrix the basic relations for the fundamental low-frequency components of the output voltage and the input current are given in the form

$$\begin{aligned} \underline{V_0}(t) &= M \cdot \underline{V_i}(t) \\ \underline{I_i}(t) &= M \cdot \underline{I_0}(t) \end{aligned} \quad (8.41)$$

There are no accumulation elements between the input and the output sides of the matrix converter so the output voltage is generated directly from the input. The duration of each period is controlled so that the average value of the output voltage follows the desired waveform. Therefore, the switching period must be significantly shorter than the fundamental period of the input and the output voltage.

As a result, without going into the overmodulation area ($m_a > 1$) the maximum output voltage is $\frac{\sqrt{3}}{2}$ of the maximum input voltage. In the over modulation it is possible to achieve a higher transfer ratio, but as a consequence there is an increase of harmonic distortion of the output voltage and the input current.

A SPWM-modulated three-phase inverter supplied by the output voltage of a DC bus can have only two values of the output voltage ($+V_{DC}$ or $-V_{DC}$), where $+V_{DC}$ is the voltage of the DC bus. A matrix converter shows the characteristics of a direct AC/AC converter. The output voltage of a matrix converter can have only the value of one input voltage v_a , v_b , or v_c . Depending on which switch is on, one input voltage is passed to the output, and its values are time-variable (Fig. 8.19a). The waveforms of the output voltage v_{AB} and the current i_A are shown in Fig. 8.19. The input voltage is symmetrical three-phase and the rms value of the line to line voltage is 380 V. The load is a symmetric, serial L - R connection with $L = 1$ mH and $R = 2$ Ω .

Higher harmonics of the input current appear around the switching frequency. Their value can be comparable with the fundamental harmonic, and thus it is necessary to use an appropriate filter in order to reduce the input current harmonics. The control of the power factor and low harmonic distortion of the input current from the standpoint of power quality are very attractive characteristics of the matrix converter.

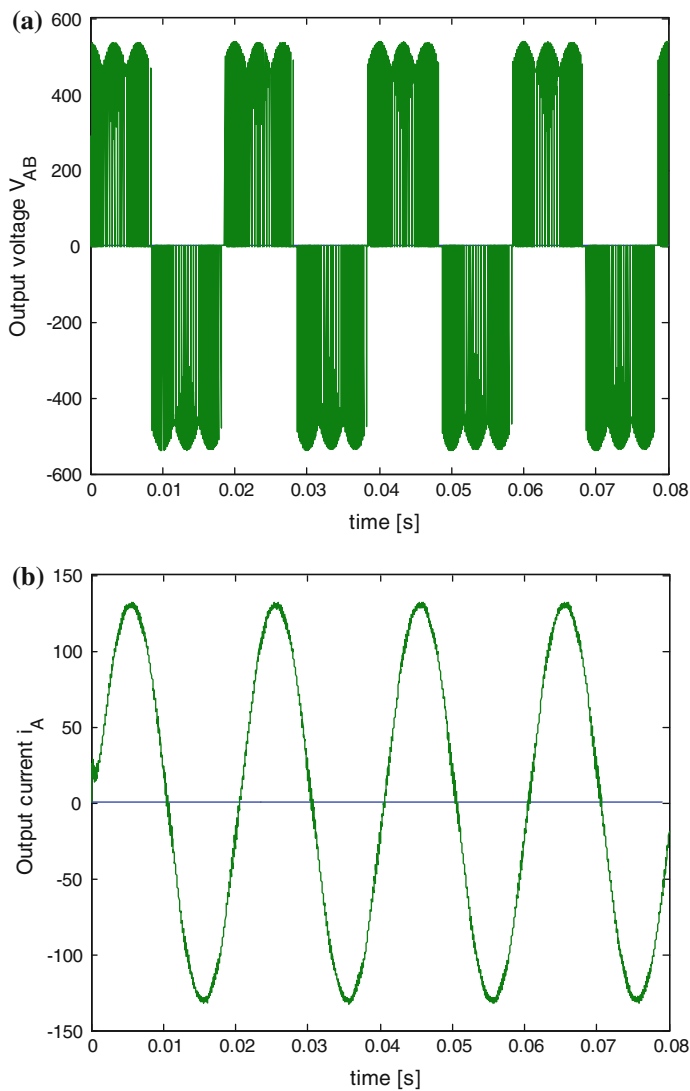


Fig. 8.19 Waveforms of output voltage v_{AB} (a) and output current i_A (b) for a three-phase AC/AC matrix converter

8.4.2 Bidirectional Switches

The matrix converters require the use of bidirectional switches, which can conduct electric current in both directions and have the ability to block a certain voltage. Also, it is necessary to use discrete switches in order to obtain an adequate switching cell. Some realizations of bilateral switches suitable for use in matrix

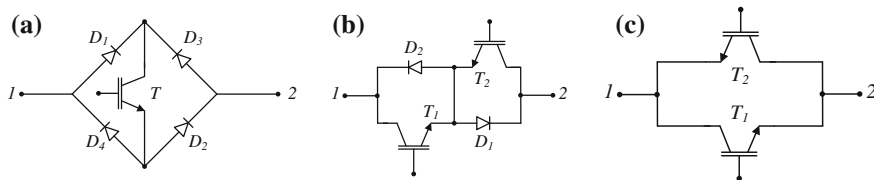


Fig. 8.20 Realization of some bilateral switches suitable for use in matrix converter, with four diodes (a), with two diodes connecting in antiparallel and two IGBT transistors (b), and with two NPT-IGBT transistors connected in antiparallel (c)

converters are shown in Fig. 8.20. A bilateral switch with two diodes connected in antiparallel and two IGBT transistors is shown in Fig. 8.20b. The diodes have a function to increase the switch voltage block capability. The advantage of this configuration compared to the one shown in Fig. 8.20a is in reducing conduction losses. When the switch is turned on, only two switching components conduct. For the current direction from the point 1 to the point 2, the transistor T_1 and the diode D_1 conduct and for the opposite direction of current the transistor T_2 and the diode D_2 conduct. Another advantage of this configuration is in independent control of current direction. The disadvantage is in the need to use mutually isolated electric circuits for gate control of the IGBT transistors T_1 and T_2 .

In the switching topology shown in Fig. 8.20c two NPT-IGBT transistors are connected in antiparallel, which ensures an inverse blocking capability. The basic advantages of this solution are the reduction of the number of semiconductor components and the reduction of conducting losses. One of the important tasks in the control of the matrix converters is to provide a reliable commutation from one bilateral switch to another. So, a special attention must be devoted to synchronization and duration of the control signals led to the switches.

8.4.3 Realization of Input Filter

The input filter is the interface between the matrix converter input and a primary AC source. Its main task is to minimize changes in the matrix converter input voltage and to prevent injection of unwanted current harmonics to the AC source. The existence of current harmonics results in higher voltage distortion, and has effect on the operation of the entire converter.

Several different topologies for matrix converter input filters were proposed (Fig. 8.21). Generally, the design of input filters for matrix converters supplied from the primary AC system must meet the following requirements [1]:

- reduction of noise caused by operation of switches,
- small angular displacement between the filter input voltage and the current, and
- providing the overall system stability.

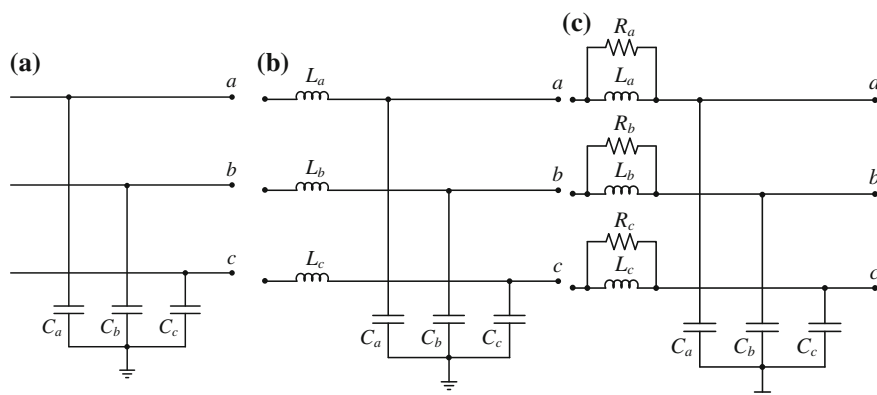


Fig. 8.21 Basic input filter configurations used in matrix converters. (a) capacitive filter, (b) second order L - C filter, (c) L - C filter with damping resistor

A simple capacitive filter is shown in Fig. 8.21. To satisfy the EMI standards related to the attenuation of higher harmonics in the spectrum of output voltage and input current, such filter should have capacitors with a significant capacitance. On the other hand, such a capacitive filter inserts significant phase displacement between the filter input current and the line-to-neutral voltage. These are reasons why the LC filter, shown in Fig. 8.21b, is more commonly used. Such filter can be designed to attenuate the most significant harmonics in the input current (produced by the converter), typically in the range between the first harmonic frequency and the switching frequency. However, due to time asymmetry in control signal propagation, some uncharacteristic and unwanted harmonics, whose value can be significant, may appear. The filter does not attenuate them. For this reason an additional damping resistor is used (Fig. 8.21c).

The design of the input filter of a matrix converter is a complex task, and it can be considered an issue of utmost importance, since it has to satisfy the request to reduce the input current harmonic distortion, to comply to the EMI standards, to fulfill the requirement for a low output impedance, and to achieve an overall system stability.

8.4.4 Current Commutation

A reliable current commutation between the switches in a matrix converter is more complicated for realization than in the case of the indirect AC/AC converter with a DC link between two converter units. Current commutation is essential for the operation of the matrix converter. The commutation process in a matrix converter must be actively controlled all the time, and two basic rules must be met. Two bilateral switches must not be simultaneously connected to the same output

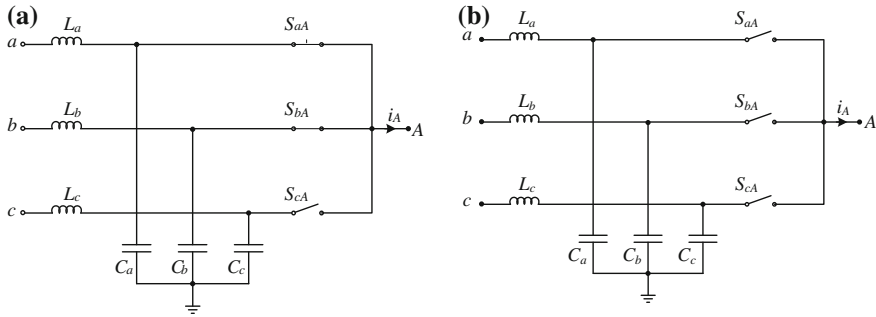


Fig. 8.22 Illegal states, short circuit between two input phases (a) and inductive load current interruption (b)

(Fig. 8.22a). This would cause a short-circuit between the two inputs and the occurrence of significant currents leading to a damage to the converter. Also the inductive load current must not be interrupted, because this would cause appearance of significant overvoltages that can also cause damage to the converter (Fig. 8.22b).

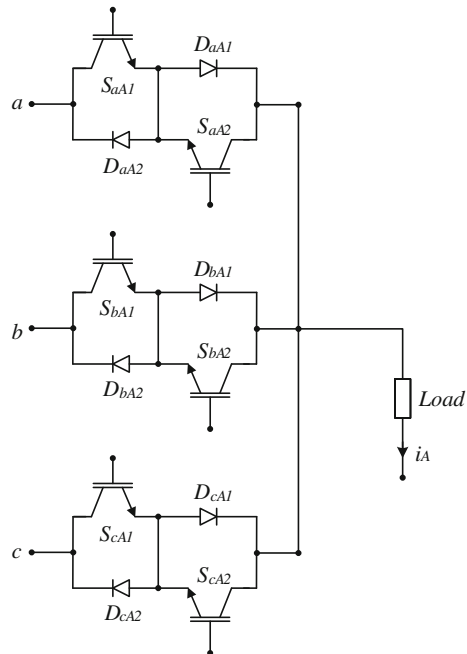
These two requirements are contradictory, because the switches cannot instantly change their state due to the propagation of control signals and the time required for the change of a switch state.

In the simplest form of current commutation the basic rule is intentionally violated. Specifically, one switch (e.g., S_{bA}) is turned on before the switch connected to the same output is turned off (e.g., S_{aA}). This would normally cause a short-circuit of the two phases. However, the existence of the phase inductance will slow down the current increase, and in this way a safe commutation will be realized. This commutation method is not desirable, because the commutation time significantly increases and causes problems related to the switch control. Another possibility is the existence of a dead time so that in a short time interval all switches connected to one output phase are switched off. In this case, the clamping or snubber circuits must be used to provide a continuous current flow.

However, this solution is impractical for several reasons. The realization of snubber circuits for a bilateral switch is more complex and commutation losses are increased.

A more reliable method that meets the previously defined rule uses a four-step commutation strategy [2]. The application of this strategy ensures the control of the current through the switch. The obvious condition is that switches are implemented, thus enabling the control of the current through them. Three switches S_{aA} , S_{bA} , and S_{cA} connected to the output phase A are shown in Fig. 8.23. The current i_A is the load current of the phase A . First, the direction of the current through the switch and the inactive switch unit is determined. For the current direction shown in Fig. 8.23 these are the switch S_{aA} and the switch unit S_{aA2} . In this way, the process of commutation starts when the switches that participate in commutation leave the steady state and move through the transition state until a new steady state is established.

Fig. 8.23 Connection of the one-phase load over bilateral switches to a three-phase input



In the next step (step 2), the switching unit of the next switch is turned on. It is the S_{bA1} switch unit for the switch S_{bA} and the direction of the current is shown in Fig. 8.23. In the third step, the switch unit of the switch S_{aA1} that previously conducted is switched off. A new steady state is established in the fourth step by turning on the second switch unit S_{bA2} of the active switch S_{bA} . The time interval T_{tr} between the two stationary states is determined by the characteristics of the switch. The corresponding time diagrams of the switch units during the commutation process are shown in Fig. 8.24. A high level of the signal corresponds to the on-state of the switch and the low level to the off-state of the switch.

This method allows the current commutation from one switch to another, and there is no occurrence of short circuiting between the two input stages or an interruption of the load current. The advantage of this method is a reduction of switching losses (the use of soft switching techniques), so this method is often called the semi soft current commutation [3].

Also, there is a 2-step switching in which the active switching unit change only at the switch that is active. During the commutation only the active switching units participate. These are the units through which the electric current flows at the beginning and at the end of commutation. A time diagram for the 2-step switching commutation in the case of turning off the switch S_{aA} and turning on the switch S_{bA} and the direction of current i_A as in the Fig. 8.23 is shown in Fig. 8.25.

Resonant techniques are also used in the matrix converter. Beside the reduction of the switching losses as the main advantage of these control techniques, they can

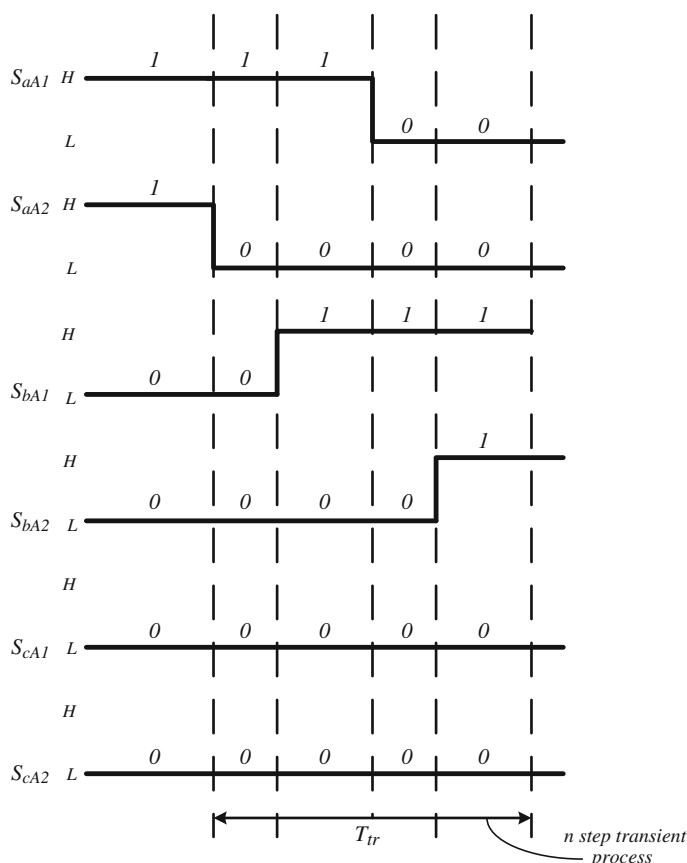


Fig. 8.24 Time diagrams of control signals for 4-step semi-soft current switching commutation between two bilateral switches

be used to solve the problem of current commutation. The problems in the application of the resonant techniques for matrix converters are an increased number of the used components and complex control.

8.4.5 Protection of Matrix Converter

Similarly to the other static converters, the matrix converters must have an adequate protection against overvoltage and overcurrent that can lead to damage of semiconductor components. Overvoltages occur in matrix converters for two primary reasons. One is the appearance of overvoltages at the input lines, and the other is an error or inaccuracy in the control of switches, which can lead to a load current

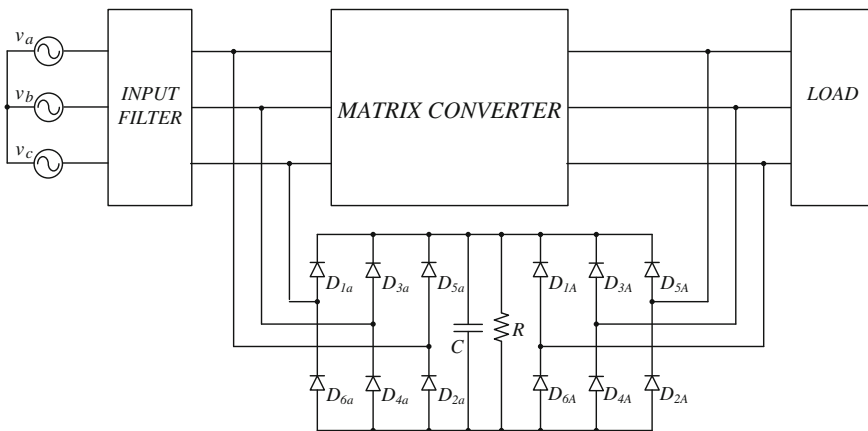


Fig. 8.26 Clamp circuit as common protection for all bilateral switches of matrix converter

8.4.6 Application of Matrix Converter

Because of its good characteristics, as described previously, the matrix converter plays a significant role in some practical applications. The appearance of new types of switches and technologies of their production, as well as of microcontrollers and DSP processors with high processing powers and low cost, decrease the importance of some drawbacks of the matrix converters for practical applications, like the use of bilateral switches, and the need for complex control algorithms. The matrix converters have found the most important use in the controlled AC motor drives. The standard inverter topology, which includes a rectifier, a DC link with a capacitor and an inverter block is shown in Fig. 8.27a. If the diode bridge rectifier, which is not reversible, is used, it is necessary to have a branch with a resistor and a switch for breaking. Also, this rectifier is a significant source of harmonics in the input current, so it is necessary to use the DC reactor (DCL) for the reduction of input current harmonics. Instead of this converter topology it is possible to use only one matrix converter, which is much simpler, cheaper, and allows bidirectional power flow (Fig. 8.27b). This is one reason why the matrix converters are suitable for the use in electric traction vehicles.

The advantages of the matrix converter in comparison to the conventional indirect converter in Fig. 8.27a are:

- bidirectional power flow,
- unity input power factor and the input current shape close to sinusoidal, and
- there is no DC link capacitor block, so the weight and dimensions of the converter are significantly reduced.

One application of a matrix converter in a diesel electric locomotive is shown in Fig. 8.28. The matrix converters MC1 and MC2 are used to power the traction

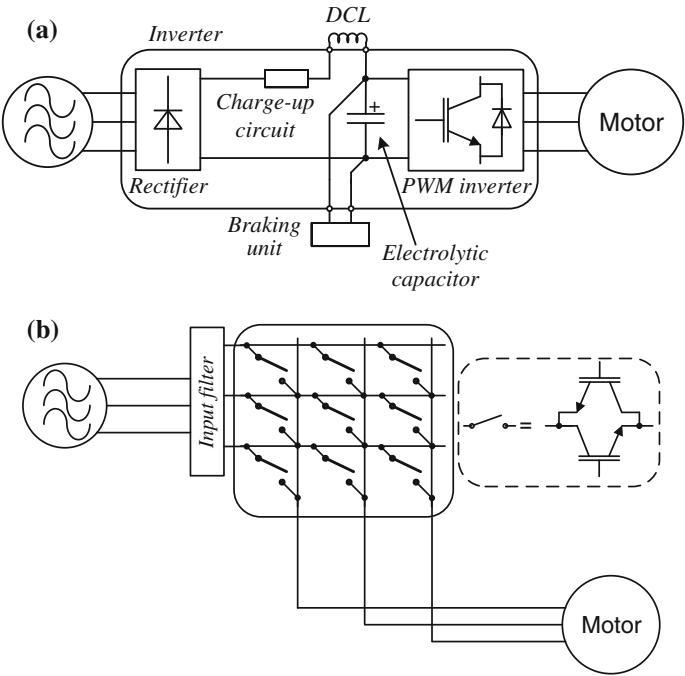


Fig. 8.27 Some topologies of AC/AC converters used in electric drives (a) conventional indirect converter type rectifier-inverter (b) matrix converter

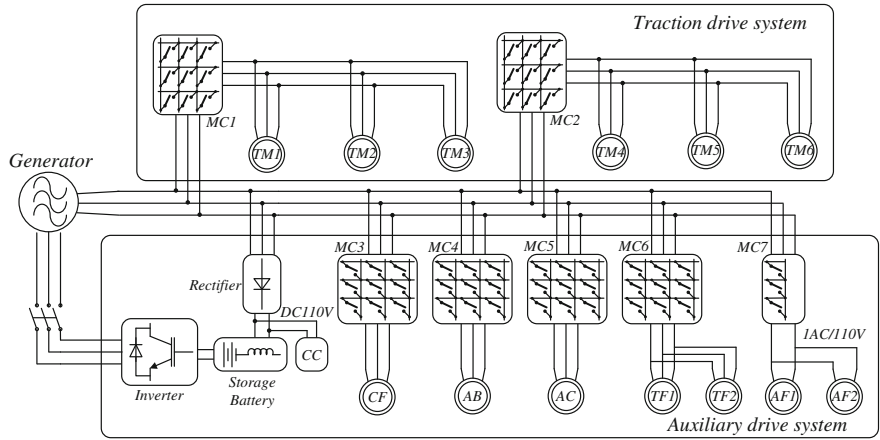


Fig. 8.28 Block diagram of the drive system of a diesel-electric locomotive [4]

motors TM1–TM6, and MC3–MC6 for the auxiliary drive (air conditioning, compressor, cooling of traction motors, etc.). The MC7 converter has a three-phase AC input and is used for obtaining a single-phase AC output voltage with an rms value of 110 V.

Problems

- 8.1 The single-phase AC/AC converter shown in Fig. 8.1a has a $220\text{ V}_{\text{rms}}$, 50 Hz source and load resistance of $25\ \Omega$. The delay angle is 45° . Determine:
 - (a) the rms load voltage,
 - (b) the average and the rms current of the thyristors,
 - (c) the power absorbed by the load, and
 - (d) the power factor.
- 8.2 The single-phase AC/AC converter shown in Fig. 8.1a has a $220\text{ V}_{\text{rms}}$, 50 Hz source. The load is a resistance of $10\ \Omega$. Determine the delay angle of the thyristors so the power delivered to the load is 1 kW.
- 8.3 The single-phase AC/AC converter shown in Fig. 8.3a has a $220\text{ V}_{\text{rms}}$, 50 Hz source. The load consist of a resistance $R = 15\ \Omega$ and an inductance $L = 25\text{ mH}$ connected in series. The delay angle is 45° . Determine:
 - (a) the rms load current, and
 - (b) the power absorbed on the load.
 - (c) Draw the waveforms of the load voltage and the voltage across the thyristors.
- 8.4 The heater of a laser photocopier machine is designed for a nominal voltage of $130\text{ V}_{\text{rms}}$. The supply voltage is $220\text{ V}_{\text{rms}}$, 50 Hz. To obtain the desired voltage, an AC/AC converter with TPC is used. Draw a scheme of the applied inverter. Calculate the number of periods of the input voltage n when the thyristors conduct and the number of periods m when the thyristors are turned off if $T = m + n = 60\text{ ms}$. Calculate the power factor. Is it possible to get a converter output voltage of exactly $130\text{ V}_{\text{rms}}$ at the given conditions?
- 8.5 A three-phase Y -connected AC/AC controller has a $380\text{ V}_{\text{rms}}$, 50 Hz line to line source (Fig. 8.5a). The load in each phase is a resistance of $R = 15\ \Omega$. The delay angle is 90°
 - (a) Draw the waveforms of the voltage at the resistor R (b -phase load).
 - (b) Determine the thyristor voltage stress.
- 8.6 Describe the working principle, i.e., explain how to get the desired frequency and amplitude of the output signal for the cycloconverter shown in Fig. 8.11a. Sketch the waveform of the input and the output voltage for the case when the frequency of the input voltage is 50 Hz and the required output voltage frequency is $16\frac{2}{3}\text{ Hz}$.

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Chapter 9

Resonant Converters

DC/DC converters based on pulse-width modulation (PWM) suffer from two serious drawbacks. In the course of turning on and off of the power switches, very fast voltage dv/dt and current di/dt changes occur. These changes, which may be in excess of 10^8 V/s or A/s, cause the appearance of electromagnetic interference (EMI) which may exceed the permitted level of conductive interference in the power lines. On the other hand, during each change of switch state there is increased power dissipation owing to the simultaneous existence of the voltage across and current through the switch. Typical changes of the current and voltage of a switch are shown in Fig. 9.1a. Due to a reactive character of the load in all topologies of DC/DC converters, the voltage change lags behind the current change or vice versa. Therefore, it could happen that the maximum current through the switch is established in the course of its closing and that the voltage across it is still the same as when it was open. A typical example of this is the MOS transistor switch. Until the voltage across the switch drops to zero the switch will dissipate considerable power. A similar phenomenon occurs during the opening of the switch. All this causes the operating point to move closer to the boundary of the safe operating area (SOA) (Fig. 9.1b). The total power of dissipation in the switch is equal to its mean value within one cycle. If it is assumed that the variations of the current and voltage during transients are linear, then

$$P_d = \frac{1}{T} \int_0^T v i dt \sim I_{ON} V_{OFF} (t_{on} + t_{off}) f, \quad (9.1)$$

where I_{ON} is the current in the closed state, V_{OFF} is the voltage in the open state, t_{on} and t_{off} are the closing and opening times, respectively, and f is the frequency of the switch. Therefore, the power of dissipation is directly proportional to the frequency and the duration of the transient process $t_{on} + t_{off}$. If the frequency is sufficiently high that the cycle is close to $t_{on} + t_{off}$, the dissipation will be excessive ($P_D \approx I_{ON} V_{OFF}$). This not only degrades the coefficient of efficiency but also may cause a catastrophic failure of the switch.

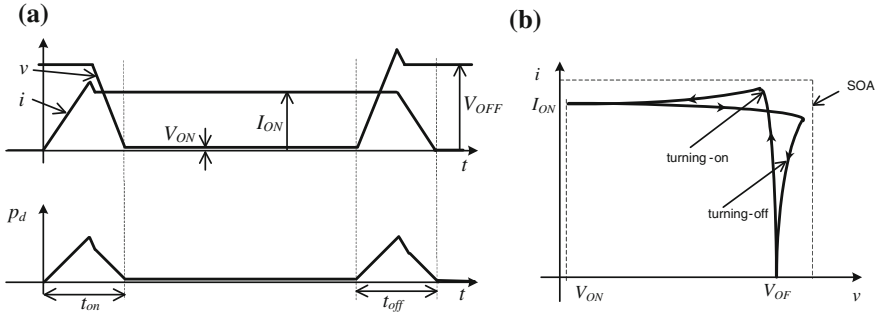


Fig. 9.1 Typical changes during transient processes of the current and voltage in the conventional switching circuits (a) and boundary of the safe operating area (SOA) (b)

Consequently, the limiting factor for increasing the frequency is determined by the dynamic losses in the switches. On the other hand, in order to reduce the dimensions and increase the power density of power converters, it is necessary to increase the frequency because this leads to smaller dimensions of the capacitors and magnetic components.

The answer to the requirement to increase both the frequency and the coefficient of efficiency is sought through the reduction of dynamic power losses. A solution can be accomplished if zero voltage and/or current are provided during commutation, as shown in Fig. 9.2. If either voltage or current is approximately zero during transient, the dynamic losses will be negligible irrespective of the operating frequency of the switch. The trajectory of the operating point (Fig. 9.2b) is close to the coordinate axis away from the SOA boundaries. The values of changes dv/dt and di/dt are considerably smaller and so is the EMI.

The converter topologies providing the above conditions are called the resonant converters, because they use resonant circuits for shaping the forms of voltage and current. If the commutation of a switch occurs at zero voltage across it, then these are the *Zero Voltage Switching (ZVS)* converters and if the commutation is at zero current, then these are the *Zero Current Switching (ZCS)* converters.

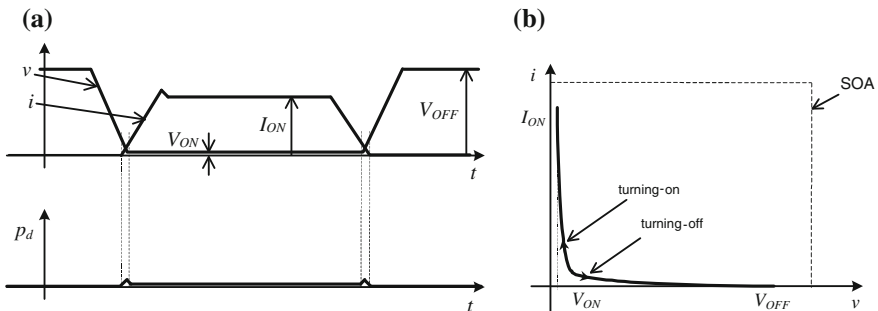


Fig. 9.2 The changes when the switch commutation is at zero voltage and zero current (a) and boundary of the safe operating area (SOA) (b)

Since the voltages and currents of the oscillatory circuits are harmonic, the commutation of switches is synchronous with the voltage and/or current zero crossing. The rises of the currents or voltages of the switch are gradual so the stresses caused by EMI are not generated. For this reason these converters are often called the soft commutation converters.

There are various criteria for the classification of resonant converters. Globally, however, they can be classified in four groups:

- resonant converters of class D,
- resonant converters of class E,
- converters based on resonant switches, and
- PWM soft commutation converters.

9.1 Resonant Circuits

Since resonant circuits are a constituent part of all resonant converters, a brief recapitulation of the basic characteristics of these circuits is due. There are two types of resonant circuits: series and parallel. An unloaded series resonant circuit is shown in Fig. 9.3. The initial conditions at $t = t_0$ are I_{L0} and V_{C0} and are denoted by figures in square brackets.

The state of the circuit can be described by the following equations:

$$L_r \frac{di_L}{dt} + v_C = V_{DC}, \quad (9.2)$$

$$i_L = C_r \frac{dv_C}{dt}. \quad (9.3)$$

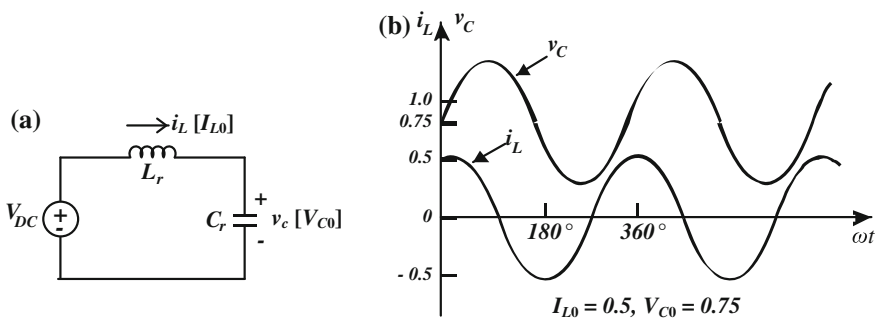


Fig. 9.3 The unloaded series resonant circuit (a) and normalized variations of i_L and V_c (b), with initial conditions $I_{L0} = 0.5$ and $V_{C0} = 0.75$

The solutions of these equations for $t \geq t_0$ are

$$i_L(t) = I_{L0} \cos \omega(t - t_0) + \frac{V_{DC} - V_{C0}}{Z_0} \sin \omega(t - t_0) \quad (9.4)$$

$$v_C(t) = V_{DC} - (V_{DC} - V_{C0}) \cos[\omega_0(t - t_0)] + Z_0 I_{L0} \sin[\omega_0(t - t_0)], \quad (9.5)$$

where

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_r C_r}}, \quad (9.6)$$

is the resonant circular frequency and

$$Z_0 = \sqrt{L_r / C_r} \quad (9.7)$$

is the characteristic impedance. The normalized waveforms of the voltage v_c and the current i_L with respect to V_{DC} and V_{DC}/Z_0 , respectively, are shown in Fig. 9.3b. Let the resonant circuit be loaded by the current generator I_0 in parallel with a capacitor (Fig. 9.4). The current I_0 is constant. By using (9.2) and bearing in mind that now

$$i_L = I_0 + C_r \frac{dv_C}{dt}, \quad (9.8)$$

it turns out that

$$i_L(t) = I_0 + (I_{L0} - I_0) \cos[\omega_0(t - t_0)] + \frac{V_{DC} - V_{C0}}{Z_0} \sin[\omega_0(t - t_0)], \quad (9.9)$$

$$v_C(t) = V_{DC} - (V_{DC} - V_{C0}) \cos[\omega_0(t - t_0)] + Z_0(I_{L0} - I_L) \sin[\omega_0(t - t_0)]. \quad (9.10)$$

In the special case of $V_{C0} = 0$ and $I_{L0} = I_0$

$$i_L(t) = I_0 + \frac{V_{DC}}{Z_0} \sin[\omega_0(t - t_0)], \quad (9.11)$$

$$v_C(t) = V_{DC} - \{1 - \cos[\omega_0(t - t_0)]\}. \quad (9.12)$$

In addition to the characteristic impedance Z_0 and the circular frequency ω_0 , the third essential parameter of an oscillatory circuit is the quality factor

$$Q = \frac{\omega_0 L_r}{R} = \frac{1}{\omega_0 C_r R} = \frac{Z_0}{R}, \quad (9.13)$$

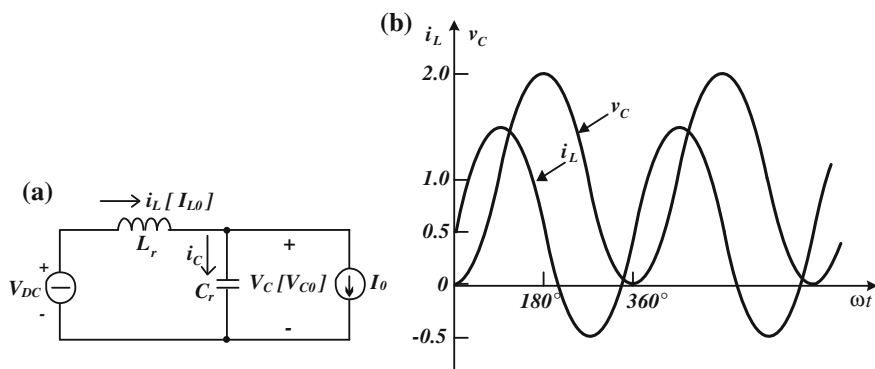


Fig. 9.4 A loaded series resonant circuit (a) and the waveforms for $V_{C0} = 0$ and $I_{L0} = 0.5$ (b)

where R is the series resistance. The frequency characteristic of a series resonant circuit (Fig. 9.5) consists of its impedance and the phase shift between the current and the voltage as a function of frequency. At the resonant frequency the impedance is purely resistive. For high Q factors, the sensitivity of the impedance to frequency variations around ω_0 is very high. It can be considered that to the left of the frequency $\omega_0 - \Delta\omega/2$ the character of the oscillatory circuit can be considered mainly capacitive, and to the right of the frequency $\omega_0 + \Delta\omega/2$ it is mainly inductive.

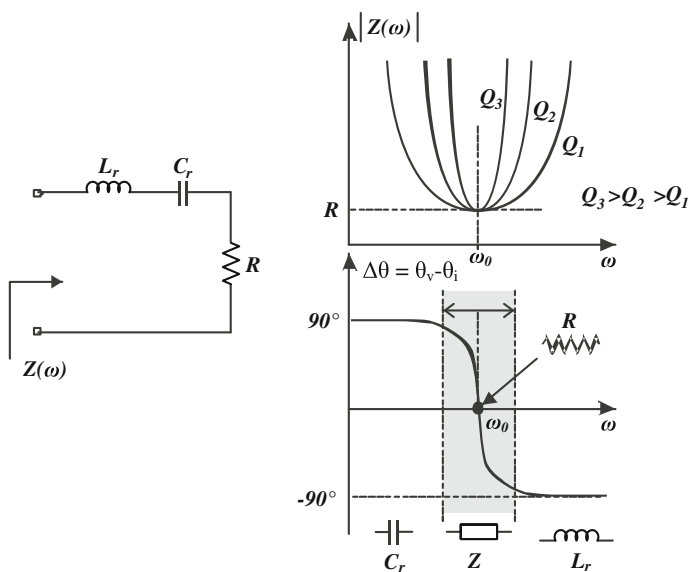


Fig. 9.5 The frequency characteristic of a series resonant circuit

Irrespective of the Q factor, for $\omega < \omega_0$ the capacitive influence is dominant, whereas for $\omega > \omega_0$ the inductive influence prevails.

A parallel oscillatory circuit fed by a constant current I_{DC} is shown in Fig. 9.6. It is straightforward to show that

$$i_L(t) = I_{DC} + (I_{L0} - I_{DC}) \cos[\omega_0(t - t_0)] + \frac{V_{C0}}{Z_0} \sin[\omega_0(t - t_0)], \quad (9.14)$$

$$v_C(t) = Z_0(I_{DC} - I_{L0}) \sin[\omega_0(t - t_0)] + V_{C0}[\cos \omega_0(t - t_0)]. \quad (9.15)$$

If the parallel resistance is R , the Q factor is determined by

$$Q = \omega_0 R C_r = \frac{R}{\omega_0 L_r} = \frac{R}{Z_0}. \quad (9.16)$$

In an ideal case ($R \rightarrow \infty$) the impedance Z_p at a circular frequency ω_0 is infinitely large and it is very sensitive to the variations of ω around ω_0 (Fig. 9.6b). To the left of ω_0 the impedance is mainly inductive, and to the right of ω_0 it is mainly capacitive.

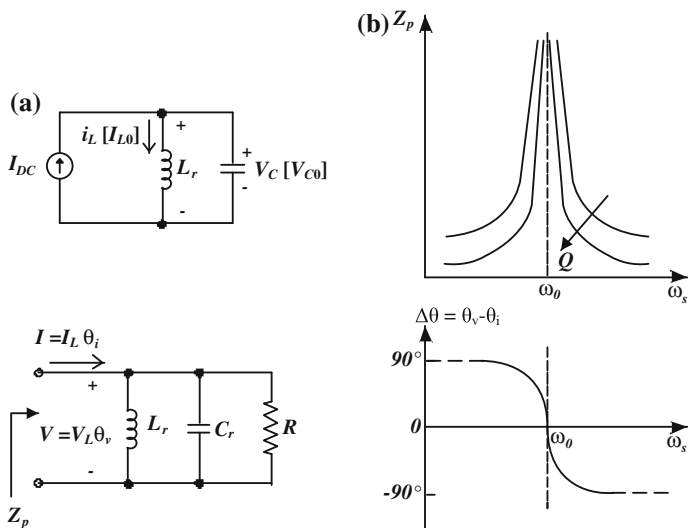


Fig. 9.6 A parallel resonant circuit (a) and its frequency characteristic (b)

9.2 Resonant Converters of Class D

Resonant DC/DC converters of class D consist of a DC/AC converter (inverter), a rectifier, and a filter (Fig. 9.7). The load of the inverter, which may be a half-bridge (Fig. 9.7a) or a full-bridge (Fig. 9.7b) circuit, is a resonant circuit. The advantages and disadvantages of one of these topologies compared to the other has already been explained in Chap. 4. The peculiarity of the half-bridge resonant inverters is that in some connections, like in the series resonant converter, the capacitive divider may carry out the function of the resonant capacitor under the condition that $C_d = C_r/2$. In the other half-bridge connections the capacitors C_d are large and behave like voltage dividers. The resonant circuits are driven by square voltage pulses formed in the process of turning on and off of a transistor. The operating mode of the inverter depends upon the ratio of the operating frequency of the switch and the resonant frequency of the oscillatory circuit. The lowest dynamic losses in transistors are in the discontinuous mode of the current of the resonant coil which arises when $f > f_0$.

The characteristic waveforms of the switch and coil currents are shown in Fig. 9.8. Since the current through the coil lags behind the voltage across it, at the instant the transistor is turned on, its antiparallel diode will conduct. For this reason the transistor is turned on when the voltage across it is zero, thus its dynamic losses are negligible.

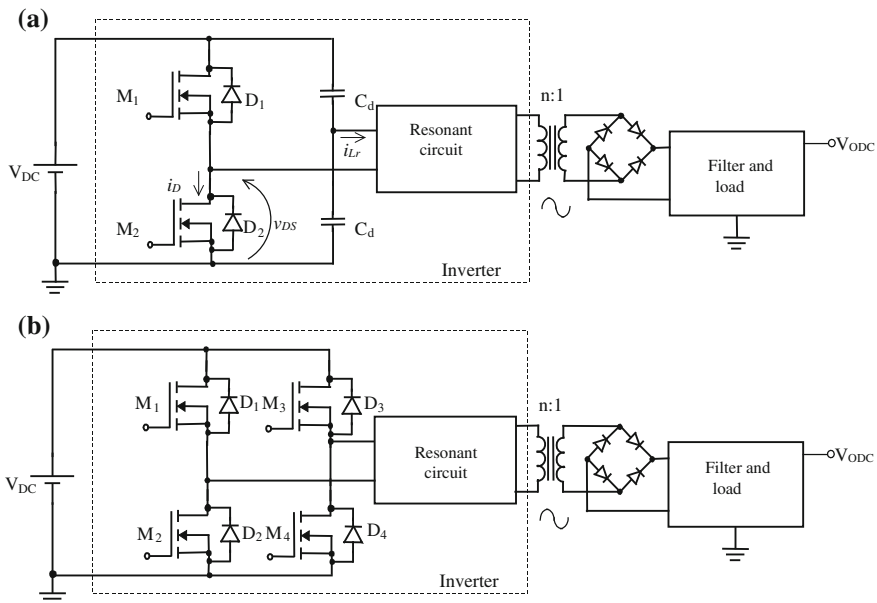
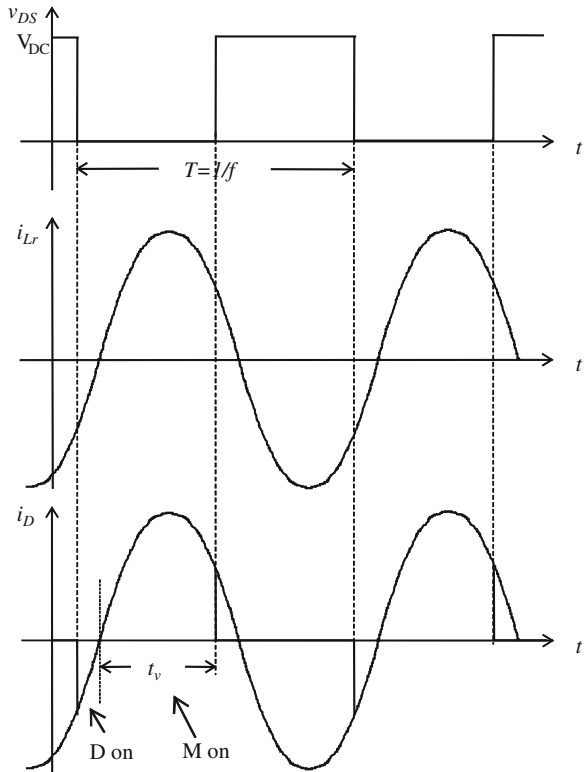


Fig. 9.7 The basic circuit diagram of a DC/DC converter of class D, a half-bridge (a), and a full-bridge (b)

Fig. 9.8 The waveforms at $f < f_0$



If an MOS transistor is used as the switch, the topology of the resonant converter should ensure that it is turned on at zero voltage across it because of the parasitic capacitance between the drain and the source which, for power MOS transistors, is of the order of several hundreds pF if not more. When an MOS transistor is turning on, the voltage across it will exist until the parasitic capacitance is discharged. The current through it $I_D = K_n(V_{GS} - V_m)^2$ is larger than the load current (Fig. 9.9b) and this causes a considerable dissipation by the transistor, approximately

$$P_D = 1/2 C_{DS} (V_{DSOFF} - V_{DSON})^2 f. \quad (9.17)$$

Therefore, it is very important that an MOS transistor is turned on when the voltage across it is zero (very small). Then $V_{DSOFF} = V_{DSON} \approx 0$ and $P_D \approx 0$.

The voltage at the output of the oscillatory circuit is fed to the input of a rectifier via a transformer. The rectified voltage is filtered and one obtains its DC component at the output. Usually, the output voltage of these converters is controlled by varying the switching frequency, i.e., by frequency modulation (FM). If the load or the input voltage variations are large, the required range of the frequency variations is wide. Owing to the frequency dependence of the magnetic elements and the

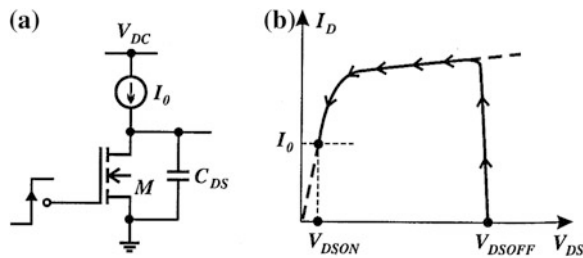


Fig. 9.9 A standard MOS switch (a) and the trajectory of the operating point during the turn-on process of the transistor (b), when the resonant principle is not applied

output filter, the characteristics of the converter may deviate considerably from the designed optimum. On the other hand, for distributed power supplies there is no possibility of synchronization because the loads are different, so the converters operate at different frequencies.

This generates a wide spectrum of interference. In order to avoid this problem, the recent practice is to use control circuitry operating at a constant frequency but with a variable phase shift of the pulses driving the transistors in the bridge. Depending on the position of the load with respect to the elements of the resonant circuit, the converters of class D may be divided in three basic groups:

- series resonant converters,
- parallel resonant converters, and
- series-parallel (hybrid) converters.

9.2.1 Series Resonant Converters

The load of this type of converters is connected in series with the oscillatory circuit. The half-bridge topology without a matching transformer (Fig. 9.10) is considered here. The AC current is rectified by a full-wave rectifier so that the current i_L flows through the load R_L . The capacitor of the output filter is large, so that it may be considered that the output is DC voltage containing negligible high frequency components.

The input capacitors are sufficiently large that they may be considered a voltage source $\pm V_{DC}/2$. Therefore, the voltage between the points A and B varies from $-V_{DC}/2$ to $+V_{DC}/2$. When M_1 is on, then $V_{AB} = +V_{DC}/2$, whereas while M_2 is on $V_{AB} = -V_{DC}/2$. The constant output voltage V_0 is reflected back between the points B and B'. The voltage $V_{BB'}$ is $+V_0$ or $-V_0$ depending on which pair of diodes in the rectifier is conducting. If the series resistance of the resonant circuit is neglected, the equivalent circuit of the converter becomes a simple circuit (Fig. 9.10b). The polarities of the voltage generators V_{AB} and $V_{BB'}$ are dependent on the direction of

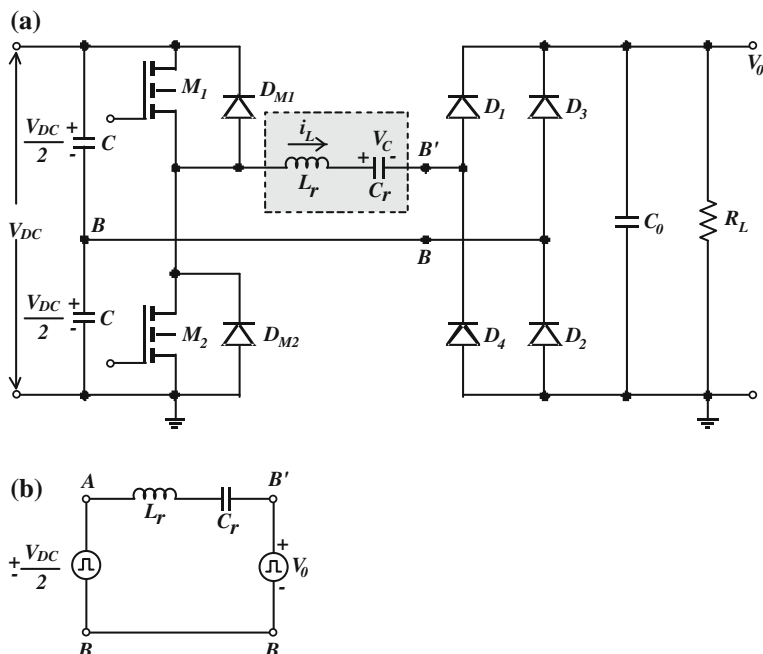


Fig. 9.10 A half-bridge resonant DC/DC converter (a) and its equivalent circuit (b)

the current through the coil. For instance, when the current through the coil is $i_L > 0$, it will then flow through M_1 if it is on and in that case $V_{AB} = V_{DC}/2$. If, however, M_1 is off, the positive current i_L will flow through the diode D_{M2} and then $V_{AB} = -V_{DC}/2$. The situation is similar during the cycle when either M_2 or D_{M1} is on. Therefore, it follows that:

$$i_L > 0 \quad \begin{cases} M_1 \text{ on } V_{AB} = +V_{DC}/2, V_{B'B} = +V_0 \\ D_{M2} \text{ on } V_{AB} = -V_{DC}/2, V_{B'B} = +V_0 \end{cases} \quad (9.18)$$

$$i_L < 0 \quad \begin{cases} M_2 \text{ on } V_{AB} = -V_{DC}/2, V_{B'B} = -V_0 \\ D_{M1} \text{ on } V_{AB} = +V_{DC}/2, V_{B'B} = -V_0 \end{cases} \quad (9.19)$$

The polarity of $V_{B'B}$ is dependent on the direction of the current i_L .

The current i_L may be continuous or discontinuous, so one may speak of the continuous or discontinuous mode of converter operation. The mode of operation is dependent on the ratio of the resonant frequency and the operating frequency of the switches, f .

9.2.1.1 Discontinuous Mode ($\omega < \omega_0/2$)

On the basis of (9.18) and (9.19) and the equivalent circuit of the converter (Fig. 9.10b), the equivalent circuits are drawn within the characteristic time intervals (Fig. 9.11). At the beginning of the cycle, at $\omega_0 t_0$ the transistor M_1 is on and the current i_L starts increasing from zero. The initial voltage across the capacitor is $V_{C0} = -2V_0$.

After the first half cycle of the coil current, at $\omega_0 t_1$, M_1 is turned off and a negative current i_L starts flowing via D_{M1} since M_2 is off. After the current i_L has dropped to zero again at $\omega_0 t_2$, it remains at zero because all transistors and diodes are off. This state remains unchanged until the transistor M_2 is turned on, at $\omega_0 t_3$. The coil current is interrupted over the interval $\omega_0(t_3 - t_2)$ when the voltage across capacitor C_r is constant and amounts $V_{C0} = 2V_0$. Since $V_{C0} < V_{DC}/2 + V_0$, it follows that $V_0 \leq V_{DC}/2$. By turning on the transistor M_2 at $\omega_0 t_3$, the negative current i_L will flow through it. This half cycle is complementary to the previous, but now M_2 is on

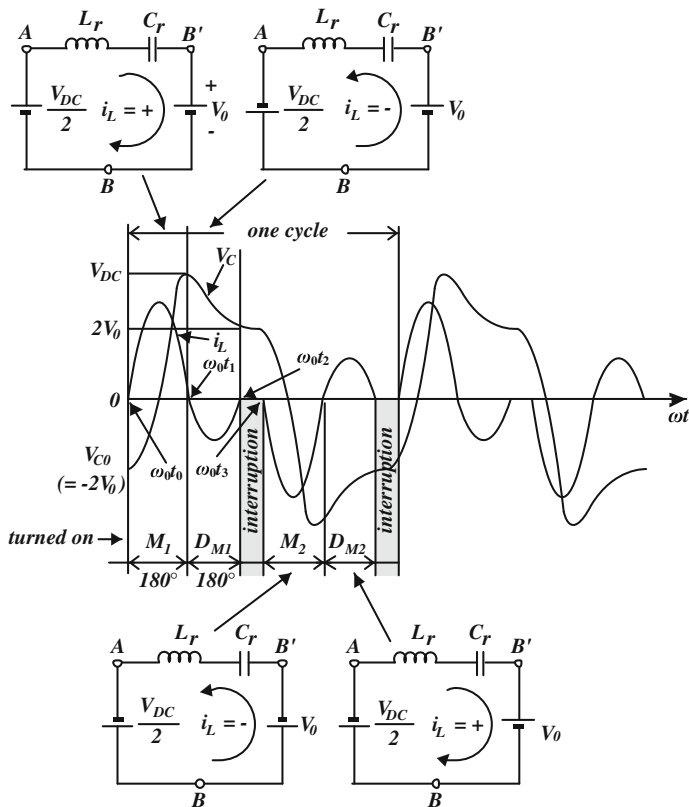


Fig. 9.11 The waveforms and equivalent circuits in the discontinuous mode

first and then D_{M2} is on, the current i_L is negative at first and then becomes positive. It ends by an interval of current discontinuity when all transistors and diodes are off.

In this mode the transistors are turned off at zero current and zero voltage (the antiparallel diode is on), and they are turned on at zero current, but not at zero voltage, which increases the dynamic losses at turn on. For this reason this mode is used in low frequency applications and with thyristors as the switches.

9.2.1.2 Continuous Mode ($\omega_0/2 < \omega < \omega_0$)

The waveforms of the current i_L and the voltage v_c for this mode are shown in Fig. 9.12. The transistor M_1 is turned on at $\omega_0 t_0$. Both the current and the voltage are nonzero which increases the losses at turn on. The transistors are turned off at the current zero crossing (M_1 at $\omega_0 t_1$, M_2 at $\omega_0 t_3$). The diodes do not conduct throughout the half cycle similar to the discontinuous mode. The diode current is taken over by the transistor of the other arm when turned on. For instance, the current of the diode D_{M1} is taken over by the transistor M_2 at $\omega_0 t_2$.

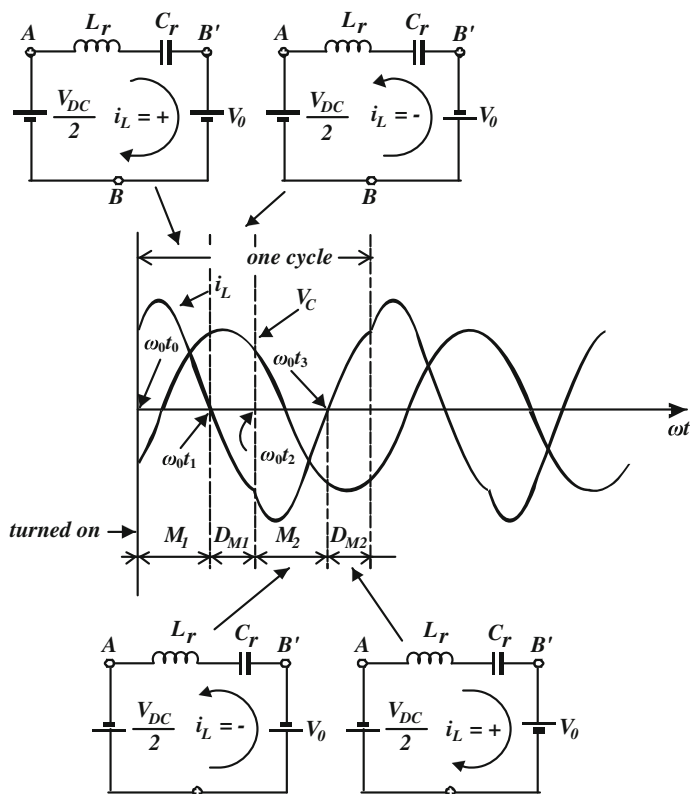


Fig. 9.12 The waveforms of the continuous mode at $\omega_0/2 < \omega < \omega_0$

Because of the presence of the current and voltage at the turn on of transistors, the MOS transistors are not suitable as the switches in this mode. This mode is also used in low frequency applications and with thyristors as the switches.

9.2.1.3 Continuous Mode at $\omega > \omega_0$

In this mode the transistors are turned on at zero current and zero voltage, and they are turned off at nonzero current. The characteristic waveforms are shown in Fig. 9.13. At $\omega_0 t_1$ the transistor M_1 is turned off and its current is taken over by the diode D_{M2} .

Owing to the high voltage across the resonant circuit, which in this interval is $V_{AB} = V_{DC}/2 - V_0$, the diode current quickly reaches the zero crossing, at $\omega_0 t_2$ (Fig. 9.13).

As soon as the diode D_{M2} is turned on, the conduction of the transistor M_2 is enabled so that it takes over the current i_L as soon as it becomes negative. Since the diode D_{M2} is on at the instant of turning on of the transistor M_2 , it is turned on at

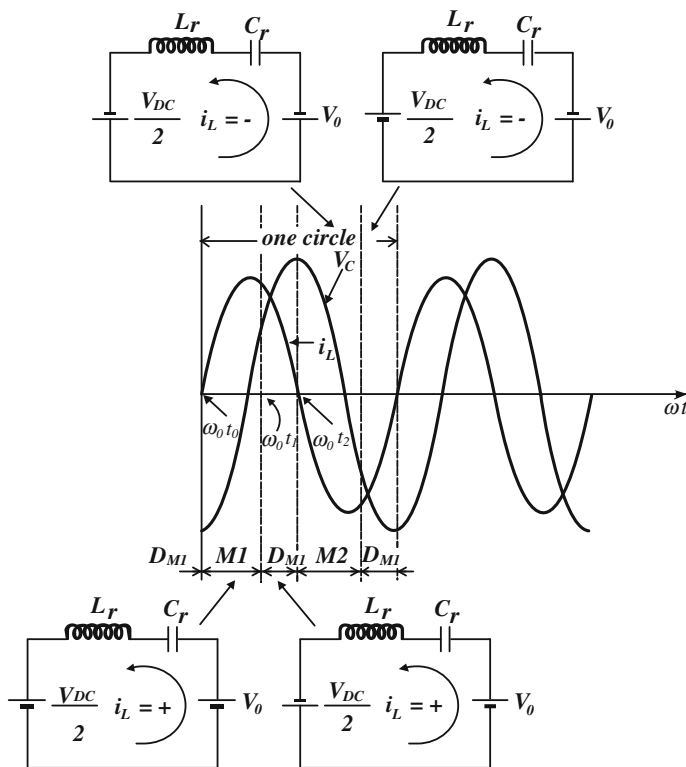


Fig. 9.13 The continuous mode at $\omega > \omega_0$

zero current and zero voltage. Therefore, the turn-on losses are negligible. Since M_2 takes over the negative current, the turn-off time of the diode D_{M2} is not critical. Practically, its turn-off time can be as long as the interval of conduction of M_2 . Therefore, the diodes can be of a medium speed. At the commutation frequencies of the order of several hundred kHz, the function of the antiparallel diodes can be taken over by the internal drain-substrate diodes of the MOS transistors.

In one sense a drawback of the continuous mode at $\omega > \omega_0$ is that the transistors are not turned off at zero current and zero voltage conditions. This drawback is not significant if the switches are MOS transistors because they have the intrinsic capacitance drain–source C_{DS} , which does not allow a fast rise of the voltage V_{DS} . Therefore, C_{DS} behaves as a nondissipative snubber circuit. If the capacitance C_{DS} is small, an external capacitance C_S with a value dependent on the commutation current is connected between the drain and the source (Fig. 9.14).

Series resonant converters with a transformer coupling between the inverter and the rectifier are often used (Fig. 9.14). The use of a transformer allows a better load matching and galvanic separation of the input and the output. By the transformation ratio n one can set the designed ratio of the input and the output voltages. In the series connection with a transformer, the resonant capacitor C_r blocks the DC component of the primary current of the transformer, preventing in this way the premagnetization current and core saturation.

The resonant circuit behaves as a filter which suppresses higher harmonics and passes only the fundamental harmonic. Since it passes only harmonic current, the

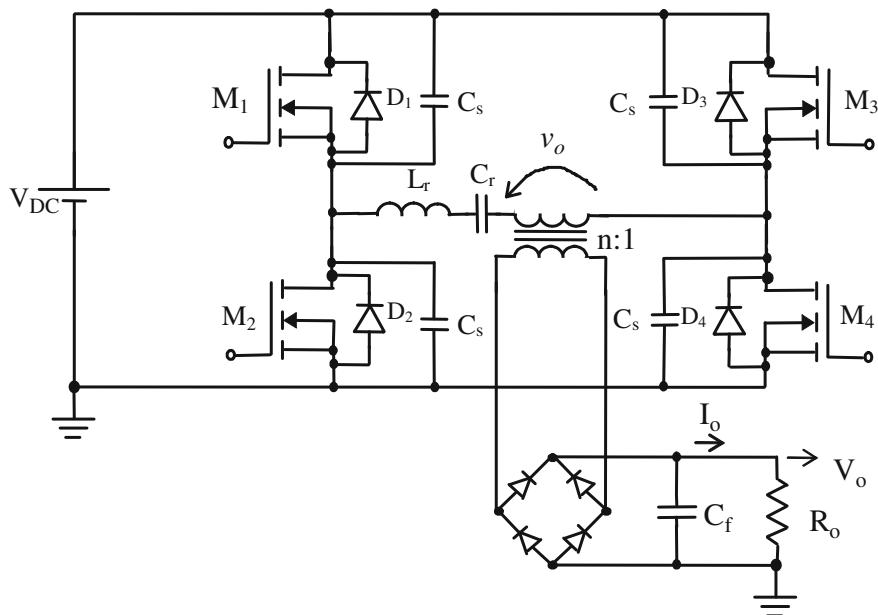


Fig. 9.14 A bridge series resonant DC/DC converter having a transformer coupling and nondissipative snubber capacitors

input voltage can be represented by its fundamental harmonic only. Therefore, the analysis of the resonant converters is well approximated by the circuit analysis methods involving harmonic currents. A realistic equivalent circuit of the converter of Fig. 9.10 is shown in Fig. 9.15a, where R is the equivalent load resistance. Since the input and the output are the sequences of symmetric bipolar square pulses $\pm V_{DC}/2$ and $\pm V_0$, respectively, the amplitudes of the fundamental harmonics are

$$V_{I1M} = \frac{4(V_{DC}/2)}{\pi} = \frac{2V_{DC}}{\pi}, \quad (9.20)$$

$$V_{O1M} = \frac{2V_0}{\pi}. \quad (9.21)$$

The output current is the full-wave rectified current i_L . Its mean value is the output current I_0 . If the current i_L is approximated by a harmonic current of amplitude I_{L1} , the mean value is

$$I_0 = \frac{2I_{L1}}{\pi} \quad (9.22)$$

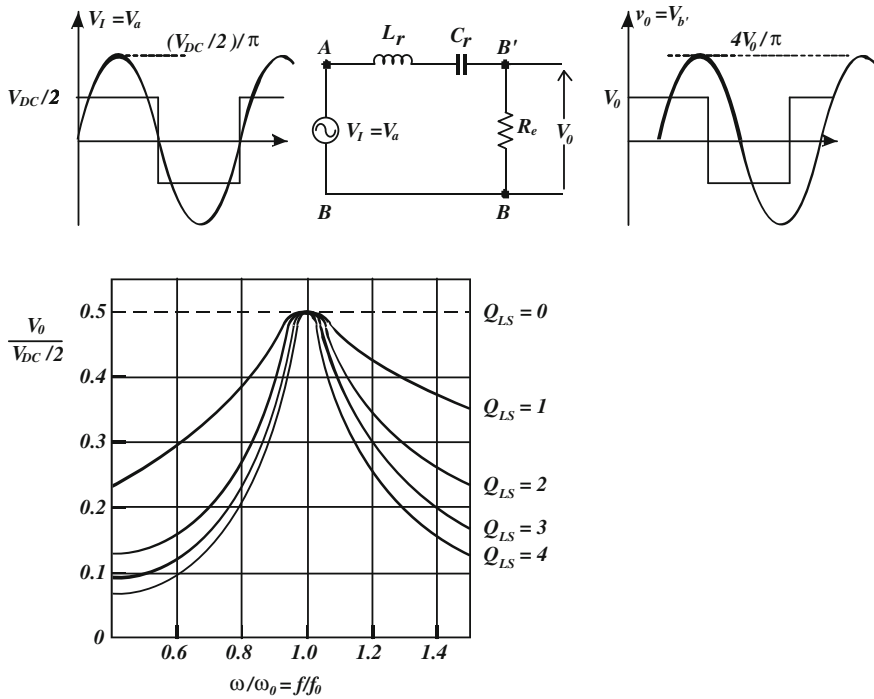


Fig. 9.15 The equivalent circuit of the series resonant converter (a) and its normalized frequency characteristics with Q factor as a parameter (b)

The equivalent output resistance can be expressed as the ratio of the voltage and current at the output of the resonant circuit, i.e.,

$$R_e = \frac{V_{O1M}}{I_{L1}} = \frac{4V_O/\pi}{\pi I_O/2} = \frac{8}{\pi^2} \frac{V_O}{I_O} = \frac{8}{\pi^2} R_L. \quad (9.23)$$

The frequency characteristic of the converter is the ratio of the output and the input voltage as a function of frequency. A simple analysis of the circuit (Fig. 9.15a) shows that

$$V_O = \frac{V_{DC}}{2} \left| \frac{R_e}{R_e + j(X_L - X_C)} \right| = \frac{V_{DC}/2}{\sqrt{1 + \left(\frac{X_L - X_C}{R_e} \right)^2}}, \quad (9.24)$$

$$X_L = \omega L_r, \quad X_C = 1/\omega C_r. \quad (9.25)$$

If the Q factor of the converter is defined with respect to the load R_L , i.e.,

$$Q = \frac{\omega_0 L_r}{R_L} = \frac{1}{\omega_0 C_r R_r}, \quad (9.26)$$

then (9.24) can be written in the form

$$\frac{V_O}{V_{DC}/2} = \frac{1}{\sqrt{1 + (Q_{LS}\pi^2/8)^2[(\omega^2/\omega_0^2) - 1]^2}}. \quad (9.27)$$

Therefore, the frequency characteristic is also dependent on the quality factor, Q_{LS} (Fig. 9.15b). The sensitivity of the characteristic reduces with the reduction of Q_{LS} . In the limiting case of an unloaded converter ($R_L \rightarrow \infty$), the output voltage is independent of frequency and equal to $V_{DC}/2$. Consequently, the output voltage of a loaded series resonant converter is set to the designed value by selecting the commutation frequency of the switches in the range $\omega > \omega_0$.

Example 9.1 Determine the output voltage of the series resonant DC/DC converter of Fig. 9.10, if $V_{DC} = 100$ V, $L_r = 30$ μ H, $C_r = 0.08$ μ F, $R_L = 10$ Ω , and $f = 120$ kHz.

The resonant frequency of the oscillatory circuit is:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{30 \times 10^{-6} \times 0.08 \times 10^{-6}}} = 102.7 \text{ kHz}.$$

The commutation frequency is higher than the resonant frequency, thus the converter operates in the continuous mode at $f > f_0$.

The equivalent resistance of the equivalent circuit is $R_e = (8/\pi^2)R_L = 8.11$ Ω . The Q factor is $Q_{LS} = \omega_0 L_r / R_L = 2\pi \cdot (102.7 \times 10^3) \times (30 \times 10^{-6}) / 10 = 1.94$.

The normalized commutation frequency is $ff_0 = 120 \text{ kHz}/102.7 \text{ kHz} = 1.17$.
On the basis of (9.27), it follows that

$$V_O = \frac{100 \text{ V}/2}{\sqrt{1 + (1.94\pi^2/8)^2(1.17^2 - 1)^2}} = 40.1 \text{ V}.$$

9.2.2 Parallel Resonant Converters

In this type of converters the load is connected in parallel with the resonant capacitor (Fig. 9.16). A transformer coupling is desirable but not mandatory. The inductance of the coil of the output filter L_0 is quite high so, taking into account that the commutation frequency is high, practically only the DC component of the output current can get through. Therefore, it may be considered that the current in the transformer secondary is $\pm I_0$, and its direction is dependent on the conducting pair of diodes in the rectifier. On the side of the primary, this current is $\pm I_0/n$ (Fig. 9.16b), where n is the transformation ratio of the transformer. The voltage V_{AB} at the input of the resonant circuit is $\pm V_{DC}$, and its polarity is dependent on the conducting pair of switches in the inverter bridge. For instance, if M_1 and M_4 are conducting, then $V_{AB} = +V_{DC}$, and if M_2 and M_3 are conducting, then $V_{AB} = -V_{DC}$.

The simplified equivalent circuit of the converter (Fig. 9.16b) may be useful in the analysis of the variations of the current i_L and the voltage V_c of the oscillatory circuit which influence the state of the individual pairs of switches M_i, D_{Mi} ($i = 1, 2, 3, 4$) in the inverter bridge. In this analysis Eqs. (9.9) and (9.10) are used.

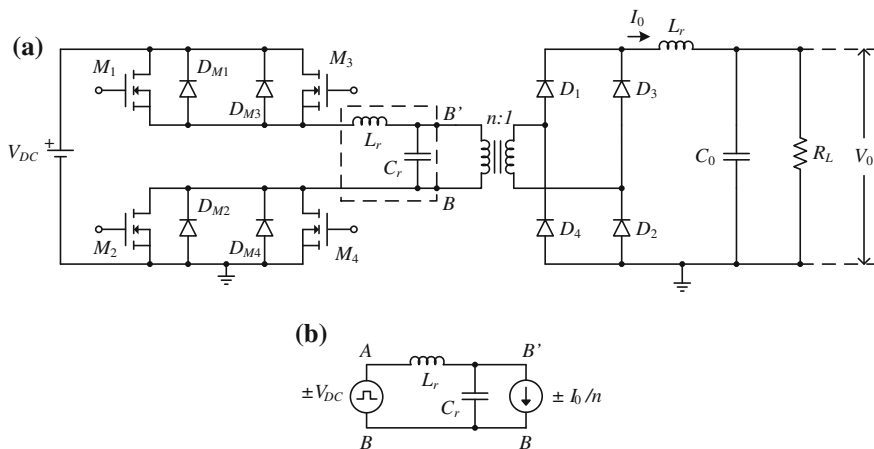


Fig. 9.16 Parallel resonant bridge converter (a), and the simplified equivalent circuit (b)

As in the case of the series resonant converters, several modes of operation are possible. One discontinuous and two continuous modes are characteristic. The discontinuous mode exists at low commutation frequencies approximately up to $\omega_0/2$. Within a certain time interval both the coil current i_L and the voltage across the resonant capacitor V_c are equal to zero. During this period one of the transistor pairs is turned on, thus the turn-on losses are negligible. Turning off occurs at the change of the current direction, or at the current zero crossing.

The output voltage is controlled by controlling the duration of the interval of zero coil current and zero voltage across C_r .

The two continuous modes of operation are different: one is below and the other is above the resonant frequency. In the mode below ω_0 ($\omega_0/2 < \omega < \omega_0$) there are no losses at turning off since the current is zero. However, the transistors are turned on at a nonzero current i_L which is being taken over from the diode of the other arm of the bridge. Therefore, the diode has to be very fast.

The continuous current i_L and voltage V_c will also exist above the resonant frequency ($\omega > \omega_0$). The difference compared to the preceding continuous mode is that now there are no losses at turning on because it happens naturally at the current zero crossing. However, the turning off is forced. The losses during the process of turning off can be reduced considerably by applying a nondissipative protection capacitor in parallel with every switch (as in the series converters Fig. 9.14).

In the analysis of the parallel converter it will be assumed that the voltage across the resonant capacitor is harmonic. The input voltage of the converter and the input current of the diode rectifier will be represented by their first harmonics. The equivalent circuit is shown in Fig. 9.17a. The amplitude of the first harmonic of the output voltage, referred to the primary side of the transformer is

$$V_b = n(\pi V_O/2). \quad (9.28)$$

The primary current is a sequence of symmetric bipolar pulses $\pm I_0$ such that the amplitude of the first harmonic is

$$I_b = 4I_0/(n\pi). \quad (9.29)$$

The equivalent resistance R_L is

$$R_e = \frac{V_b}{I_b} = \frac{n^2\pi^2}{8}R_L, \quad (9.30)$$

where $R_L = V_O/I_0$. Since the amplitude of the fundamental harmonic of the input signal is $V_a = 4V_{DC}/\pi$, from the analysis of the simple circuit of Fig. 9.17a, it follows that

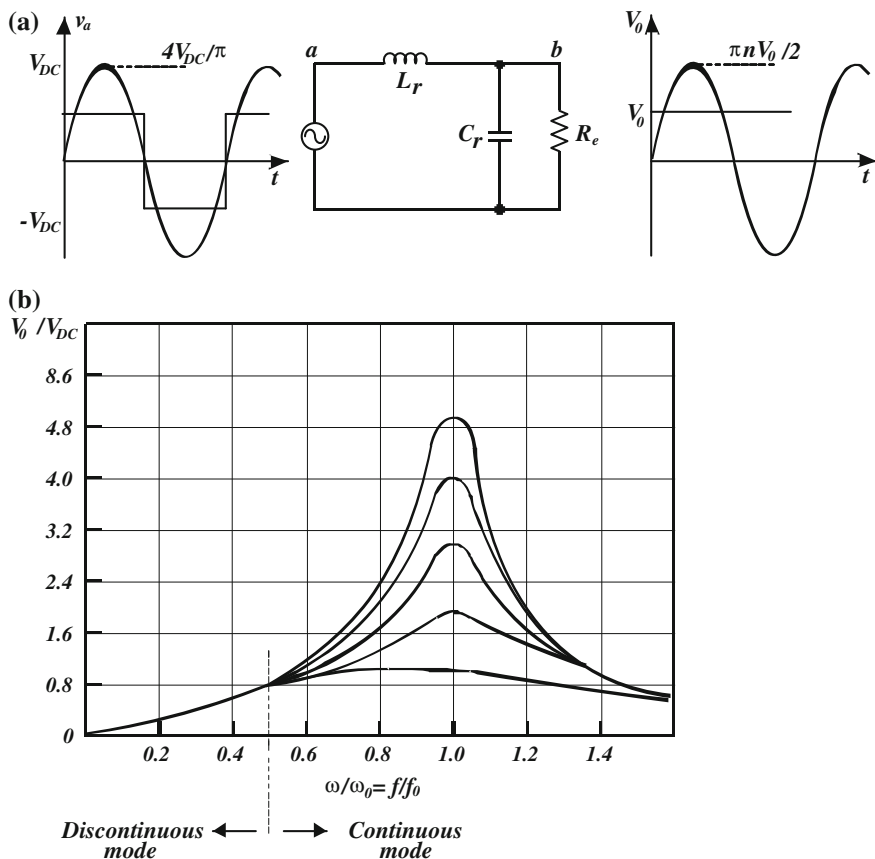


Fig. 9.17 The equivalent AC circuit of a parallel resonant DC/DC converter (a) and its normalized frequency characteristic (b) for $n = 1$

$$V_o = \frac{8V_{DC}}{n^2\pi^2\sqrt{\left(1 - \frac{X_L}{X_C}\right)^2 + \left(\frac{X_L}{R_e}\right)^2}} = \frac{8V_{DC}}{n^2\pi^2\sqrt{\left(1 - \frac{\omega^2}{\omega_0^2}\right)^2 - \left(\frac{8}{n^2\pi^2 Q_{LP}}\right)^2}}, \quad (9.31)$$

where $Q_{LP} = R_L/(\omega_0 L_r)$ is the quality factor and $\omega_0 = 1/\sqrt{L_r C_r}$ is the circular frequency of the oscillatory circuit. The normalized frequency characteristic is shown in Fig. 9.17b.

In the range of the discontinuous mode ($\omega < \omega_0/2$) the output voltage does not depend on the Q factor, which means that it does not depend on the load, and is a linear function of frequency. The converter in this region behaves like an ideal voltage source. In the range of the continuous mode, in addition to the frequency, the output voltage is also load dependent. Its value can be higher or lower than the input voltage V_{DC} which was not the case with the series resonant converters.

Example 9.2 Determine the output voltage of a parallel resonant converter with no transformer coupling, if $V_{DC} = 100$ V, $L_r = 8$ μ H, $C_r = 0.32$ μ F, $R_L = 10$ Ω , and $f = 120$ kHz.

The resonant frequency of the oscillatory circuit is $\omega_0 = 1/\sqrt{L_r C_r} = 625 \times 10^3$ 1/s, and $\omega/\omega_0 = 2\pi \times 120/625 = 1.21$. The Q factor is $Q_{LP} = R_L/(\omega_0 L_r) = 2$.

On the basis of (9.31), it follows that

$$V_0 = \frac{8 \times 100 \text{ V}}{\pi^2 \sqrt{(1 - 1.21^2)^2 + \left(\frac{8}{2\pi\tau}\right)^2}} = 121.4 \text{ V}$$

9.2.3 Series-Parallel Resonant Converter

In this type of resonant converters the capacitor of the oscillatory circuit is split in two parts. One is connected in series with the coil, and the other is in parallel with the load. Therefore, the oscillatory circuit together with the load constitutes a series-parallel combination. This type of converters is often called the hybrid converter.

In the half-bridge connections of the series-parallel resonant converters the capacitors of the capacitive divider are often used as the series capacitors of the oscillatory circuit (Fig. 9.18).

The capacitors C_s and C_p can be of the same value. It can be shown that this is the optimum choice at high load resistances. The analysis procedure is the same as for the previous two types of converters. The equivalent AC circuit is shown in Fig. 9.19a. On the basis of this circuit, one obtains

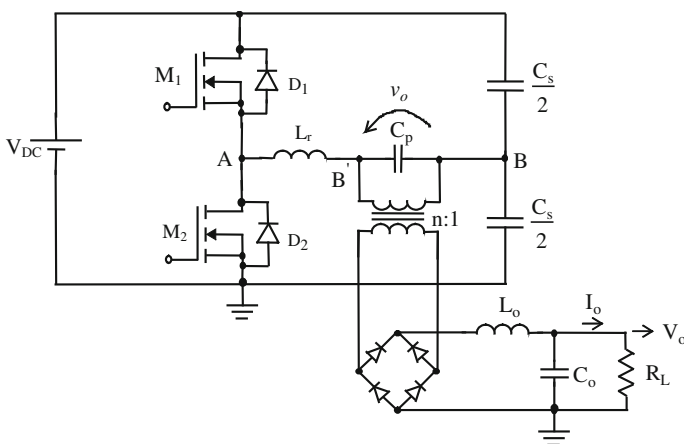


Fig. 9.18 A series-parallel resonant DC/DC converter

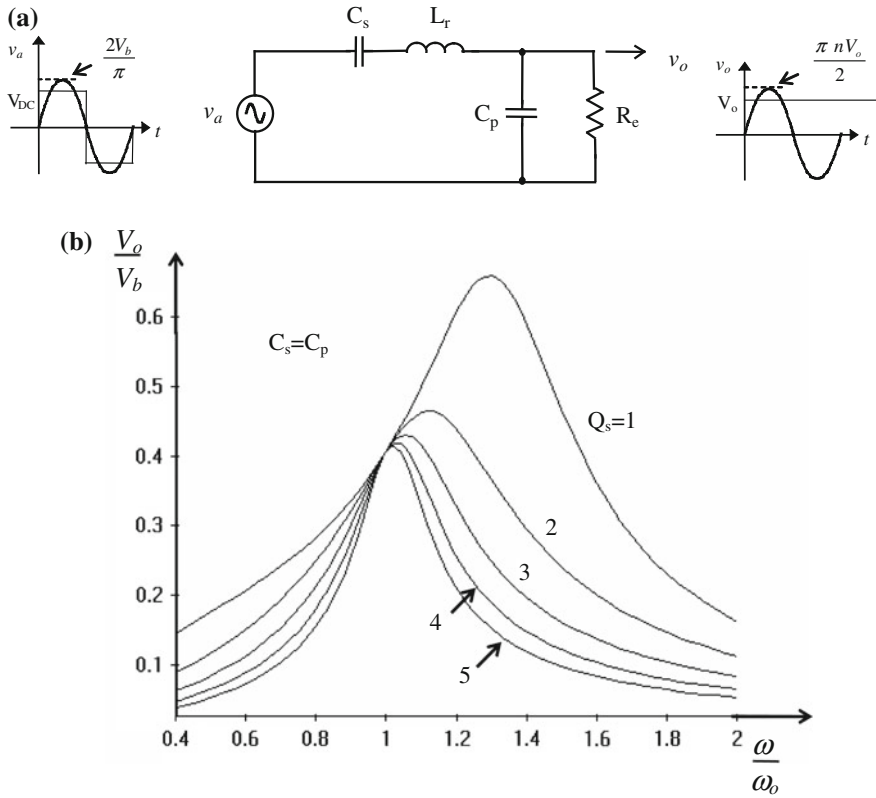


Fig. 9.19 The equivalent circuit of a hybrid resonant converter (a) and its frequency characteristic for $n = 1$ (b)

$$\frac{V_o}{V_{DC}} = \frac{4}{n\pi^2 \sqrt{\left[1 + \frac{C_p}{C_s} \left(1 - \frac{\omega^2}{\omega_0^2}\right)^2 + Q_s^2 \left(\frac{\omega}{\omega_0} + \frac{\omega_0}{\omega}\right)\right]}}, \quad (9.32)$$

where

$$Q = \frac{\omega_0 L_r}{R_e} = \frac{8}{\pi^2 n^2} \frac{\omega_0 L_r}{R_L} = \frac{8}{\pi^2 n^2} Q_{LS}. \quad (9.33)$$

The normalized frequency characteristic, with Q as a parameter, is shown in Fig. 9.19b.

The dependence of the output voltage on frequency exists even for an open output.

By choosing Q_s to be between 4 and 5, high efficiency is retained even at small loads because the current of the oscillatory circuit reduces. The parallel capacitor C_p can be connected at the secondary side of the transformer for the purpose of matching, if it is used. The stray inductance of the transformer is then included in the resonant inductance.

Example 9.3 Determine the output voltage of a series–parallel resonant DC/DC converter from Fig. 9.18, if $V_{DC} = 100$ V, $L_r = 50$ μ H, $C_r = C_p = 0.1$ μ F, $R_L = 10$ Ω , $n = 1.2$, and $f = 75$ kHz.

The resonant frequency of the oscillatory circuit is $\omega_0 = \frac{1}{\sqrt{L_r C_r}} = 447210$ 1/s and $\omega/\omega_0 = 2\pi \cdot f/\omega_0 = 1.0537$.

The Q of the circuit is determined from 9.3

$$Q = \frac{8}{\pi^2 n^2} Q_{LS} = 1.2587.$$

On the basis of (9.32), it follows

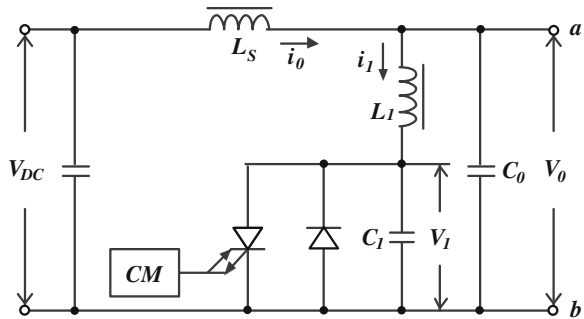
$$V_0 = \frac{4 \times 100 \text{ V}}{1.2 \cdot \pi^2 \sqrt{(1 - 1.0537^2)^2 + 1.2587^2 (1.0537 - 0.949)^2}} = 111 \text{ V}$$

9.3 Series Resonant Converters Based on GTO Thyristors

The elementary connection of a series resonant converter based on the GTO thyristor as a switch is shown in Fig. 9.20. In order to achieve resonance, the inductance L_s should be at least one order of magnitude larger than L_1 and the capacitance C_0 should be at least twice the value of the capacitance C_1 .

The operating mode of the converter is very complex. A complete analysis is possible only with the aid of a computer. For this reason, a brief analysis will be given of an unloaded converter in two limiting cases: short and long intervals of

Fig. 9.20 The basic circuit of a series resonant converter based on GTO thyristors



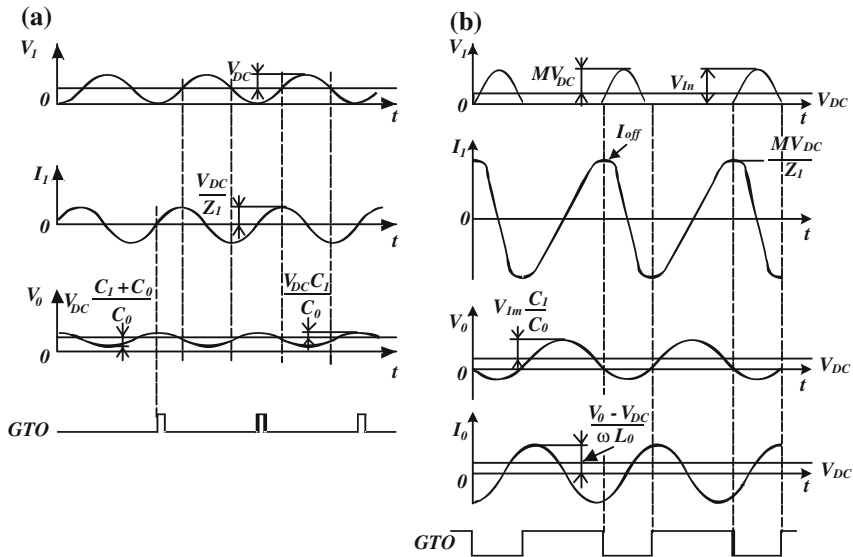


Fig. 9.21 The waveforms of the unloaded converter for short (a) and long conduction of the GTO thyristor (b)

conduction of the GTO thyristor. The analysis is simplified and aims at showing only the qualitative relations in the circuit.

The characteristic wave forms for the case of short conduction of the thyristor are shown in Fig. 9.21a.

While the GTO thyristor is off, current i_1 oscillates around zero at the resonant frequency

$$\omega_0 = \frac{1}{\sqrt{L_1 C_t}}, C_t = \frac{C_1 C_0}{C_1 + C_0} \quad (9.34)$$

The maximum value of this current is determined by

$$I_{1m} = \frac{V_{DC}}{Z_1} = V_{DC} \sqrt{\frac{C_1}{L_1}}, \quad (9.35)$$

and its instantaneous value is

$$i_1(t) = I_{1m} \sin \omega_0 t. \quad (9.36)$$

The existence of the oscillations in the circuit implies that within each cycle the voltage V_1 drops to zero (minimum value). Its instantaneous value is approximately expressed by

$$V_1(t) = V_{DC}(1 - \cos \omega_0 t), \quad (9.37)$$

Therefore, it follows that the maximum value is $V_{1m} = 2V_{DC}$. Thus this voltage oscillates between 0 and $2V_{DC}$, and its mean value is equal to the input voltage, V_{DC} . The maximum value of the output voltage depends on the capacitance ratio C_1/C_0 and it approximately amounts

$$V_{0M} = V_{DC} \left(1 + \frac{C_1}{C_0} \right), \quad (9.38)$$

while its maximum variation is

$$\Delta V_{0M} = V_{0M} - V_{DC} = V_{DC} \frac{C_1}{C_0}. \quad (9.39)$$

The turning on of the GTO thyristor is synchronized with the zero crossing of the current i_1 . Then the capacitor C_1 is very quickly discharged. Since the conduction time is very short and coincides with the minimum of the voltage V_1 , the conduction of the GTO thyristor does not influence the waveforms.

The waveforms in the case of long conduction of the GTO thyristor are shown in Fig. 9.21b. While the GTO thyristor is on, C_1 discharges, so $V_1 = 0$. Now, the maximum of the oscillating current is

$$I_{1M} = M \frac{V_{DC}}{Z_1}, \quad (9.40)$$

where

$$M = \sqrt{\left(\frac{I_{\text{off}} Z_1}{V_{DC}} \right)^2 + 1}, \quad (9.41)$$

and I_{off} is the current through L_1 due to the current I_0 . The maximum value of the voltage across C_1 is determined by

$$V_{1M} = V_{DC}(1 + M), \quad (9.42)$$

and the corresponding variation is

$$\Delta V_{1M} = MV_s. \quad (9.43)$$

It follows from (9.42) that the maximum multiplication factor is

$$M_{\text{max}} = \frac{V_{TM}}{V_{DC}} - 1, \quad (9.44)$$

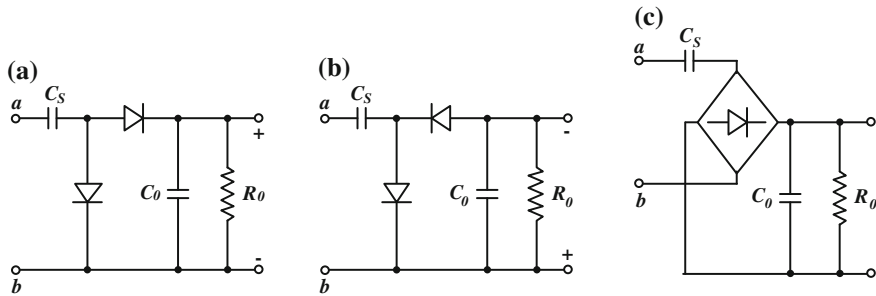


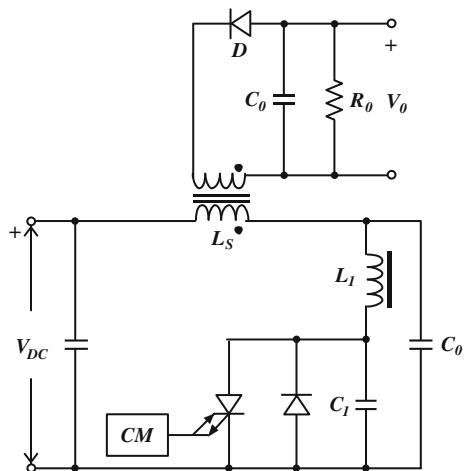
Fig. 9.22 The circuits for rectifying the AC voltage (a, b and c)

where $V_{TM} = V_{1M}$ is the maximum permitted voltage across the thyristor. For instance, if $V_{DC} = 300$ V, $V_{TM} = 1,200$ V, then $M_{\max} = 3$. This means that the maximum value of the current through L_1 has grown three times when the conduction interval of the GTO thyristor was increased to the maximum permitted value as determined by the maximum voltage across the GTO thyristor.

As already shown (Fig. 9.21) the output voltage of an unloaded converter is harmonic. In order to obtain a DC voltage across the load this voltage should be rectified. For this purpose one can use the standard techniques of half-wave or full-wave rectifiers. Three such circuits are shown in Fig. 9.22. Depending on the directions of the diodes, the output voltage can be positive (Fig. 9.22a) or negative (Fig. 9.22b).

It is, however, often required to realize galvanic separation of the load. This may be accomplished by a separation transformer whose primary is the choke L_s (Fig. 9.23). With the opposite direction of winding of the secondary, one would obtain an indirect series resonant converter.

Fig. 9.23 A direct series resonant converter containing a separation transformer



9.4 Class E Resonant Converters

The basic circuit is the class E resonant inverter (Fig. 9.24). It consists of a switch, a parallel capacitor C_1 , a series resonant circuit L_r , C_r , an input choke L_f , and an output load R_L . Instead of an MOS transistor, the switch may be a bipolar transistor or a thyristor. By turning the switch on and off, the oscillation conditions are created for the oscillatory circuit which results in an almost harmonic current through the load. In addition to the very simple topology, the efficiency of this inverter is very high, up to 96 %. Therefore, it is correct to say that the inverter in Fig. 9.24 is among the most efficient inverters developed so far.

The inductance of the input choke should be sufficiently high so that the variations of the current through it are negligible. In that case the input with V_{DC} and L_f can be considered a current source I_{DC} . While the resonant circuit $L_r C_r$ gives a harmonic current through the load, the capacitor C_1 provides optimum conditions for the change of state of the switch from the point of view of the minimum dynamic losses.

A class E resonant inverter operates at a frequency somewhat higher than the resonant frequency $\omega_0 = 1/\sqrt{L_r C_r}$. When the transistor is on, it makes a short circuit for capacitor C_1 (Fig. 9.25b), so $V_{DS} = 0$ and $i_{DS} = i_D - i_0$. Since C_1 is discharged, zero voltage conditions for turning off of the transistor are ensured. Until the current through the transistor drops to zero, the variation of the voltage across C_1 is small and the dynamic losses during the turn off are negligible.

The equivalent circuit of the converter while the transistor is off is shown in Fig. 9.25c. The current through capacitor C_1 is

$$i_{C1} = I_{DC} + i_0 = C_1 \frac{dV_{DS}}{dt}. \quad (9.45)$$

At the instant the transistor is turned on, it takes over the current of the capacitor C_1 . Consequently, the zero voltage and zero current conditions during the turn on are obtained if

$$V_{DS}(t_0) = 0 \quad (9.46)$$

$$dV_{DS}/dt|_{t_0} = dV_{C1}/dt|_{t_0}, \quad (9.47)$$

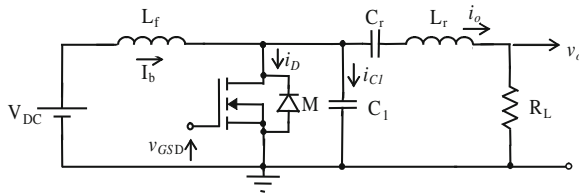


Fig. 9.24 The basic circuit of the class E inverters

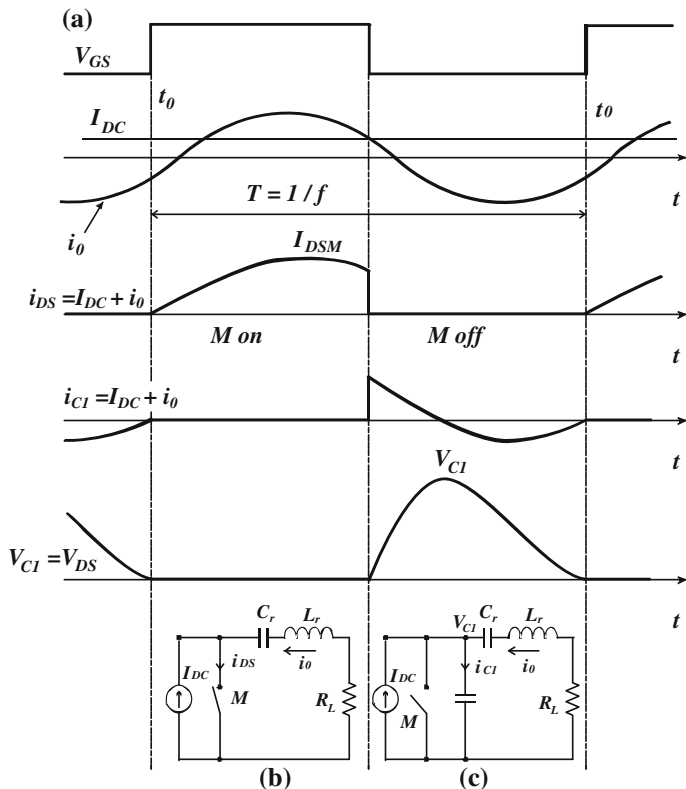


Fig. 9.25 The waveform of the class E inverter at the optimum operating conditions (a) and the equivalent circuits when the transistor is on (b) and when it is off (c)

because at $dv/dt = 0$ the current through C_1 is equal to zero. The beginning of the cycle of conduction of the transistor M is denoted by t_0 . Equations (9.46) and (9.47) are the conditions for the optimum operation of the class E inverters when the dynamic losses are negligible. The optimum conditions, at the duty cycle of the pulses controlling the transistor $D = 0.5$, may be expressed in the following way

$$R_L = \frac{8}{4 + \pi^2} \frac{V_{DC}^2}{P_O} \approx 0.5768 \frac{V_{DC}^2}{P_O}, \quad (9.48)$$

$$C_1 = \frac{8}{\pi(4 + \pi^2)R_L\omega} \approx \frac{0.1836}{R_L\omega}, \quad (9.49)$$

$$L_r = Q R_L / \omega, \quad (9.50)$$

$$C_r = \frac{1}{\left(Q - \frac{\pi(\pi^2-4)}{16}\right)R_L\omega} \approx \frac{1}{(Q - 1.1525)R_L\omega}, \quad (9.51)$$

where P_0 is the input power and Q is the quality factor of the resonant circuit L_r , C_r , and R_L . The minimum inductance of the choke, which ensures that the ripple of the input current is below 10 %, when the above conditions are still valid, is

$$L_{f\min} = \frac{2(\pi^2/4 + 1)R_L}{f} \approx 7R_L/f. \quad (9.52)$$

The optimum mode of operation, therefore, is dependent on the load. Matching techniques exist that reduce this dependence. It should be emphasized that the optimum conditions are different for $D \neq 0.5$. The nearly harmonic form of the output current is obtained if the Q factor is greater than 7 ($Q > 7$). The output voltage is changed by a small variation of the frequency. By increasing the commutation frequency, if $f > f_0 = 1/(2\pi\sqrt{L_r C_r})$, the output current and voltage are reduced.

Except in optimum conditions, a class E inverter may also operate in suboptimum or nonoptimum conditions, which arise when the load is variable. If $R_L < R_{L\text{opt}}$ (9.48), the voltage across the capacitor will reach zero value with a negative slope ($dv/dt < 0$) so that its current is $i_{C1} = C_1 dv_C/dt < 0$. Therefore, the first optimum mode condition (9.46) is met, but the second (9.47) is not. However, then the antiparallel diode will turn on and keep a zero voltage across the switch (Fig. 9.26). The transistor will turn on again at $V_{DS} = 0$. The function of this diode can be carried out by the internal p-n junction substrate-drain of the MOS transistor. This is the suboptimum mode.

The nonoptimum mode arises when $R_L > R_{L\text{opt}}$. Then, none of the two optimum mode conditions is met. The transistor will be turned on at a positive voltage ($V_{DS} > 0$) which will increase dynamic losses. This mode should be avoided.

The advantages of class E resonant inverters is the circuit simplicity (single-transistor structure), high efficiency (up to 96 %), and an almost harmonic load current resulting in negligible EMI. The operating frequency may be several MHz. It is limited by the input capacitance of the MOS transistor and is approximately $f_M \approx 0.2/(2\pi C_{DSS} R_L)$. By applying the corresponding matching circuit the optimum or suboptimum mode of operation can be accomplished for an arbitrary load.

A drawback of the class E inverters are quite high amplitudes of the current and voltage of the switch which may amount up to several times the corresponding input DC values V_{DC} and I_{DC} . Consequently, their application is restricted to the circuits having low voltages of the primary source V_{DC} .

Adding a rectifier to the output of a class E inverter results in a resonant DC/DC converter. The rectifier could be a standard half-wave or full-wave rectifier. The rectifier of the DC/DC converter in Fig. 9.27 is also a class E. The switching losses

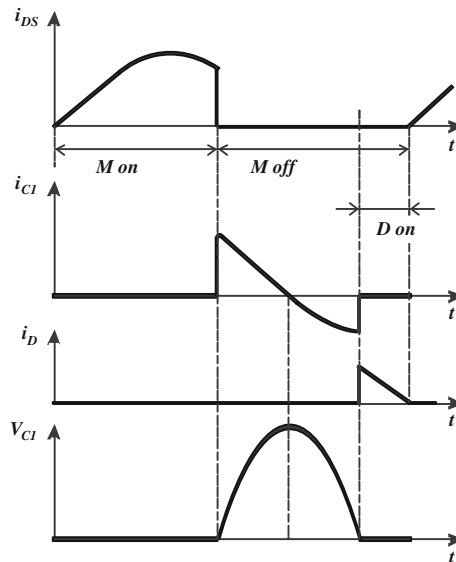


Fig. 9.26 The waveforms of a class E resonant inverter in the suboptimum mode

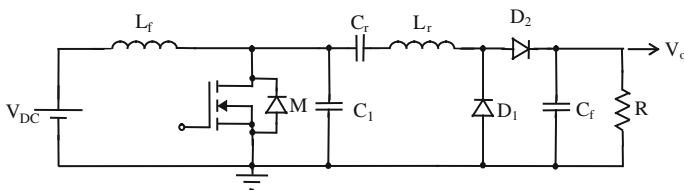


Fig. 9.27 The resonant E^2 converter

in its diodes are minimized because they change the state at small voltage variations dv/dt . Therefore, the converters in Fig. 9.27 is called the E^2 DC/DC converter.

9.5 DC/DC Converters Based on Resonant Switches

A resonant switch consists of a switching element (transistor or thyristor) and an oscillatory circuit. The oscillatory circuit shapes the current and voltage of the switch so that the commutation (turning on/off) is carried out at zero voltage. The resonant switches performing zero current commutation (Fig. 9.28) are called *Zero Current Switches (ZCS)* and those performing zero voltage commutation (Fig. 9.29) are called *Zero Voltage Switches (ZVS)*.

The resonant LC circuit of a ZCS switch, consisting of the coil L_r and the capacitor C_r , shapes the current through the switching element. The resonant coil L_r ,

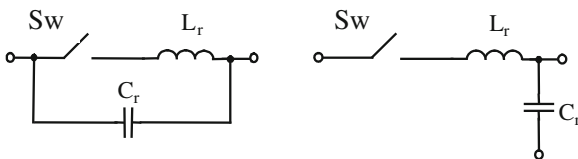


Fig. 9.28 The ZCS resonant switches

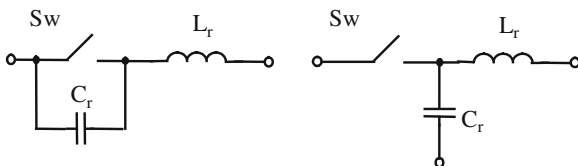


Fig. 9.29 The ZVS resonant switches

resists fast current changes in the switching transistor by keeping the current, during the switch-on process at a near-zero value until the voltage across P_r becomes negligibly small. While P_r is closed the current flowing through it is, due to the resonant circuit, of resonant character, i.e., contains current zero crossing. This enables turning off the switch at zero current.

The resonant capacitor C_r of the ZVS switches (Fig. 9.29) is short-circuited while P_r is closed. Therefore, during opening of P_r it will keep the voltage across P_r approximately zero until the current through P_r drops to a negligible value.

While P_r is open, the oscillations of the voltage in the oscillatory circuit involve voltage zero crossing. If this zero crossing is synchronized with the drive of the switch, turning on is completed at zero voltage.

The switching element is a bipolar or MOS transistor together with an anti-parallel diode (two-quadrant current switch) or with a series diode (two-quadrant voltage switch). The functions of these diodes will be explained by specific examples of DC/DC converters.

The topologies of DC/DC converters are obtained by replacing the switching elements of the PWM converters, described in Chap. 5, with resonant switches. In this way two basic groups of converters based on the resonant switches are obtained:

- Quasi-resonant converters—QR, and
- Multiresonant converters—MR.

The name “quasi-resonant” originates from the fact that the resonant process is established only during one half cycle. Taking into account the type of resonant switches, two groups of the quasi-resonant converters can be distinguished:

- ZCS quasi-resonant converters (ZCS-QR), and
- ZVS quasi-resonant converters (ZVS-QR).

9.5.1 ZCS Quasi-resonant Converters

The operating principle of the ZCS quasi-resonant converters will be explained by the example of the buck (step-down) converter (Fig. 9.30). A ZCS-QR converter is obtained by a direct replacement of the transistor T of the PWM forward converter of Fig. 5.1 by the ZCS resonant switches of Fig. 9.28. In this way one arrives at two versions of the buck ZCS-QR converters, Figs. 9.30 and 9.33. Owing to the internal structure of the substrate-drain of an MOS transistor it could conduct in the opposite direction if the source were on a higher potential. In order to prevent this, the diode D_s is connected in series with the transistor M so that the switching element can conduct only in one direction.

In the analysis of the quasi-static states, one starts from the same assumptions as in the case of the PWM converters, i.e.,

- filter inductance L_f is sufficiently high that the variations of the current through the filter can be neglected, thus its current is approximately constant and equal to I_0 , and
- the diodes and transistors are ideal switches.

The variations of the current of the resonant coil and of the voltage of the resonant capacitor within one switching cycle of the transistor M are shown in Fig. 9.31a. Let the transistor M turn on at an instant $t = 0$. Before this, it was off and the diode D was on, thus $i_L = 0$ and $V_{Cr} = 0$. After turning on of the transistor, the diode remains on until the current through the coil becomes greater than I_0 (Fig. 9.31b).

Initially, the coil takes over the whole of the voltage and does not allow a quick rise of the current through the transistor, this rise being linear since $V_{Cr} = V_D = 0$. In this way, the condition that the transistor turns on at zero voltage and zero current is fulfilled. Upon turning off the diode at the instant t_1 , the LC oscillatory circuit (Fig. 9.31c) causes i_L and V_{Cr} through the turned-on transistor to become oscillatory. The voltage across the capacitor lags (it is phase shifted) behind current i_L , which at $t = t_2$ becomes zero. Although the transistor is still on, the current through the coil L_r cannot change direction owing to the series diode D_s . Therefore, after t_2 , $i_{Lr} = 0$. After t_2 M can be turned on. Therefore, the condition of turning off at zero

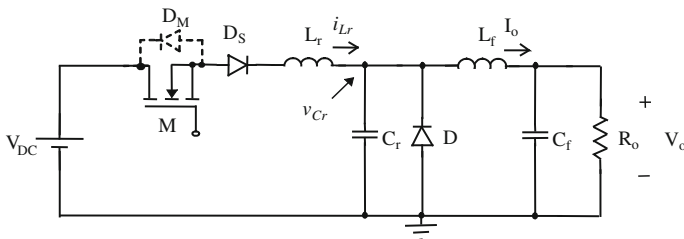


Fig. 9.30 The ZCS-QR forward converter

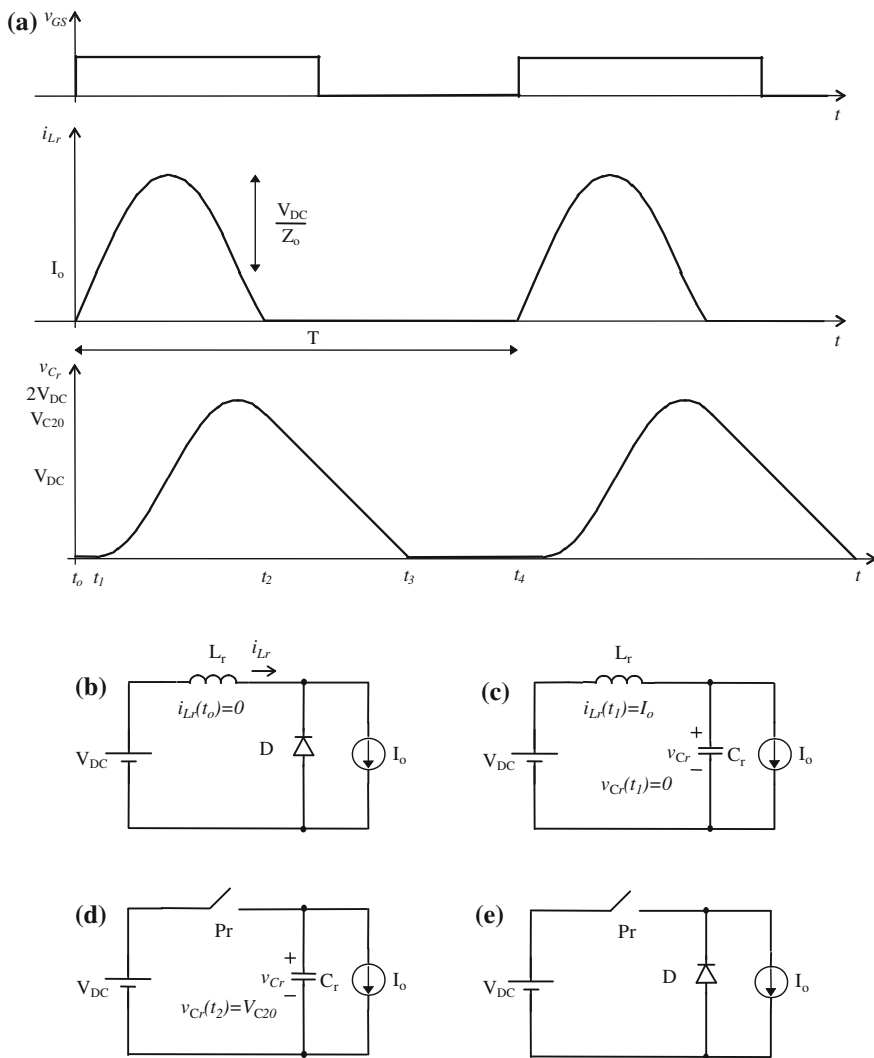


Fig. 9.31 The waveforms of coil current and capacitor voltage of the oscillatory circuit (a) and the equivalent circuits for each characteristic interval (b–e)

current is accomplished. During the interval after t_2 , the capacitor C_r is being discharged by the output current I_0 . The voltage across it decreases linearly and when it reaches zero (changes polarity) the diode is turned on again ($t = t_3$). Until the transistor is turned on again, the diode D is on, thus closing the circuit for I_0 .

Each of the characteristic intervals will be analyzed separately.

9.5.1.1 Interval T_{0-1} ($0 \leq t \leq t_1$)

The transistor and the diode are on. The initial current of the coil L_r is zero. Since $V_{Lr} = V_{DC}$, the coil current is

$$i_{Lr}(t) = \frac{1}{L_r} \int_0^t V_{DC} dt = \frac{V_{DC}}{L_r} t. \quad (9.53)$$

At $t = t_1$, $i_{Lr}(t_1) = I_0$ and the diode is turned off. By using (9.53), it turns out that

$$T_{0-1} = t_1 = L_r I_0 / V_{DC}. \quad (9.54)$$

9.5.1.2 Interval T_{1-2} ($t_1 \leq t \leq t_2$)

By turning off the diode, the oscillatory circuit $L_r C_r$ is established (Fig. 9.31c) and the following equations apply

$$V_{Cr}(t) = V_{DC} - L_r \frac{di_{Lr}(t)}{dt}, \quad (9.55)$$

$$i_{Cr}(t) = i_{Lr}(t) - I_0. \quad (9.56)$$

The solution of these differential equations, with the initial conditions $i_L(t_1) = I_0$ and $V_{Cr}(t_1) = 0$, is

$$i_{Lr}(t) = I_0 + \frac{V_{DC}}{Z_0} \sin[\omega_0(t - t_1)], \quad (9.57)$$

$$V_{Cr}(t) = V_{DC} \{1 - \cos[\omega_0(t - t_1)]\}, \quad (9.58)$$

where $Z_0 = \sqrt{L_r C_r}$ is the characteristic impedance of the oscillatory circuit and $\omega_0 = 1/\sqrt{L_r C_r}$ is the resonant frequency. As long as $V_{Cr}(t) < V_{DC}$ the current through the coil increases. It reaches its maximum at $V_{Cr} = V_{DC}$, or by taking into account (9.58), at $\omega_0(t - t_1) = \pi/2$. From this and equation (9.58), it follows that the maximum transistor current is

9.5.1.3 Interval T_{2-3} ($t_2 \leq t \leq t_3$)

The equivalent circuit for this interval is shown in Fig. 9.31d. The transistor M is turned off at zero current and the capacitor C_r is discharged by I_0 , thus:

$$V_{Cr} = V_{C20} - \frac{I_0}{C_r}(t - t_2). \quad (9.59)$$

Therefore, $V_{Cr}(t)$ decreases linearly. At its zero crossing, the diode D is turned on and keeps the voltage across the capacitor at zero value. This is the end of this time interval. From the conditions $V_{Cr}(t_3) = 0$ and (9.59), it follows

$$T_{2-3} = (t_3 - t_2) = \frac{V_{C20}C_r}{I_0}. \quad (9.60)$$

9.5.1.4 Interval T_{3-4} ($t_3 \leq t \leq t_4 = T$)

Within this interval the transistor is off and the diode is on, so $i_{Lr} = 0$ and $V_{Cr} = 0$. The equivalent circuit is shown in Fig. 9.31e. This interval ends by turning on the transistor, so

$$T_{3-4} = t_4 - t_3 = T - (T_{0-1} + T_{1-2} + T_{2-3}). \quad (9.61)$$

9.5.1.5 The Output Voltage

Ideally, without losses, the output voltage can be determined on the basis of the energy balance. Within one cycle, the energy of the power source W_s is equal to the energy absorbed by the load W_0 , where

$$W_s = \int_0^t p_s(t)dt = V_{DC} \int_0^T i_{Lr}(t)dt, \quad (9.62)$$

$$W_0 = \int_0^t p_0(t)dt = V_0 I_0 T. \quad (9.63)$$

Considering (9.53) and (9.57), it turns out that

$$\begin{aligned} W_s &= V_{DC} \int_0^{t_1} \frac{V_{DC}t}{L_r} dt + V_{DC} \int_{t_1}^{t_2} \left[I_0 + \frac{V_{DC}}{Z_0} \sin \omega_0(t - t_1) \right] dt \\ &= V_{DC} I_0 \left[\frac{t_1}{2} + (t_2 - t_1) + \frac{V_{DC}C_r}{I_0} (1 - \cos \omega(t_2 - t_1)) \right] \\ &= V_{DC} I_0 \left(\frac{T_{0-1}}{2} + T_{1-2} + T_{2-3} \right). \end{aligned} \quad (9.64)$$

From $W_s = W_0$ one obtains

$$V_O = V_{DC} \frac{T_{0-1}/2 + T_{1-2} + T_{2-3}}{T}. \quad (9.65)$$

It is obvious that (9.65) is similar to (4.11) which defines the output voltage of a PWM forward converter as $V_O = V_{DC} \tau/T$, where τ is the interval while the switching element is on. The interval τ of PWM converters is equivalent to the quasi-resonant interval of a quasi-resonant converter τ_{QR} , where

$$\tau_{QR} = T_{0-1}/2 + T_{1-2} + T_{2-3} \quad (9.66)$$

Therefore, (9.65) can be written in the form

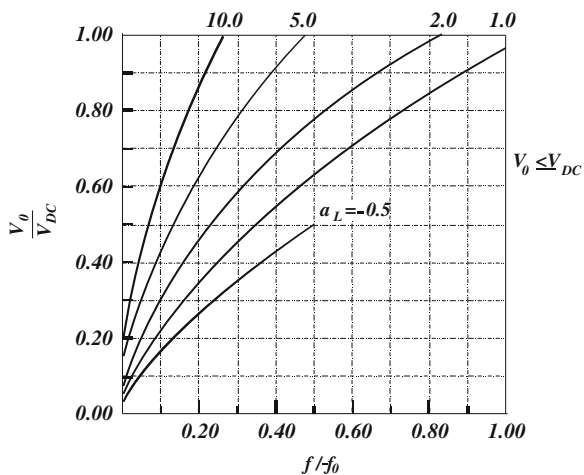
$$V_O = V_{DC} \frac{\tau_{QR}}{T}. \quad (9.67)$$

In this way a complete analogy is obtained for the output voltage of the PWM and the quasi-resonant forward converters. Since $\tau_{QR} < T$, the output voltage is smaller than the input voltage like in the PWM forward converters.

The τ_{QR} is denoted as quasi-resonant because the resonant changes are only a part of the whole cycle. From (9.54), (9.60), and (9.63) it is obvious that time τ_{QR} is a function of the output current I_O , the input voltage V_i , and the parameters of the oscillatory circuit L_r , C_r . Therefore, by varying the load and the input, the voltage τ_{QR} changes and so does the output voltage, V_O . Maintaining a constant output voltage is possible if the cycle time T or the frequency of the control pulses is varied. An increase of the control frequency increases the output voltage.

Figure 9.32 shows the dependence of the normalized output voltage (V_O/V_{DC}) on the normalized frequency, ff_0 with the load constant $a_L = R_L/Z_0$ as a parameter. The sensitivity of the function $V_O/V_{DC} = \Phi(ff_0)$ increases with decreasing the load

Fig. 9.32 The frequency characteristic of the ZCS-QR forward converter



(increasing of R_L). Without the diode D_s the internal diode of the MOS transistor would conduct the negative current of the resonant coil. In that case the quasi-resonant interval is shortened and the output voltage is an approximately linear function of frequency

$$V_0 \approx (V_{DC}/f_0)f,$$

regardless of the load. In this case, however, a part of the energy accumulated in the resonant capacitor is returned to the primary source instead of contributing to the output current.

Example 9.4 The parameters of the ZCS-QR converter of Fig. 9.30 are $V_{DC} = 12$ V, $C_r = 0.1$ μ F, $L_r = 810$ μ H, $I_0 = 1$ A, and frequency $f = 100$ kHz. Determine:

- the output voltage, the maximum transistor current, and the maximum reverse voltage of diode D ,
- frequency f at which the voltage is 6 V, at the same current,
- the maximum frequency.

The circular frequency and the characteristic impedance of the oscillatory circuit are, respectively,

$$\omega_0 = 1/\sqrt{C_r L_r} = 1/\sqrt{(0.1 \times 10^{-6})(10 \times 10^{-6})} = 10^6 \text{ rad/s},$$

$$Z_0 = \sqrt{L_r/C_r} = \sqrt{(10 \times 10^{-6})/(0.1 \times 10^{-6})} = 10 \Omega.$$

The characteristic time intervals are

$$T_{0-1} = t_1 = I_0 L_r / V_{DC} = 1 \times (10 \times 10^{-6}) / 12 = 0.833 \mu\text{s}.$$

$$T_{1-2} = t_2 - t_1 = \frac{1}{\omega_0} \left[\pi + \arcsin \frac{Z_0 I_0}{V_{DC}} \right] = \frac{1}{10^6} \left[\pi + \arcsin \frac{1 \cdot 10}{12} \right] = 4.13 \mu\text{s}.$$

$$\begin{aligned} T_{2-3} &= t_3 - t_2 = \frac{C_r V_{DS}}{I_0} \{1 - \cos[\omega_0(t_2 - t_1)]\} \\ &= \frac{(0.1 \times 10^{-6}) \times 12}{1} [1 - \cos(10^6 \times 4.13 \times 10^{-6})] = 1.86 \mu\text{s}. \end{aligned}$$

The quasi-resonant interval is $\tau_{QR} = T_{0-1}/2 + T_{1-2} + T_{2-3} = 6.4065 \mu\text{s}$.

(a) The output voltage is

$$V_O = V_{DC}\tau_{QR}/T = V_{DC}\tau_{QR}f = 12 \times (6.4065 \times 10^{-6}) \times (100 \times 10^6) = 7.69 \text{ V}.$$

- The maximum transistor current is $I_{DSM} = I_0 + V_{DC}/Z_0 = 1 + 12 \text{ V}/10 \Omega = 2.2 \text{ A}$.
- The maximum reverse voltage of the diode D is equal to the maximum voltage across the resonant capacitor, i.e., $V_{CrM} = 2V_{DC} = 2 \times 12 = 24 \text{ V}$.

(b) When the output current I_0 and the output voltage V_0 do not vary, then the quasi-resonant interval does not depend on the output voltage, and

$$f = V_O(V_{DC}\tau_{QR}) = 6 \text{ V}/(12 \text{ V} \times 6.406 \text{ ms}) = 78 \text{ kHz}.$$

(c) The cycle of control pulses has to be

$$T > t_3 = T_{0-1} + T_{1-2} + T_{2-3} = 0.833 + 4.13 + 1.86 = 6.82 \mu\text{s}, \text{ and } f_{\max} = 1/T_{\min} = 1/t_3 = 146 \text{ kHz}.$$

The ZCS-QR forward DC/DC converter based on the resonant switch in Fig. 9.28a is shown in Fig. 9.33a. Initially, at $t = 0$, the transistor M is off, the diode D is on, so the voltage across the resonant capacitor is V_{DC} , and the current of the resonant coil is zero. Therefore, the transistor is turned on at zero current. During the quasi-resonant interval τ_Q , while the transistor is on and the diode is off, the oscillatory character of i_L and V_{Cr} , involving zero crossing, is established. Owing to this, the transistor turning off at zero current is enabled. In fact, the principle is the same as for the circuit in Fig. 9.30. The waveforms and the equivalent circuits for each characteristic time interval presented in Fig. 9.33 clearly indicate the processes in the circuit.

The general characteristics of the ZCS-QR forward converter can be summarized as follows:

- The current of transistor M is approximately zero at turn on and turn off, thus dynamic losses are negligible.
- The maximum current is load dependent ($I_{DSM} = I_0 + V_{DC}/Z_0$).
- The diode D is turned on at small voltage variations dv/dt so the requirements regarding its choice are not tight.
- In order to enable the transistor to be turned off at zero current, the current of the resonant coil should reach zero value, which is obtained if its amplitude is higher than the output current, i.e., $V_{DC}/Z_0 \geq I_0$. On the basis of this, it follows that the condition for turning off the transistor at zero current is formulated as $Z_0 V_O/V_{DC} \leq R < \infty$.

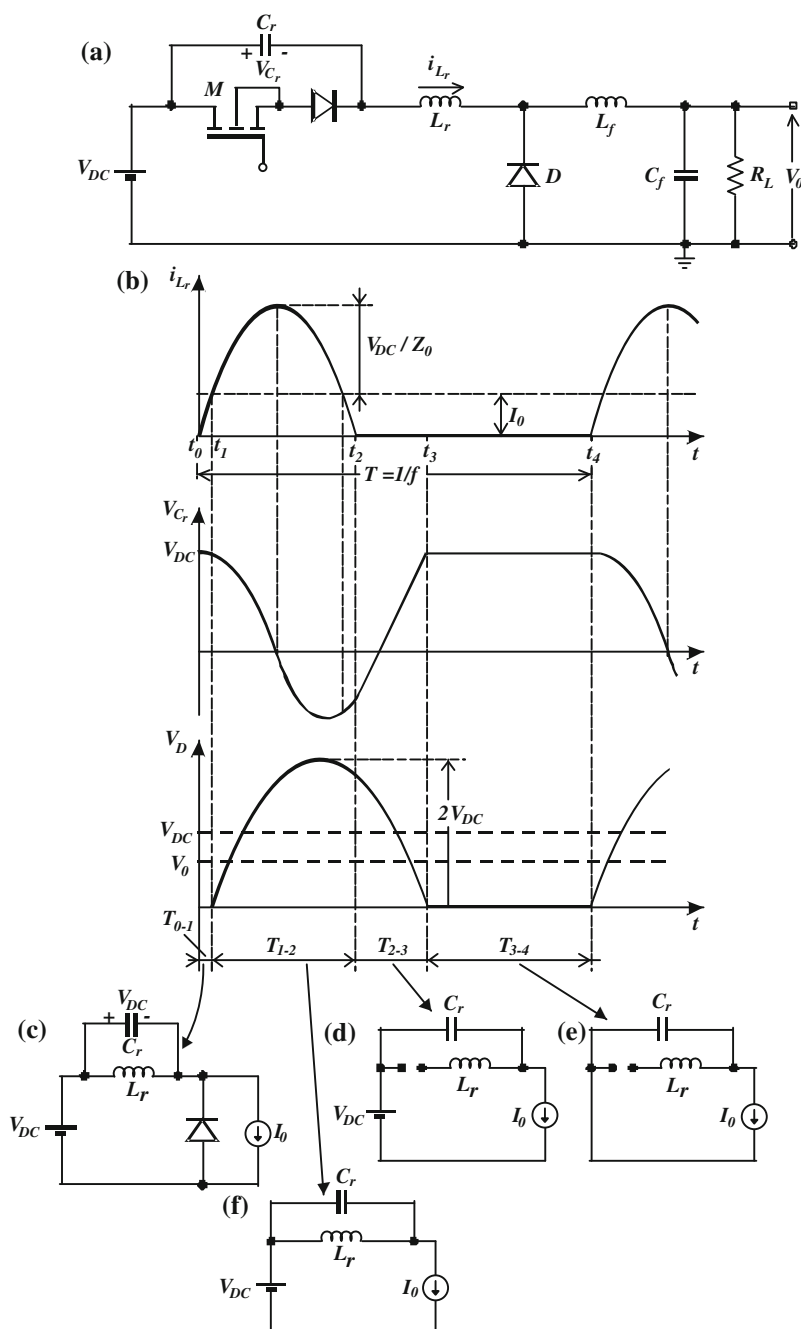


Fig. 9.33 The second version of a ZCS-QR forward converter (a), characteristic waveforms (b), and equivalent circuits within one cycle (e-f)

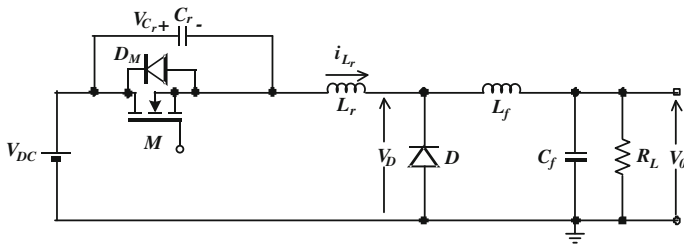


Fig. 9.34 The ZVS-QR forward converter

9.5.2 ZVS Quasi-resonant Converters

The ZVS quasi-resonant DC/DC converters are obtained by replacing the switching element of a PWM converter by a ZVS resonant switch. The principle of the operation of the ZVS-QR converters will be considered by presenting the example of the forward converter (Fig. 9.34), assuming that the current of the output choke L_f is approximately I_0 and that the transistor and the diode are ideal switches.

The waveforms of the voltage across the resonant capacitor C_r and the current through the coil L_r are shown in Fig. 9.35a. Prior to the instant $t_0 = 0$, when the cycle begins, the transistor M is on. The current through the transistor is I_0 . The capacitor C_r is empty ($V_{C_r} = 0$). The diode D is off. At an instant t_0 the transistor is turned off at zero voltage. After that, the current I_0 flows through C_r and L_r (Fig. 9.35b) and the voltage across the transistor increases linearly. The variation of this voltage while the current through the transistor is decreasing is negligible, so the dynamic losses at turning off are negligible. At the instant t_1 , when $V_{C_r} = V_{DC}$, the voltage across the diode D changes its direction and the diode turns on (Fig. 9.35c). The series oscillatory circuit $L_r C_r$ is established and so are the oscillatory variations of the voltage V_{C_r} and the current i_{L_r} involving zero crossings. Upon zero crossing of the voltage V_{C_r} , the antiparallel diode D_M will turn on and limit further variations of V_{C_r} , thus $V_{C_r} = 0$. Then the control pulse turns the transistor M on, ensuring a zero voltage turn on. In order to determine the output voltage it is necessary to determine the quasi-resonant cycle. For this purpose the circuit will be analyzed by intervals.

9.5.2.1 Interval T_{0-1} ($0 \leq t \leq t_1$)

The transistor M and the diode D are off. The equivalent circuit of the converter, including the initial conditions, is shown in Fig. 9.35b. The voltage across the capacitor C_r is

$$V_{C_r}(t) = \frac{I_0}{C_r} t. \quad (9.68)$$

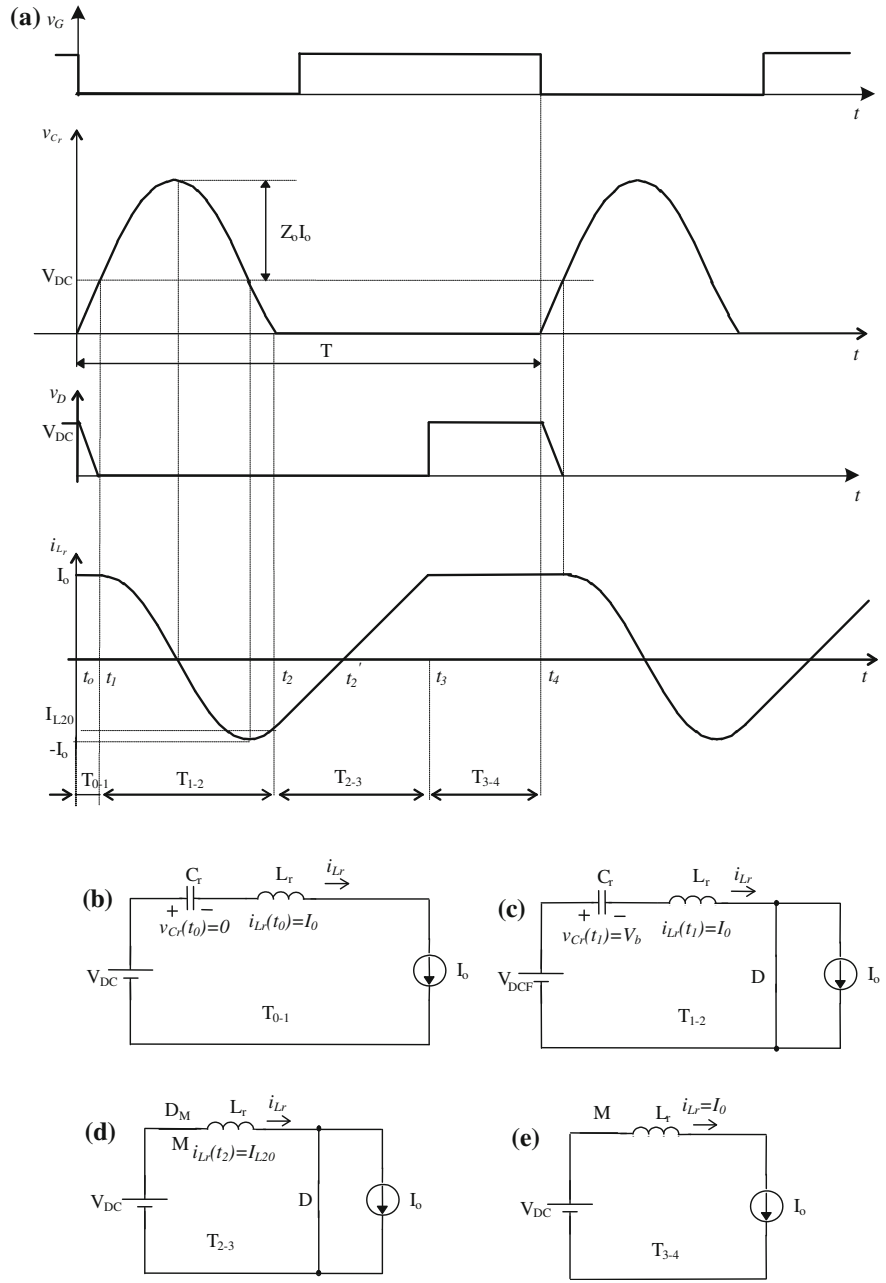


Fig. 9.35 The waveforms within one cycle of the ZVS-QR forward converter (a), and the equivalent circuits (b–e)

Since the current through the coil is constant, the voltage drop across it is negligible and the voltage across the diode is

$$V_D = V_{DC} - V_{Cr}(t). \quad (9.69)$$

This interval ends when the diode is turned off, i.e., at $V_D(t) = 0$, and

$$T_{0-1} = t_1 = \frac{C_r V_{DC}}{I_0}. \quad (9.70)$$

9.5.2.2 Interval T_{1-2} ($t_1 \leq t \leq t_2$)

The transistor is off, whereas the diode is on (Fig. 9.35c). Now

$$L_r \frac{di_{Lr}(t)}{dt} + V_{Cr}(t) = V_{DC}, \quad (9.71)$$

$$i_{Cr}(t) = C_r \frac{dV_{Cr}(t)}{dt}, \quad (9.72)$$

and the initial conditions are marked in Fig. 9.35c. The solution of this set of equations is given by

$$i_{Lr}(t) = I_0 \cos[\omega_0(t - t_1)], \quad (9.73)$$

$$V_{Cr}(t) = V_{DC} + I_0 Z_0 \sin[\omega_0(t - t_1)], \quad (9.74)$$

where ω_0 is the circular resonant frequency and Z_0 is the characteristic impedance of the oscillatory circuit. The maximum drain–source voltage of the transistor is equal to the amplitude of the voltage across capacitor C_r , V_{Cr} , i.e.,

$$V_{DSM} = V_{CrM} = V_{DC} + I_0 Z_0 = V_{DS} + I_0 \sqrt{L_r/C_r}. \quad (9.75)$$

This interval ends at $V_{Cr}(t_2) = 0$, so

$$T_{1-2} = t_2 - t_1 = \frac{1}{\omega_0} \left[\pi + \arcsin \frac{V_{DC}}{I_0 Z_0} \right]. \quad (9.76)$$

The current of the resonant coil at the end of this interval is

$$I_{L20} = I_0 \cos[\omega_0(t_2 - t_1)]. \quad (9.77)$$

The voltage across the capacitor may become zero only if $I_0 Z_0 > V_{DC}$, therefore it turns out that the maximum resistance of the load which still permits turning on of the transistor at zero voltage is

$$R_{L\max} = Z_0(V_0/V_{DC}). \quad (9.78)$$

9.5.2.3 Interval T_{2-3} ($t_2 \leq t \leq t_3$)

Both diodes, D and D_M , are on. The antiparallel diode D_M conducts the negative current of the coil L_r toward the primary source. The transistor M should turn on before the instant t_2 in order to take over the positive current i_L . Therefore, in the interval T_{2-3} the coil is connected to the primary source by a low resistance (Fig. 9.35d). The voltage across the coil L_r is constant and equal to V_{DC} , so the coil current increases linearly, i.e.,

$$i_{Lr}(t) = I_{L20} + \frac{1}{L_r} \int_{t_2}^{t_3} V_{DC} dt = I_{L20} + \frac{V_{DC}}{L_r} t. \quad (9.79a)$$

This interval ends by turning off the diode D at $i_{Lr}(t) = I_0$, and from (9.79a)

$$T_{2-3} = t_3 - t_2 \frac{I_0 - I_{L20}}{V_{DC}} L_r = \frac{I_0 L_r}{V_{DC}} [1 - \cos(\omega_0 T_{1-2})]. \quad (9.79b)$$

9.5.2.4 Interval T_{3-4} ($t_3 \leq t \leq t_4$)

The transistor is on and the diode is off. The equivalent circuit is as shown in Fig. 9.35e. The current I_0 flows via the transistor which keeps the voltage across C_r at zero value until it is turned on again within the next cycle.

9.5.2.5 Output Voltage

The voltage across the diode D (Fig. 9.35a) is the input voltage of the output filter. Therefore, the output voltage can be calculated as the average value of the voltage V_D , i.e.,

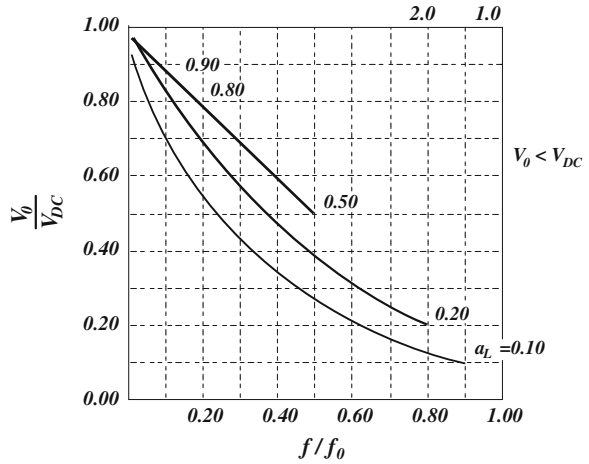
$$V_0(t) = \frac{1}{T} \int_0^T V_D(t) dt. \quad (9.80)$$

According to Fig. 9.35a, and taking into account (9.69), it turns out that

$$V_D(t) = \begin{cases} V_{DC}(1 - t/t_1), & 0 < t < t_1 \\ 0 & t_1 < t < t_3 \\ V_{DC} & t_3 < t < T. \end{cases} \quad (9.81)$$

By combining (9.80) and (9.81) one obtains:

Fig. 9.36 The normalized frequency characteristic of the ZVS-QR forward converter



$$V_0 = V_{DC} \left(1 - \frac{\tau_{QR}}{T} \right), \quad (9.82)$$

where, analogously to the ZCS-QR converters,

$$\tau_{QR} = T_{0-1}/2 + T_{1-2} + T_{2-3}, \quad (9.83)$$

is the quasi-resonant interval. Since this interval is load-current-dependent, the output voltage is also a function of the load (Fig. 9.36). The load constant is dependent on the frequency characteristics of the converter in Fig. 9.36.

According to (9.78), the permitted range of load variations still allowing zero voltage turning on the transistor is

$$0 < R_L < Z_0(V_0/V_{DC}).$$

The output voltage is a function of the frequency of the control pulses of the transistor M . Increasing this frequency causes the output voltage to drop. At a constant voltage V_{DC} and output current I_0 the quasi-resonant interval is constant, whereas the interval T_{3-4} varies.

At first glance there is no corresponding analogy between the V_0/V_{DC} ratios of the ZVS-QR and the PWM converters like the one existing between the ZCS-QR and the PWM converters. This is only apparent, because in the quasi-resonant interval τ_{QR} of the ZVS-QR converters the transistor is off, whereas in the PWM during τ it is on. With respect to the interval in the PWM converters when the transistor is off, the output voltage is

$$V_0 = V_{DC} \frac{\tau}{T} = V_{DC} \frac{T - \tau_{\text{off}}}{T} = V_{DC} \left(1 - \frac{\tau_{\text{off}}}{T} \right). \quad (9.84)$$

Consequently, the analogy between the ZVS-QR and the PWM converters is complete.

The general characteristics of the ZVS-QR DC/DC forward converters can be summarized as follows:

- The switching element is turned on and off at approximately zero voltage across it, thus the switching losses are negligible.
- Since the dynamic losses are small these converters may operate at very high frequencies (up to 10 MHz).
- The output capacitance of the transistor is a constituent part of the resonant capacitor C_r and has no adverse influence on the operation of the converter.
- The maximum voltage across the transistor is higher than that of the PWM converters and is load dependent ($V_{DSM} = V_{DC} + Z_0 I_0$). The breakdown voltage of the transistor has to be higher than V_{DSM} at the maximum current I_0 .
- The capacitance of the reverse biased diode D , during the interval when it is turned off, together with the resonant coil may cause undesirable oscillations which induce additional losses and control problems.

Example 9.5 The following parameters of a ZVS-QR forward converter are known: $V_{DC} = 20$ V, $L_r = 1$ μ H, $C_r = 0.047$ μ F, and $I_0 = 5$ A. One should determine:

- the switching frequency so that the output voltage is $V_0 = 10$ V,
- the maximum voltage across the switching element, and
- the maximum resistance of the load still permitting the zero voltage turning on of the transistor.

The parameters of the resonant circuit are

$$\omega_0 = 1 / \sqrt{10^{-6} \times (0.047 \times 10^{-6})} = 4.61 \times 10^6 \text{ rad/s},$$

$$Z_0 = \sqrt{L_r / C_r} = \sqrt{10^{-6} / (0.047 \times 10^{-6})} = 4.61 \Omega.$$

The time intervals

$$T_{0-1} = t_1 = V_{DC} C_r / I_0 = 20 \times (0.047 \times 10^{-6}) / 5 = 0.188 \mu\text{s}.$$

On the basis of (9.76) and (9.79a), respectively,

$$T_{1-2} = t_2 - t_1 = \frac{1}{4.61 \times 10^6} \left[\arcsin\left(\frac{20}{5 \times 4.61}\right) + \pi \right] \approx 0.9 \mu\text{s},$$

$$T_{2-3} = t_3 - t_2 = \frac{5 \times 10^{-6}}{20} [1 - \cos(4.61 \times 10^6 \times 0.9 \times 10^{-6})] = 0.37 \mu\text{s},$$

the quasi-resonant interval is $\tau_{QR} = T_{0-1}/2 + T_{1-2} + T_{2-3} = 1.36 \mu\text{s}$.

(a) From (9.82) it follows

$$f = \frac{1}{\tau_{QR}} \left(1 - \frac{V_O}{V_{DC}} \right) = \frac{1}{1.36 \times 10^{-6}} \left(1 - \frac{10}{20} \right) = 3.67 \text{ kHz.}$$

(b) According to (9.75), the maximum voltage drain–source of the transistor is

$$V_{DSM} = 20 \text{ V} + 5 \text{ A} \times 4.61 \Omega = 43 \text{ V.}$$

(c) With reference to (9.78), the maximum resistance of the load still permitting the zero voltage turning on the transistor is

$$R_{L\max} = 4.61 \Omega \frac{10}{20} = 2.61 \Omega.$$

9.5.3 Multiresonant Converters

The *multiresonant* (MR) ZVS converters have one additional capacitor and a diode (Fig. 9.37). The capacitor C_D includes the capacitance of the reverse biased diode which was causing the undesirable oscillations in the ZVS-QR converters.

Here, the oscillations through C_D are taken into account and controlled. An example of a ZVS-MR forward DC/DC converter is shown in Fig. 9.38. Compared to the topology of the corresponding ZVS-QR converter it differs only by the capacitor C_D . During time intervals when the diode is on, the capacitor C_D is short-circuited and has no influence. When the diode is off and the transistor is on, $C_D = C_{r1}$ and together with L_r it forms an oscillatory circuit. During time intervals when both the transistor and the diode are off, the capacitor C_D together with C_M forms a resonant capacitor $C_{r2} = C_D C_M / (C_D + C_M)$. Therefore, oscillatory circuits made of different elements are active in different time intervals. In one of these, the resonant capacitor is $C_{r1} = C_D$ and in the other $C_{r2} = C_D || C_M$. For this reason these converters are denoted as multiresonant.

The general characteristics of ZVS-MR converters can be summarized as follows:

- All main parasitic elements of the converter are included in the resonant elements. The switching elements change states at zero voltage so the dynamic losses are negligible. Therefore, they can operate at very high frequencies (10 MHz) and reach high power densities ($>50 \text{ W/inch}^3$).
- Compared to the ZVS-QR converters the maximum voltage across the transistor is lower, but the current in the oscillatory circuit is increased so the ohmic losses are increased.

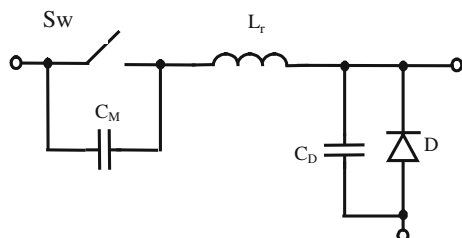


Fig. 9.37 A ZVS multiresonant switch

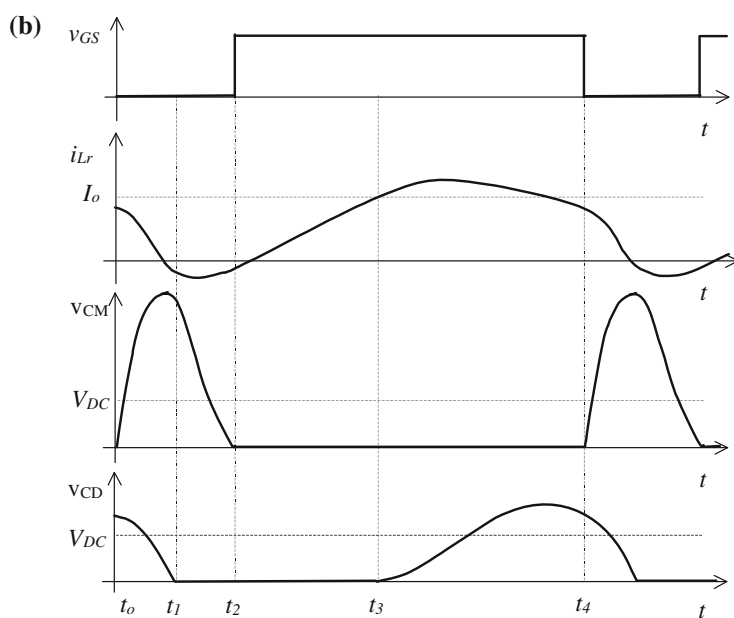
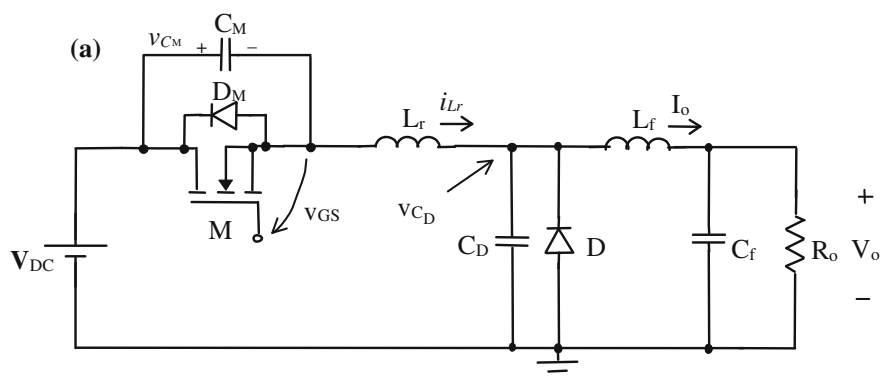


Fig. 9.38 A ZVS multiresonant forward converter (a) and its waveforms (b)

9.6 ZVS Resonant DC/AC Converters

The ZVS resonant DC/AC converters (Fig. 9.39a) are essentially the simplified class E resonant inverters where the reactive L_f - C_f net is a function of the resonant L_r - C_r net. On the other hand, since the resonant capacitor C_r is connected in parallel with the P_r switch, the circuit in Fig. 9.39a is a resonant converter where the commutation of the switching element is at zero voltage. According to this, a ZVS resonant DC/AC converter is a loaded ZVS. The load may be, for example, a motor having the internal inductance sufficiently high so that the motor current within one resonant cycle may be considered constant. Therefore, the load in Fig. 9.39a is represented by a current generator I_0 . Since the basic application of a DC/AC converter is supplying a load by AC current when the primary source is DC, the original name of this group of converters is the resonant DC-phase (link) inverters.

In the initial state, the switch P_r is on (Fig. 9.39c). The current through the resonant coil increases linearly. When i_{L_r} reaches the value of the load current, I_0 , the current through the switch becomes zero. The switch P_r is then turned off. Since $V_{C_r} = 0$, turning off occurs at zero voltage and a very small (ideally zero) current. Upon the turn off of the switch, there remains a loaded oscillatory circuit (Fig. 9.39d), whose current and voltage are, respectively,

Fig. 9.39 A ZVS resonant DC/AC converter (a), the waveforms (b), and equivalent circuits (c and d)

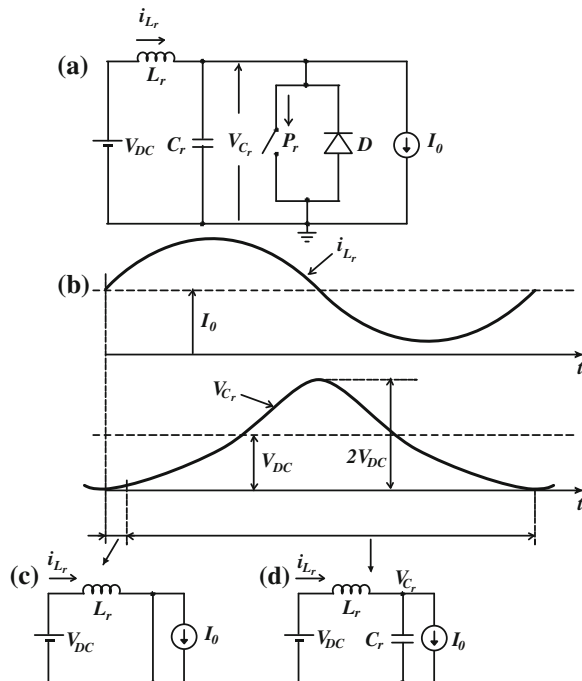
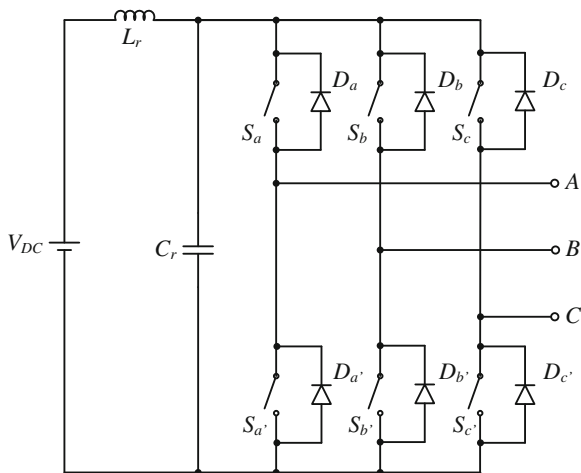


Fig. 9.40 A ZVS resonant DC/AC three-phase inverter



$$i_{L_r}(t) = I_0 + \frac{V_{DC}}{Z_0} \sin[\omega_0(t - t_0)], \quad (9.85)$$

$$V_{C_r}(t) = V_{DC}[1 - \cos(\omega_0 t)], \quad (9.86)$$

where Z_0 is the characteristic impedance of the oscillatory circuit. Therefore, these variations are harmonic with zero voltage across the capacitor at the beginning and at the end of each resonant cycle. Thus the switch control should be synchronized so that it turns on or off when V_{C_r} is close to zero. The control pulse frequency is approximately equal to the frequency of the oscillatory circuit. The switch is on only during short intervals, required by the resonant coil to accumulate the energy from the DC source. While the switch is on, the coil current is close to I_0 so the current through the switch is very small. Since turning on and off of the switch occurs at zero voltage, the dynamic losses of the converter due to the change of the states of the switch are negligible.

The described concept of the DC/AC converters can be implemented in three-phase PWM inverters (Fig. 9.40). The switch and the diode are the constituent parts of the three-phase bridge. The commutation of the switch in each arm of the bridge is performed when the voltage across the resonant capacitor reaches zero value.

9.7 Soft Switching PWM DC/DC Converters

The soft switching implies the change of the states of the switch at very low voltages, currents, and dissipations of the switch. Ideally, the switch would change the states at zero current and zero voltage. In practice different techniques of approximately zero current or zero voltage commutation of the switch are in use.

Dynamic losses in both cases are negligible. In that sense all resonant converters are the converters involving soft switching.

The emphasis on soft switching in resonant converters is aimed at stressing that some sort of advanced technique in the resonant converters is being introduced (constant frequency control, the maximum current or voltage reduction, etc.). Each improvement, however, causes impairment of some other parameters.

In this section two PWM topologies involving soft switching are described. In their quasi-static states they correspond to the conventional PWM converters, but the changes of states of the switch involve soft switching. These are:

- the phase shift bridge converters, and
- the resonant transitions PWM converters.

These converters retain all the good properties of the conventional PWM converters (operation at a constant frequency, small maximum voltage and current of the switch, and small ohmic losses) and at the same time reduce dynamic losses and stresses in the circuit that occur because of large voltage and current variations. Soft switching in phase shift bridge converters is accomplished through the parasitic elements of the circuit utilizing the phase shifted control pulses of the switching elements. Therefore, if the control module is excluded, the basic topology remains that of the conventional PWM bridge converters.

The topology of the resonant transitions PWM converters is modified by a resonant switch which ensures a resonant change of the voltage across the main switching element only during its commutation.

9.7.1 Phase Shift Bridge Converters

The topology of the basic circuit of a phase shift bridge converter (Fig. 9.41) is in fact a bridge connection of the symmetric converter (Fig. 4.29). The coil L_r (Fig. 9.39) is not a separate element. It is an equivalent inductance comprising of the stray inductance of the transformer and a possible inductance of the circuit connections. It is extracted here for the purpose of facilitating the explanation of the principle. The capacitors C_i and the diodes D_i ($i = 1, \dots, 4$), also do not represent separate components; they are actually the substrate-drain p-n junctions of the MOS transistors M_i , which behave like capacitors at reverse polarization and like small resistors at forward polarization.

The peculiarity of the phase shifted bridge converters, compared to the conventional converters, is the system of control which enables the active use of the parasitic elements of the components already present in the circuit. As emphasized by the name, the control is carried out by the phase shifted pulses. The conventional PWM connections allow the conduction of the diagonal switches of the bridge only. In these converters, during preparations for soft switching, either both upper and both lower transistors of the bridge are conducting. This interval is controlled by the

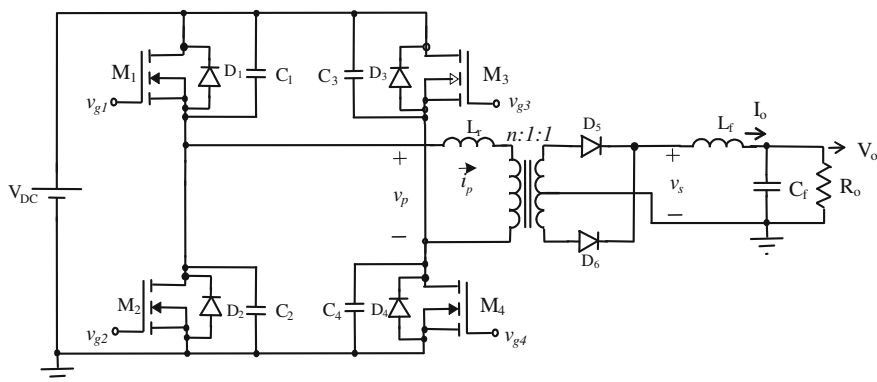


Fig. 9.41 A phase shifted bridge converter

dead times of the phase shifted pulses at the transistor gates. Therefore, the role of the dead time in the phase shifted connections is twofold:

- it prevents simultaneous conduction of the transistors of the same arm of the bridge, and
- it enables the preparation for the soft switching of the transistors.

The control pulse frequency on all phases is constant, with a 50 % duty cycle. The duty cycle of the secondary voltage of the transformer is phase shift dependent. For this reason the output voltage is a function of the phase shift. Therefore, compared to the conventional PWM converters where the output voltage is controlled by varying the duty cycle and the resonant converters where this control is accomplished by varying the frequency, the output voltage of these converters is controlled by varying the phase shift of the control pulses at a constant frequency. The phase shift of the control pulses of the transistors in the opposite arms of the bridge is variable. The pulses of the same arm (M_1 – M_2 or M_3 – M_4) are counter-phased with the dead time for the preparation of the soft switching.

The principle of operation of the phase shift PWM converters will be explained with the aid of the waveforms (Fig. 9.42) and equivalent circuits for each characteristic interval (Fig. 9.43). The state in the circuit and the variations of the primary current and the characteristic voltages will be monitored from the moment t_0 when the high voltage level in the transformer secondary is established.

9.7.1.1 Interval T_{0-1} ($t_0 \leq t \leq t_1$)

In this interval the gate voltages of the transistors M_1 and M_4 are high and these transistors are on. The other two transistors are off since $V_{g2} = V_{g3} = 0$. The equivalent circuit is shown in Fig. 9.43a. The voltage of the transformer primary is $V_p = V_{DC}$. The transfer of energy to the load in this interval is identical to the one in

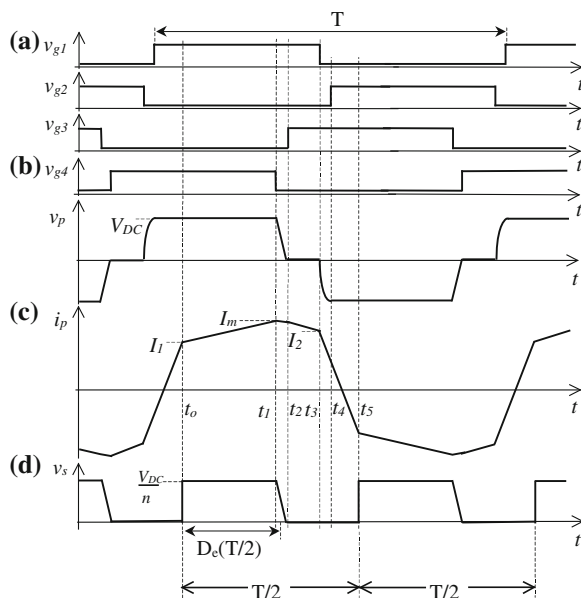


Fig. 9.42 The waveforms of control pulses at the gates of the transistors (a), voltage and current of the primary (b and c), and secondary voltage of the transformer (d)

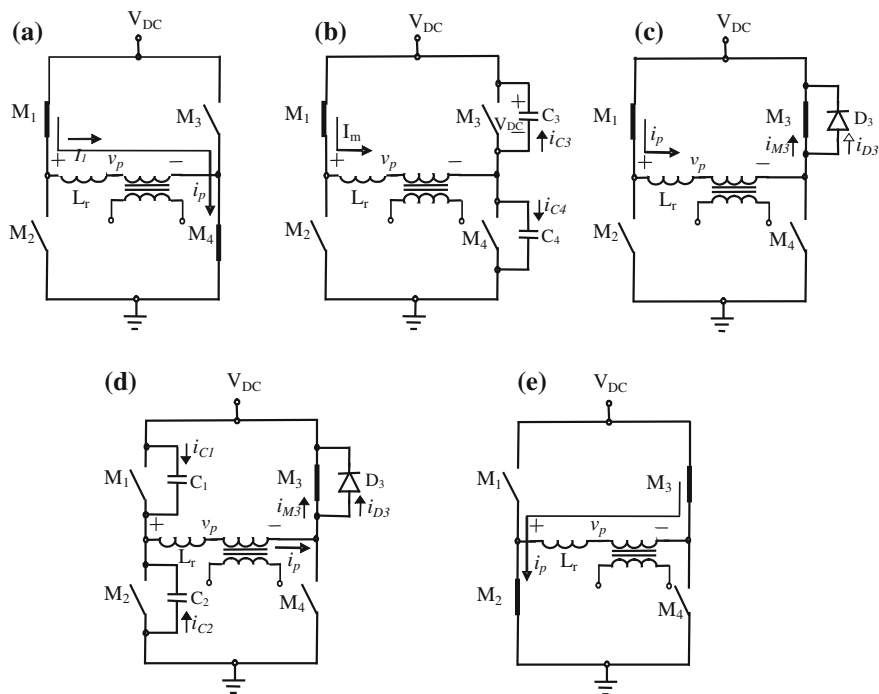


Fig. 9.43 The equivalent circuits of the converter within the characteristic time intervals. (a) T_{0-1} , (b) T_{1-2} , (c) T_{2-3} , (d) T_{3-4} , (e) T_{4-5}

the conventional converters. Since the voltage of the primary is constant, its current is a linear function of time. It can be expressed as the output current referred to the primary side of the transformer, i.e.,

$$i_p(t) = I_1 + \frac{V_{DC}/n - V_0}{nL_f}(t - t_0), \quad (9.87)$$

where I_1 is the initial primary current and n is the transformation ratio of the transformer. This interval ends at the instant the transistor M_4 is turned off when $V_{g4} = 0$. This turning off occurs at zero voltage since the capacitor is empty while M_4 is on.

9.7.1.2 Interval T_{1-2} ($t_1 \leq t \leq t_2$)

This interval is equal to the dead time of the control pulses of the transistors in the right arm of the bridge, i.e.,

$$T_{1-2} = t_{D34}. \quad (9.88)$$

Only the transistor M_1 is on (Fig. 9.43b). Now C_4 is being charged and C_3 discharged since it was previously charged to V_{DC} by the residual primary current I_{pM} . This is the maximum primary current. The variation of this current within interval T_{1-2} is negligible so the charging of C_4 and discharging of C_3 are by a constant current and with a linear voltage variation.

Consequently, the primary and the secondary voltage of the transformer also vary linearly (Fig. 9.42b, d). The capacitor C_3 should discharge to zero voltage. Since the voltage variation across C_3 and C_4 is

$$\Delta V_{Ce} = \frac{I_{pM}}{C_e}t, \quad C_e = C_3 + C_4, \quad (9.89)$$

from condition $\Delta V_{Ce}(T_{1-2}) = V_{DC}$, it follows that the dead time is

$$t_{D3,4min} = C_e V_{DC} / I_{pM}. \quad (9.90)$$

9.7.1.3 Interval T_{2-3} ($t_2 \leq t \leq t_3$)

The end of the interval T_{1-2} and the beginning of the interval T_{2-3} coincide with the positive pulse at the gate of the transistor M_3 , when the transistor is turned on. This turning on is at zero voltage because C_3 has discharged previously. During the interval T_{2-3} both upper transistors of the bridge, M_1 and M_3 , are on. The primary and the secondary voltages are equal to zero. Therefore, the primary of the transformer in this interval is short-circuited. The current through the primary is the

secondary current referred to the primary which is approximately a linear function of time, i.e.,

$$i_p(t) = I_{pM} - \frac{V_0}{nL_f}(t - t_2). \quad (9.91)$$

This interval ends at $V_{g1} = 0$ when M_1 is turned off. Thus T_{2-3} is the time between the pulses V_{g1} and V_{g3} .

9.7.1.4 Interval T_{3-4} ($t_3 \leq t \leq t_4$)

The transistor M_1 is off. This turning off occurred at zero voltage. Only the transistor M_3 remains on (Fig. 9.43d). This time interval is determined by the dead time of the control pulses of the transistors M_1 and M_2 in the left arm of the bridge and is approximately equal to one quarter of the resonant interval, i.e.,

$$T_{3-4} = t_{D1,2} \approx \frac{\pi}{2} \sqrt{L_r C_r}. \quad (9.92)$$

The capacitor C_1 is being charged and C_2 is discharged by the current appearing due to the energy accumulated in the resonant coil. In order to discharge C_2 to zero and to prepare M_2 for soft switching in the next interval, the energy accumulated in the coil L_r has to be sufficient to discharge C_2 and charge C_1 , i.e.,

$$\frac{1}{2} L_r I_2^2 > \frac{1}{2} C_1 + C_2 V_{DC}^2 = \frac{1}{2} C_e V_{DC}^2, \quad (9.93)$$

where I_2 is the primary current of the transformer at instant t_3 . From (9.93), it follows that the current has to be

$$I_2 > V_{DC} \sqrt{C_e / L_r}, \quad (9.94)$$

which is met at high output loads. If the condition (9.94) is not met at the maximum voltage V_{DC} and at the minimum load in the designed range of load variations, then a separate coil is used for the resonant coil. This increases the energy required for charging C_1 and discharging C_2 necessary for the preparation of soft switching.

The use of a separate resonant coil reduces the slope of the primary current within interval $t_3 < t < t_5$ where

$$i_p(t) = I_i - \frac{V_{DC}}{L_r}(t - t_3). \quad (9.95)$$

This increases the duration of the interval $t_5 - t_3$ and decreases the effective value of the duty cycle, D_e , of the pulses in the transformer secondary which finally decreases the range of the output voltage variations.

9.7.1.5 Interval T_{4-5} ($t_4 \leq t \leq t_5$)

At the instant t_4 a positive pulse turns on the transistor M_2 . If C_2 is discharged during the previous interval, this turning on occurs at zero voltage. Therefore, in this interval the diagonal transistors, M_2 and M_3 , are on (Fig. 9.43e) causing the primary current to change direction and its value is approximately determined by (9.95). Within this interval both of the rectifying diodes are on and the secondary of the transformer is short-circuited ($V_s = 0$). At the instant t_5 , when the primary current is $-I_1$, one of the rectifying diodes is turned off and the secondary voltage is $V_s = V_{DC}/n$.

After t_5 , the transfer of energy to the load is the same as in a conventional PWM connection. In fact, the interval after t_5 is analogous to interval T_{0-1} , because the new cycle, with reference to the secondary, begins at instant t_5 . The rectified voltage at the output is equal to the mean value of the secondary voltage, i.e.,

$$V_O = \frac{1}{T/2} \int_0^{T/2} V_s(t) dt = \frac{1}{T/2} \int_0^{D_e(T/2)} V_{DS}/n dt = D_e V_{DC}/n, \quad (9.96)$$

where D_e is the effective value of the duty cycle of the pulses in the transformer secondary.

The general characteristics of the phase shift PWM converters can be summarized as follows:

- The transistors are turned on or off at zero voltage which reduces significantly the dynamic dissipation.
- The elements for the preparation of soft switching are the parasitic elements of the already used components so the negative effects of the parasitic elements are eliminated.
- By reducing the voltage and current variations the reduction of the generated interference (EMI and RFI) is accomplished.
- The maximum voltage across transistors is equal to the input voltage, as with the conventional circuits. The maximum currents in the bridge are higher than those in conventional circuits, but they are considerably lower than the currents of the resonant topologies.

Example 9.6 The soft switching PWM DC/DC converter (Fig. 9.41) has the following parameters: $V_{DC} = 50$ V, $n = 1.5$, $L_f = 10$ μ H, and $f = 100$ kHz.

- (a) Determine the effective value of a duty cycle so that the output voltage is 20 V.
 - (b) Determine the maximum primary current if its value at the beginning of the period is 1 A.
- (a) The output voltage is (9.96): $V_O = \frac{D_e V_{DC}}{n} \Rightarrow D_e = \frac{n V_O}{V_{DC}} = 0.6$.
 - (b) Primary current increases during the interval T_{0-1} when the transistors M_1 and M_4 , are turned on. This current is the sum of the initial current and the output

current referred to the primary side of transformer (9.87), and its maximum value is reached at the moment $t = t_1$

$$I_{pM} = I_1 + \frac{V_{DC} - V_O}{nL_f} D_e T / 2 = 3.67 \text{ A}$$

9.7.2 Resonant Transitions PWM Converters

The resonant transitions PWM converters are made by modifying the corresponding topologies of the conventional PWM converters in order to provide the soft switching of the switching element. This has been accomplished by the resonant elements, $L_r C_r$, and one auxiliary switch. The resonant capacitor is connected in parallel with the main switch, whereas the coil is in series with the auxiliary switch. This ensures a zero voltage transition and the abbreviated notation for this type of converters is *ZVT-PWM (Zero Voltage Transition-PWM)*.

Practically, each conventional PWM topology can be modified into a soft switching circuit. This will be explained here taking the example of a voltage booster (Fig. 9.44). The main switch is the MOS transistor M . Its internal diode is D_M . The auxiliary switch is M_1 .

The diode D_1 limits the maximum voltage of the transistor M_1 to the value of the output voltage, V_O . It is assumed, like with the conventional converters, that the inductance L_f and the capacitance C_f are sufficiently large to consider the current through L_f and the voltage across C_f in the quasi-static states constant. In other words, it may be assumed that the converter is fed by a constant current source I_{DC} and that the load is a constant voltage source. In the present analysis, the timing diagrams (Fig. 9.45) and the equivalent circuits in the characteristic time intervals (Fig. 9.46) will be used.

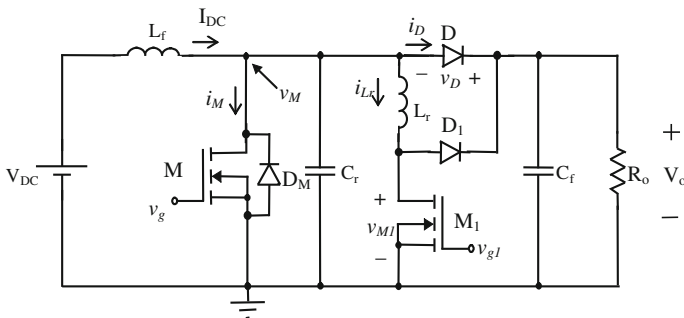


Fig. 9.44 A ZVT-PWM boost converter based on the soft switching

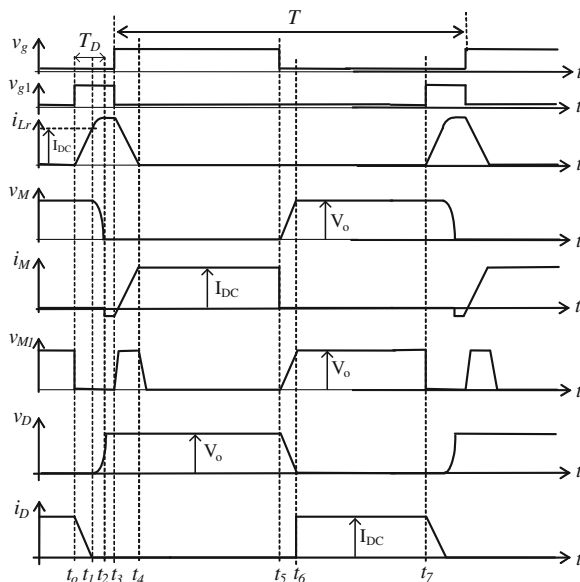


Fig. 9.45 The characteristic waveform of a PWM resonant boost converter

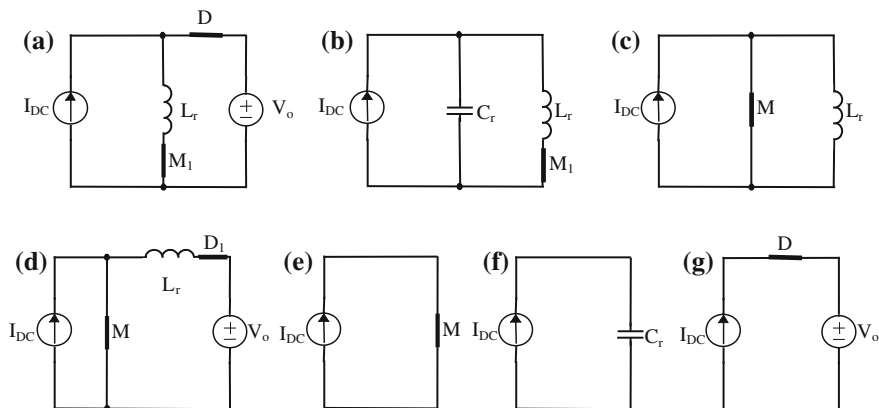


Fig. 9.46 The equivalent circuits corresponding to different time intervals. (a) T_{0-1} , (b) T_{1-2} , (c) T_{2-3} , (d) T_{3-4} , (e) T_{4-5} , (f) T_{5-6} , (g) T_{6-7}

9.7.2.1 Interval T_{0-1} ($t_0 \leq t \leq t_1$)

Until $t = t_0$ both transistors are off ($V_g = V_1 = 0$) and the diode D is on. At $t = t_0$, $V_{g1} = V_{GG}$ and M_1 is turned on. The resonant coil is then connected in parallel with the output (Fig. 9.46a). Therefore, the current through it increases linearly:

$$I_{Lr}(t) = \frac{V_0}{L_r} t. \quad (9.97)$$

The current through the diode D is $i_D = I_{DC} - i_L$. At the instant t_1 , when $i_D(t_1) = 0$, the diode is turned off and ends this interval which is determined by

$$T_{0-1} = t_1 - t_0 = I_{DC} L_r / V_0. \quad (9.98)$$

The diode D is turned off at small variations dv/dt and di/dt . Therefore, the interval T_{0-1} is the interval of the soft turning off of the diode D .

9.7.2.2 Interval T_{1-2} ($t_1 \leq t \leq t_2$)

The turned off diode separates the output from the resonant coil. Since M is turned off, an oscillatory circuit is formed in parallel with it (Fig. 9.46b). The capacitor C_r discharges and the current through L_r continues to increase (Fig. 9.45). The character of these variations is harmonic.

This interval ends at the instant t_2 when the voltage across C_r drops to zero, i.e., when $V_M(t_2) = 0$. It can be shown that this interval is equal to one quarter of the cycle of oscillation of the oscillatory circuit, i.e.,

$$T_{1-2} = t_2 - t_1 = \frac{\pi}{2} \sqrt{L_r C_r}. \quad (9.99)$$

9.7.2.3 Interval T_{2-3} ($t_2 \leq t \leq t_3$)

In this interval the internal diode D_M of the transistor M is on, so $V_M = V_d = 0$, which ensures the zero voltage turning on of the transistor M . This condition is ensured at the end of the previous interval, so it could be that $T_{2-3} = 0$. Nevertheless, $T_{2-3} > 0$ and it is a standby interval which warrants that the capacitor C_r is discharged to zero before the transistor M is on. Namely, the delay in turning on the transistor M compared to the transistor M_1 should be

$$T_D \geq T_{0-1} + T_{1-2} = \frac{I_{DC} L_r}{V_0} + \frac{\pi}{2} \sqrt{L_r C_r}. \quad (9.100)$$

Equation (9.100) is the condition for soft switching. This delay time is not load dependent as it was for the phase shift PWM converters.

If this condition is met at the minimum output voltage, it is valid for the whole range of variations of V_0 . The time T_D should be much shorter than the cycle of the control pulses if the ratio V_0/V_{DC} is not to be degraded.

9.7.2.4 Interval T_{3-4} ($t_3 \leq t \leq t_4$)

The transistor M_1 is off, whereas M is on (Fig. 9.46d). The diode D is on so $V_{M1} = V_0$. The current of the resonant coil decreases linearly and at t_4 drops to zero. Meanwhile, the energy accumulated by L_r is transferred to the load. The interval T_{3-4} is not a critical parameter because it is shorter than the time of conduction of the transistor M .

9.7.2.5 Interval T_{4-5} ($t_4 \leq t \leq t_5$)

At an instant t_4 the diode D_1 is turned off. The diode D is off and it separates the main switch from the output (Fig. 9.46e). This interval is equal to that in a conventional converter (voltage booster).

9.7.2.6 Interval T_{5-6} ($t_5 \leq t \leq t_6$)

At the beginning of this interval the voltage V_g falls to zero and the transistor M is turned off. The resonant capacitor is charged by the current I_{DC} (Fig. 9.46f) and

$$V_M(t) = \frac{I_{DC}}{C_r} t. \quad (9.101)$$

This interval is ended by turning on of the diode D at $V_M(t_0) = V_0$, giving:

$$T_{5-6} = \frac{C_r I_{DC}}{V_0}. \quad (9.102)$$

9.7.2.7 Interval T_{6-7} ($t_6 \leq t \leq t_7$)

The transistors M and M_1 and the diode D_1 are off, whereas the diode D is on (Fig. 9.46g), transferring the energy from the input to the load. This interval is equal to that in a conventional voltage booster.

The general characteristics of the ZVT-PWM voltage boosters are summarized as follows:

- The soft switching of the main transistor M and the diode D is realized, but the same is not valid for the auxiliary transistor. However, it proceeds at considerably lower power levels and thus it is not critical.
- The maximum voltages across the transistors and diodes are the same as in the conventional converters.

9.8 Control Circuits of Resonant Converters

The analysis presented in the preceding sections shows that the output voltage of the majority of the topologies of resonant converters is dependent on the switching frequency. For this reason the switching frequency is the basic control parameter of these converters, and the main part of the control circuitry is the voltage-to-frequency converter, often called the voltage controlled oscillator (abbreviated VCO). Together with the error amplifier, the VCO is in the feedback loop between the output and the control input of the switching elements of the converter.

The other group of control circuits operates at a constant frequency, but with a variable phase shift of the control pulses of different phases. The feedback elements of these control circuits control the time shifts of the pulses that regulate the switching elements of the resonant converters.

A wide selection of integrated circuits developed for the purpose of controlling the resonant converters are available on the market. All these circuits consist of standard blocks like the control circuits of PWM converters. These blocks include error amplifier, auxiliary oscillator, voltage reference source, logic block, and protection block. The standard functional inputs and outputs are: different output options, soft start, shutdown, dead time control, etc.

The peculiarities of some of the control circuits are related to the specific topologies of the converters. Peculiar in that respect are the control circuits of the converters based on resonant switches having one quasi-stable interval constant and the other variable. For this reason these circuits, in addition to the VCO, comprise a one-shot (monostable) multivibrator MM (Fig. 9.47) which determines the constant duration of control pulses. There are two groups:

- control circuits of ZCS resonant converters (Fig. 9.47a), and
- control circuits of ZVS resonant converters (Fig. 9.47b).

The output voltage of a converter based on resonant switches depends on the quasi-resonant interval τ_{QR} and the control pulse frequency. The quasi-resonant interval is kept constant during:

- the conduction time (t_{on}) of the switching element in ZCS converters, and
- the nonconduction time (t_{off}) of the switching element in ZVS converters.

The difference between the fraction of the output voltage kV_0 ($0 < k < 1$) and the voltage reference V_{REF} is amplified by the error amplifier.

The VCO is a generator of short pulses, like the one shown in Fig. 5.5, where the current charging the capacitor is a function of voltage V_{EA} at the output of the error amplifier (EA) (Fig. 9.47).

Since the VCO triggers the one-shot multivibrator, the frequency of pulses at the output of MM is equal to the VCO frequency

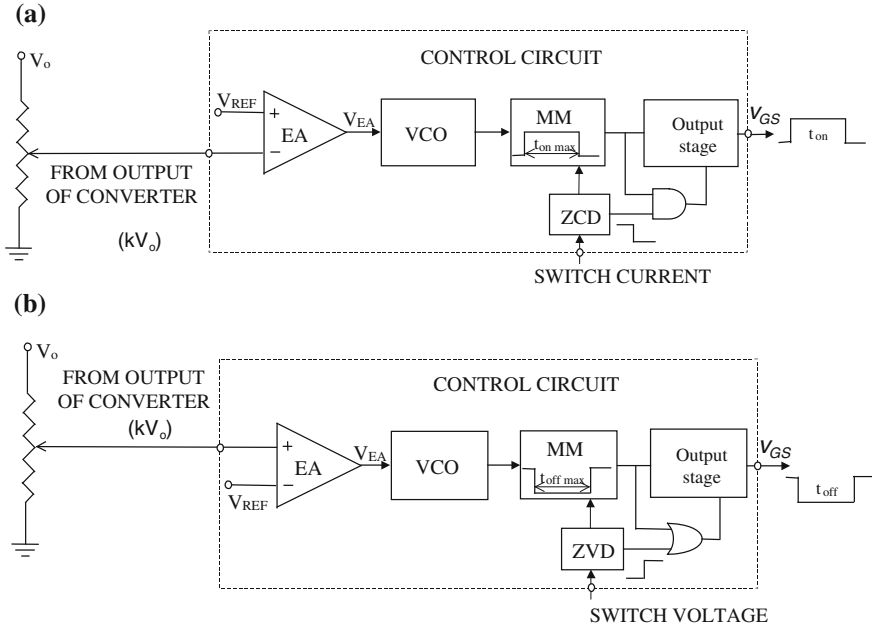


Fig. 9.47 The basic blocks of the control circuits of ZCS (a) and ZVS resonant converters (b). EA error amplifier, VCO voltage controlled oscillator, MM monostable (one-shot) multivibrator, ZCD and ZVD are zero current and zero voltage detectors, respectively.

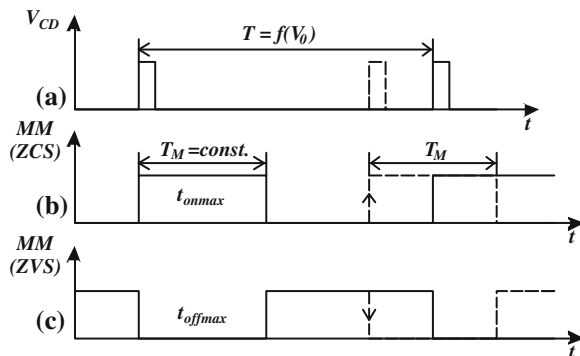
$$f \approx \frac{I(V_{EA})}{CV_h}, \quad (9.103)$$

where C and V_h are the capacitor and voltage hysteresis of the Schmitt trigger in the VCO (Fig. 5.5), and I_{EA} is the current charging the capacitor C programmed by the output of the error amplifier. The constant quasi-stable interval of these pulses is determined by the quasi-stable interval of MM (Fig. 9.48). The MM circuits of the ZCS and ZVS converters are the same except for the outputs which are complementary. The quasi-resonant intervals τ_{QR} , as shown in Sect. 9.5, are dependent on the input voltage V_{DC} and the load current I_0 . In the ZCS converters the maximum quasi-resonant interval τ_{QR} is at the minimum V_{DC} and the maximum I_0 , whereas in the ZVS at the maximum V_{DC} and the minimum I_0 . Therefore, the end of the constant part of the control pulse is synchronized with the zero crossing of current or voltage (Fig. 9.48).

The circuits for the detection of the zero crossing of current (Fig. 9.47a) or voltage (Fig. 9.47b) are thus a constituent part of the control circuitry. The elements of the one-shot multivibrator are so designed that its quasi-stable interval is $T_M > \tau_{QR\max}$, i.e.,

- $T_M = t_{on\max}$ for control circuits of ZCS converters, and
- $T_M = t_{off\max}$ for control circuits of ZVS converters.

Fig. 9.48 The voltage waveforms at the outputs of VCO (a) and MM control circuit having constant t_{on} (b) and t_{off} (c) of the switching element



Upon detection of a zero crossing of the current, at the output of an AND circuit one obtains the low level of the control pulse in the ZCS converters. The high level of the control pulse in the ZCS converters is obtained when the voltage across the switching element crosses zero. Therefore, the beginning of the constant interval of the control pulse is synchronized with the beginning of the quasi-stable interval of MM, and its end is synchronized with the zero crossing of the current or voltage of the switching element.

The block of the output stage has to provide a sufficiently powerful drive of the switching element. Since the switching elements are usually MOS transistors, the output stage charges and discharges the input capacitance of the MOS transistor $C_{ISS} = C_{GS} + C_{GD}$. C_{ISS} of powerful MOS transistors ranges from several hundred up to several thousand pF. The rise and fall times of the control pulses of the high frequency resonant converters are of the order of several hundred picoseconds up to 1 ns. Therefore, the output stage has to provide quite high currents for charging and discharging of C_{ISS} , up to the order of several A, so usually the bipolar transistors connected in push-pull configuration are used at the output. It should be emphasized that the charging and discharging current pulses are very short (shorter than 1 ns), so the average value of the output current is negligible.

A constituent part of the output stage is the enable circuit of the output transistors. This circuit is driven by the output signals of the auxiliary blocks, such as soft start signals, under voltage control, shutdown control, etc.

9.8.1 Integrated Circuit Family UCx861-8

The UCx861-8 family of integrated circuits is manufactured by *Unitrode*. Code x denotes the operating temperature range:

- $x = 1$: $-55\text{ }^{\circ}\text{C} < T_A < 125\text{ }^{\circ}\text{C}$,
- $x = 2$: $-25\text{ }^{\circ}\text{C} < T_A < 85\text{ }^{\circ}\text{C}$,
- $x = 3$: $0\text{ }^{\circ}\text{C} < T_A < 70\text{ }^{\circ}\text{C}$.

Codes 861–868 denote the specific application depending on whether the controlled object is:

- ZCS or ZVS quasi-resonant converters,
- one or two transistors converters,
- DC/DC or DC/AC converters.

The block diagram of the control circuit of the family UCx861 to UCx868 is shown in Fig. 9.49. The basic blocks are: the error amplifier EA, the voltage controlled oscillator VCO, the monostable multivibrator MM, the zero voltage/current detector ZD, and the output stage together with control logic. The resistors R_a , R_m , and the capacitor C_v are connected at the input of the VCO. The resistors R_m and R_a determine the currents of the internal current generators of the VCO required for charging capacitor C_v . These currents are dependent on the output voltage of the error amplifier. If this voltage is lower than 0.6 V (turn on voltage of a diode), VCO operates at the minimum frequency determined by

$$f_{\min} = \frac{\Delta V_{EA}}{R_m C_v} \approx \frac{3.6}{R_m C_v}. \quad (9.104)$$

Then the current generator containing R_a is off. The maximum frequency of the VCO corresponds to the maximum voltage of the error amplifier, $5 \text{ V} - V_d$, is determined by

$$f_{\max} = \frac{3.6}{(R_a || R_m) C_v}. \quad (9.105)$$

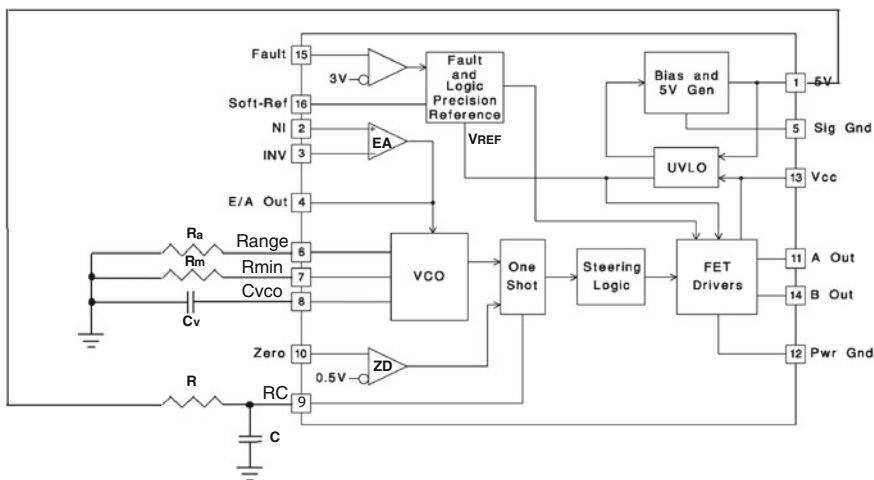


Fig. 9.49 Block diagram of the control circuits of family UCx861 to UCx868, including the external timing elements

The total variation of the frequency, or the range of the frequency control, is

$$\Delta f = f_{\max} - f_{\min} = \frac{3.6}{R_a C_V}. \quad (9.106)$$

Therefore, R_m determines the minimum frequency of the VCO and R_a determines the range of its variation. The maximum frequency is limited to 1 MHz.

The error amplifier is supplied by the internal 5 V supply. The maximum variation of the output voltage is approximately $\Delta V \approx 5 \text{ V} - 2V_D \approx 3.6 \text{ V}$, and on the basis of (9.107)

$$\Delta V_{EA}/\Delta f = R_a C_V. \quad (9.107)$$

The sensitivity of the zero current/voltage detector of the comparator, ZD, is 0.5 V. When the voltage at the detecting terminal drops below 0.5 V, the ZD comparator cuts the quasi-stable interval of the monostable multivibrator MM, determined by the time constant RC . The MM circuit contains two internal comparators having thresholds $V_{Z1} \approx 1.4 \text{ V}$ and $V_{Z2} \approx 3.2 \text{ V}$ so that the maximum quasi-stable interval is $T_{M\max} = RC$ and the minimum $T_{M\min} = 0.3RC$ (Table 9.1).

The auxiliary blocks of the integrated circuits of the family UCx861-8 are:

- internal power supply 5 V,
- the under voltage lock out block (UVLO),
- the block of error detection and reference voltage source.

Their functions are the same as those of the PWM control circuits described in Chap. 6.

There are, of course, integrated control circuits of the resonant converters by other manufacturers. By the structure, all these circuits are similar, but they differ in their functional possibilities. For instance, *Philips* circuit NE5580 can be used for the control of the majority of resonant topologies. The maximum frequency is 10 MHz.

Table 9.1 Options in the family of integrated circuits UCx861-8

Integrated circuit	Constant time	UVLO thresholds (V)	Outputs
UC1861	t_{off}	16.5/10.5	Complement
UC1862	t_{off}	16.5/10.5	Paralleled
UC1863	t_{off}	8/7	Complement
UC1864	t_{off}	8/7	Paralleled
UC1865	t_{on}	16.5/10.7	Complement
UC1866	t_{on}	16.5/10.5	Paralleled
UC1867	t_{on}	8/7	Complement
UC1868	t_{on}	8/7	Paralleled

9.8.2 Integrated Circuits for Control of Soft Switching PWM Converters

The control pulses of the bridge arms are phase shifted (Fig. 9.50). By varying the phase shift the output voltage is changed directly. The preparation of the soft switching is carried out during the dead time between the pulses of the same arm. The block diagram of this concept is shown in Fig. 9.50. It consists of a standard PWM circuit and a logic block for generating four-phased signals.

The dead times of the right t_{DR} and left t_{DL} arms of the bridge are set by the delay lines. The four-phased signals are obtained by one T flip-flop and two exclusive OR circuits (Fig. 9.50).

The outputs of the exclusive OR circuits exist only when the inputs are different. Owing to this the signals of the lines Φ_3 and Φ_4 are delayed compared to the changes of the signals Φ_1 and Φ_2 by the time DT , where D is the duty cycle and T is the cycle of pulses at the output of the single-phase PWM circuit. The effective value of the duty cycle D_e is, owing to the dead times, somewhat smaller than D .

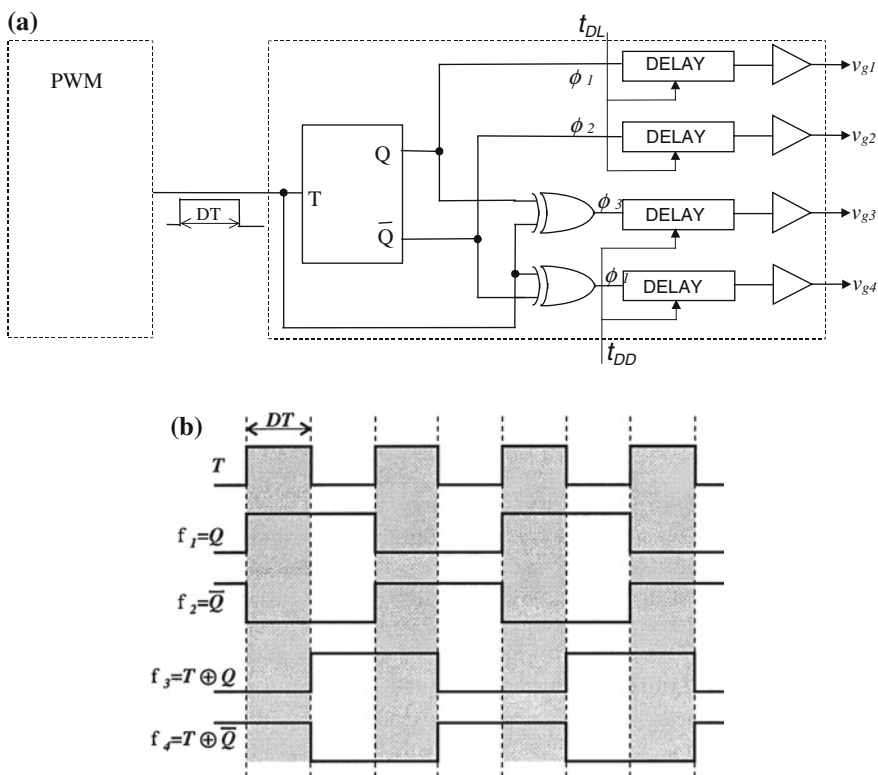


Fig. 9.50 The block diagram of the control circuit of the phase shift bridge converter (a) and the waveforms of the signals at the inputs of the logic circuit and delay lines (b)

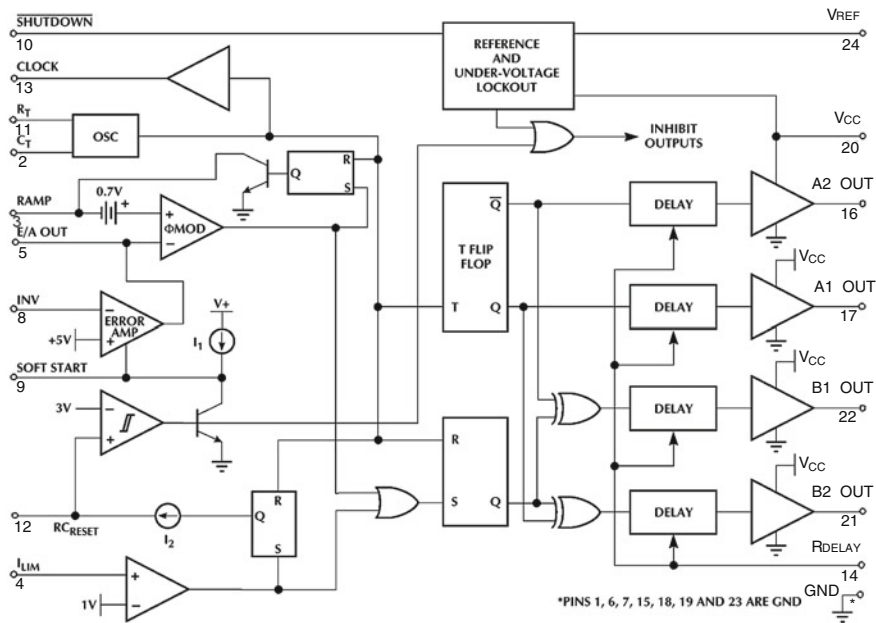


Fig. 9.51 Block diagram of control circuit ML 4818

Unitrode is the manufacturer of the integrated circuit family UCx875-8 developed for control of the phase shift PWM converters. Dead times are generated by the delay time blocks. These delays are independently programmable.

Microlinear is the manufacturer of the integrated circuit ML4818 for control of the phase shift bridge converters (Fig. 9.51) which operates at frequencies up to 500 kHz. The BiCMOS option of this circuit ML4828 can operate at frequencies up to 1 MHz. Except for the output logic block for generating the four-phased output, other blocks are available as standard PWM control circuits.

Problems

1. The circuit shown in Fig. 9.10a has the parameters $V_{DC} = 100$ V, $R_L = 5$ Ω , $C_r = 0.5$ μ F, $L_r = 10$ μ H, and $f = 75$ kHz. Determine the output voltage of the converter.
2. The circuit shown in Fig. 9.10a has the parameters $V_{DC} = 50$ V and $R_L = 5$ Ω . The desired output voltage is $V_0 = 20$ V and the switching frequency $f = 75$ kHz. Select suitable values of L_r and C_r .
3. The circuit shown in Fig. 9.16a has the parameters $V_{DC} = 100$ V, $R_L = 5$ Ω , $C_r = 0.1$ μ F, $L_r = 25$ μ H, and $f = 120$ kHz. Determine the output voltage of the converter.
4. The circuit shown in Fig. 9.16a has the parameters $V_{DC} = 15$ V, $R_L = 15$ Ω , $n = 1$, and $f = 120$ kHz. The desired output voltage is 20 V. Determine suitable values for L_r and C_r .

- 9.5. Determine the output voltage of a series–parallel resonant DC/DC converter shown in Fig. 9.18: if $V_{DC} = 80$ V, $L_r = 40$ μ H, $C_r = C_P = 0.03$ μ F, $R_L = 10$ Ω , $n = 2$, and $f = 150$ kHz.
- 9.6. The parameters of the ZCS-QR converter shown in Fig. 9.30 are $V_{DC} = 12$ V, $C_r = 0.3$ μ F, $L_r = 4$ μ H, $I_0 = 5$ A, and frequency $f = 100$ kHz. Determine the output voltage, the maximum transistor current, and the maximum frequency.
- 9.7. The following parameters of a ZVS-QR forward converter shown in Fig. 9.34 are known: $V_{DC} = 20$ V, $L_r = 4$ μ H, $C_r = 0.1$ μ F, $I_0 = 5$ A, and $f = 25$ kHz. Determine:
 - (a) the output voltage, and
 - (b) the maximum inductor current and the capacitor voltage.
- 9.8. A ZVS resonant DC/AC converter shown in Fig. 9.39a has the following parameters: $V_{DC} = 20$ V, $L_r = 5$ μ H, $C_r = 0.05$ μ F, and $I_0 = 2$ A. Determine the expressions for the inductor current and the capacitor voltage.
- 9.9. The soft switching PWM DC/DC converter (Fig. 9.41) has the following parameters: $V_{DC} = 48$ V, $n = 2$, $L_f = 10$ μ H, $f = 100$ kHz, $C_1 = C_2 = C_3 = C_4 = 0.01$ μ F, and $D_e = 0.5$.
 - (a) Determine the output voltage.
 - (b) Determine the maximum primary current if its value at the beginning of the period is 1.2 A.
 - (c) Determine the minimum value of the interval $t_{D3,4}$ so the capacitor C_3 is discharged to zero voltage.

Chapter 10

Introduction to Multilevel Converters

10.1 Basic Characteristics

Multilevel converters have found an important position among applications as high-power converters. Also, they are widely used in renewable energy sources where multilevel converters appear as a link between renewable sources, such as wind, fuel cells, photovoltaic modules from one side and high-power loads from the other side. Power converters for high-power AC motors, systems for reactive power compensation, Flexible Alternative Current Transmission Systems (FACTS) devices and inverters in tracking vehicles have become typical applications in which multilevel converters are used.

The main advantages of multilevel converters compared to the traditional topologies are [1]:

- smaller harmonic distortion,
- lower voltage stress on semiconductor components,
- lower EMI,
- higher efficiency,
- the possibility of converter implementation without magnetic material components (transformers, inductors,...).

In addition to the presented advantages, multilevel converters have disadvantages such as:

- the need to use a larger number of semiconductor components,
- realization of voltage balance on the capacitors in various converter topologies,
- some multilevel inverter topologies require power supply from mutually isolated DC sources.

A general trend in power electronics is increasing the switching frequency in power converters. Switching frequency is increased for two basic reasons. The first one is harmonic distortion reduction (simple filtration) and the second is size

reduction of passive components. On the other hand, increasing the switching frequency leads to higher switching losses, which is especially marked in switches used at higher voltages. In order to reduce the voltage stress of switches, one may use instead a series connection two or more switches, thus dividing the applied voltage to a number of series connected switches. The inverter branch, where the switch is replaced with two switches connected in series is shown in Fig. 10.1 [2].

This connection sets a number of problems related to control of switches that should be addressed:

- Static and dynamic voltage sharing on the switches. From the standpoint of the dynamic voltage balance, it is necessary that both switches commute at the same moment. Otherwise, the switch that is turned off faster would have to withstand all voltage.
- Total dv/dt , generated during the commutation of the series connected switches is equal to the sum of dv/dt values generated by each switch. Thus, a significant dv/dt value can have unwanted effect to low-voltage circuits, and it becomes necessary to apply additional protection from EMI.
- From the viewpoint of voltage control, an increased number of switches does not give a greater freedom in the selection of voltage levels, because the series connected switches must behave like one switch. The voltage at the point A is V_{DC} or 0, and the harmonic that appears at the switching frequency has a significant value.
- Increasing the number of series, connected switches does not solve the problem, actually dv/dt effect becomes more expressed and complicates the control of series connected switches.

The idea is to use the elements for balanced distribution of voltage stress on switches, instead of simultaneously turning on and off the series connected switches. A branch of an inverter bridge with a capacitive voltage divider and coupling diodes is shown in Fig. 10.2. Depending on the state of the switch, the number of voltage levels in the point A is increased by one. If an internal switch is

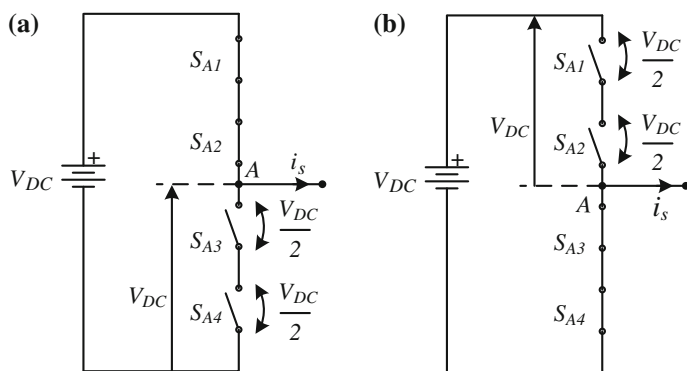
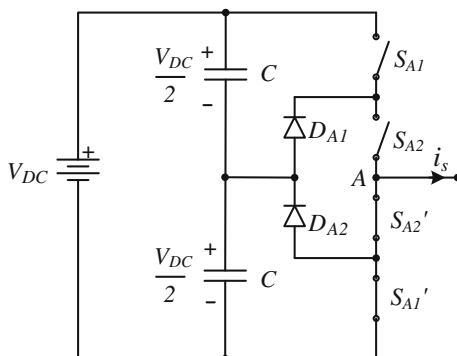


Fig. 10.1 The inverter branch, where the switch is replaced with two switches connected in series, when two upper switches are closed (a), and when two lower switches are closed (b)

Fig. 10.2 Three-level converter leg with a capacitive voltage divider and clamping diodes



turned on (depending on the current, this may be S_{A2} or S'_{A2}), and the external switch S_{A1} or S'_{A1} is turned on, then $V_A = V_{DC}/2$. In dependence of the state of the switches, the point A can be in one of the three voltage levels 0, $V_{DC}/2$ and V_{DC} . Whenever $V_A = V_{DC}/2$, electric current flows through a capacitor. If the current is bilateral and equally flows through the both capacitors, a voltage balance is maintained and the voltage across the capacitors is approximately $V_{DC}/2$. However, if the current i_s is unilateral, there is a voltage imbalance and the voltages on the capacitors are not at the desired value.

The maintenance of voltage balance on capacitive voltage dividers is one of the requirements that must be implemented through an appropriate converter control. By applying proper control techniques for the topology as shown in Fig. 10.2, only one pair of switches is turned on for every half-period. Voltage V_A changes between 0 and $V_{DC}/2$ during one-half of a period, and between $V_{DC}/2$ and V_{DC} during the other half of the period. With this control strategy, a change of the output voltage is achieved by one pair of switches for one half-period and by another pair of switches for the other half-period.

Similar result can be achieved if instead of capacitive voltage divider, only one “flying” capacitor is used (Fig. 10.3). In this topology, it is not necessary to use clamping diodes. At the same time, two inner or two outer switches must not be turned on. The capacitor is short circuited (two inner switches are turned on), or a voltage imbalance appears on the capacitor and high current flows through the closed switches (two outer switches are turned on). The permissible states of the switches for the converter topology presented in Fig. 10.3 are shown in Fig. 10.4. For the circuit shown in Fig. 10.3, voltage balance is automatically set to $V_{DC}/2$. Also, the switches (S_{A1} , S'_{A1}) and the switches (S_{A2} , S'_{A2}) are not turned on and turned off at the same time, so the maximum dv/dt of the converter leg shown in Fig. 10.3 is equal to dv/dt of one switch.

By an analogous approach, a four-level converter leg with clamping diodes (Fig. 10.5a) and a flying capacitor (Fig. 10.5b) can be realized. In this case, the output voltage levels are 0, $V_{DC}/3$, $2V_{DC}/3$, and V_{DC} .

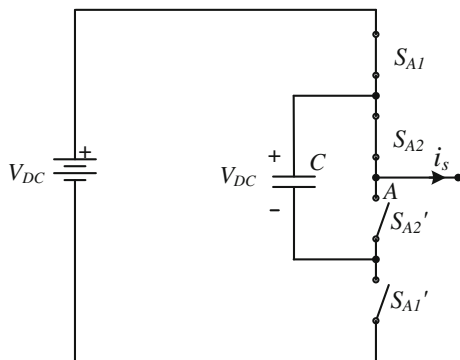


Fig. 10.3 Three-level converter leg with a flying capacitor

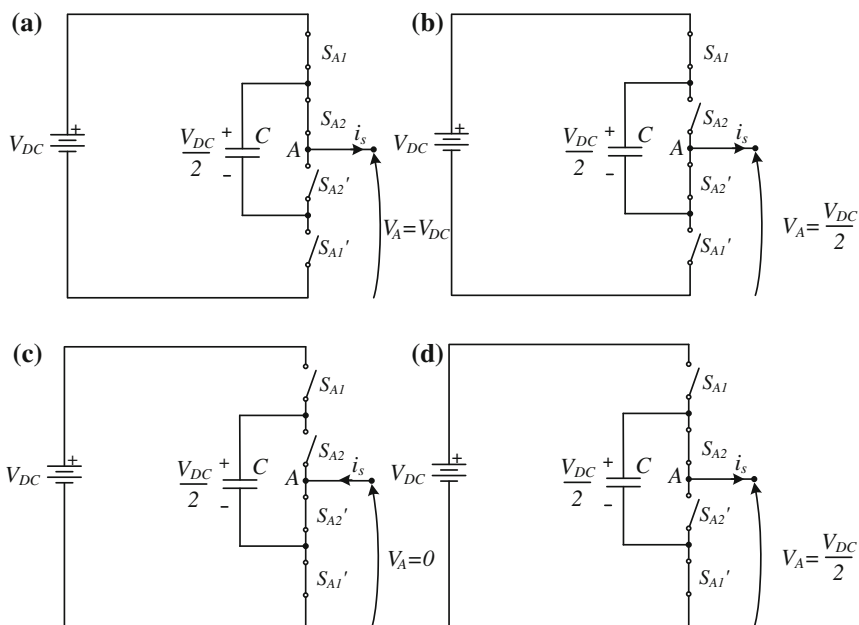


Fig. 10.4 Permissible states of switches in a three-level converter leg with a flying capacitor (a, b, c and d)

The reasons for the introduction and implementation of multilevel converters are described in Sect. 10.1. A further description of these converters follows in this chapter. Multilevel conversion is used in different types of conversion, AC/DC, DC/AC, DC/DC, and AC/AC, thus the corresponding types of multilevel converters are distinguished.

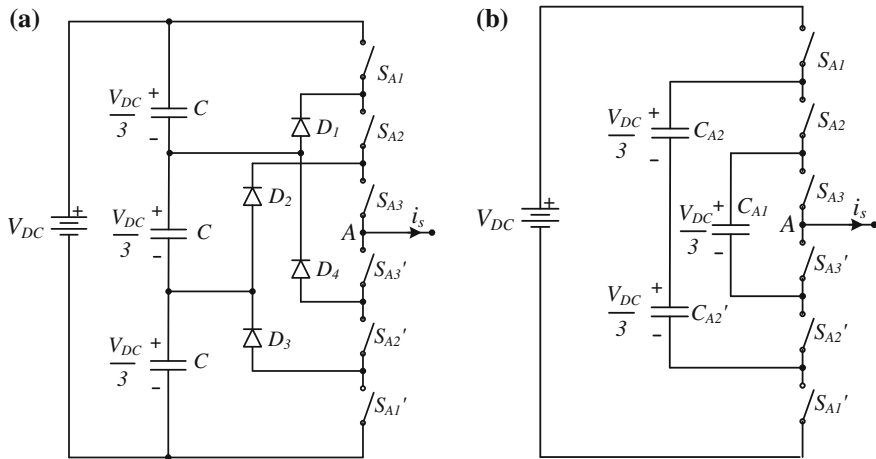


Fig. 10.5 Four-level converter leg with capacitive voltage divider and clamping diodes (a) and flying capacitors (b)

10.2 Multilevel DC/DC Converters

Multilevel DC/DC converters are used in converters where the input is DC voltage, while a higher DC voltage is required at the output, which cannot be achieved by the standard DC/DC boost converter. Also, multilevel DC/DC converters are commonly used as interfaces between primary low-voltage DC sources, such as photovoltaic modules, fuel cells, batteries or superconducting magnetic energy storages (SMES) and high-voltage multilevel inverters which are used as drive converters for high-power AC motors, or for connection to electrical grid [3]. In this application, multilevel DC/DC converter is used for balance of DC voltages at the multilevel inverter input and in this way complex control of multilevel inverter for this reason is avoided.

An important application of these converters are renewable energy sources. On the other hand, the participation of renewable energy sources in total produced electrical energy is increasing.

Another challenge is the transformer-less realization of a multilevel DC/DC converter with a significant ratio between the output and the input voltage. A multilevel boost DC/DC converter is shown in Fig. 10.6 [1]. The basis of this converter is a transformer-less conventional boost DC/DC converter, while the increase of the output voltage is realized by increasing the number of voltage levels at the output. The output voltage depends on the number of the output voltage levels (n) and is equal to nV_{o1} ($V_o = nV_{o1}$) (Fig. 10.6). Operating principle of the converter from Fig. 10.6 can be explained through the example of a four-level boost DC/DC converter (Fig. 10.7). For simplicity, we will assume that the duty factor of the switch S is equal to 0.5. There are two intervals in a single operating period of the converter, as shown in Fig. 10.6.

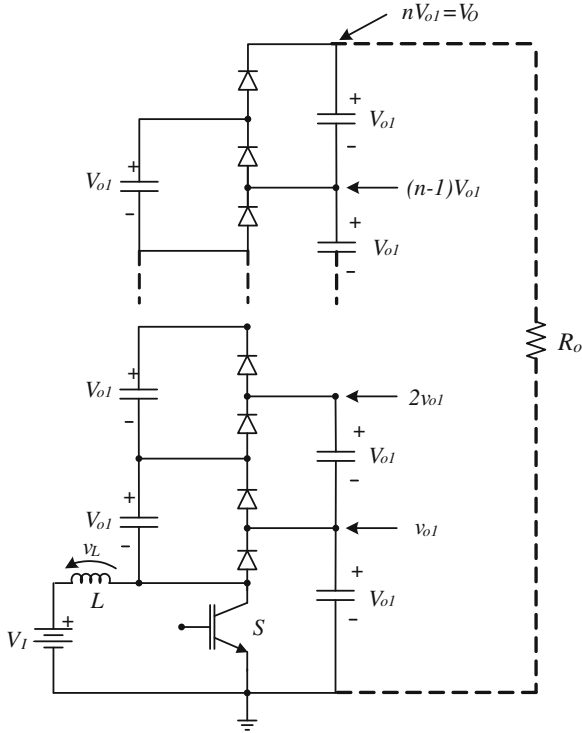


Fig. 10.6 Multilevel boost DC/DC converter [1]

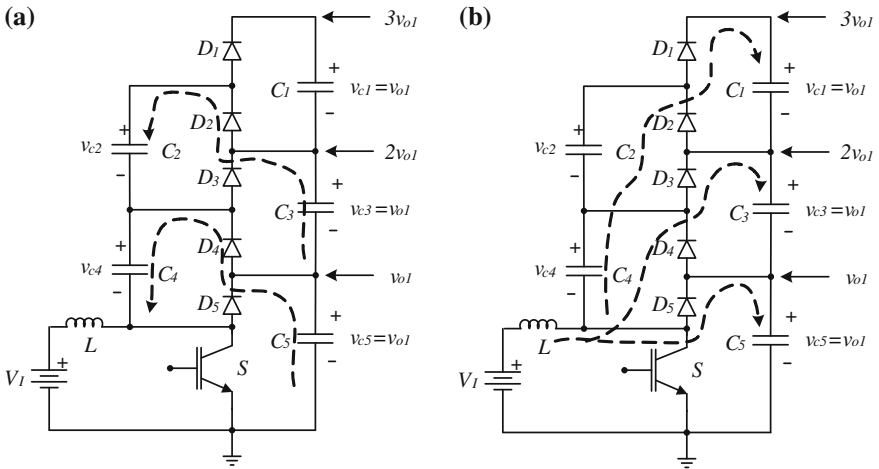


Fig. 10.7 Four-level boost DC/DC converter for switched-on state (a) and for switched-off state (b)

10.2.1 Time Interval: $nT < t < nT + DT$, $n = 0, 1, 2, \dots$

In this time interval, the switch S is turned on. The negative electrode of the capacitors C_4 and C_5 are at the same voltage potential. The inductor L is connected to V_I and accumulates energy from the primary source. Also, during that period voltage becomes balanced between the capacitors in the circuit. If the voltage on the capacitor C_5 (v_{C5}) is higher than the voltage on the capacitor C_4 (v_{C4}), the diode D_5 is turned on and C_5 clamps C_4 's voltage across the diode D_5 and the switch S . Also, if the voltage $v_{C5} + v_{C3}$ is higher than $v_{C4} + v_{C2}$, the diode D_2 is turned on and the capacitors C_5 and C_3 clamp the capacitors C_2 and C_4 through the diode D_2 and the switch S (Fig. 10.7a).

10.2.2 Time Interval: $nT + DT < t < (n + 1)T$

The switch S is turned off. The energy accumulated in the inductor L is delivered to the output capacitors. The diode D_5 is turned on and feeds across the source V_I and the inductor L the capacitor C_5 . If the voltage $V_I + v_L + v_{C4}$ (v_L is the voltage at the inductance L) is higher than the voltage $v_{C5} + v_{C3}$, the diode D_3 is turned on and the capacitor C_3 is charged. Analogously, if the voltage $V_I + v_L + v_{C4} + v_{C2}$ is higher than $v_{C5} + v_{C3} + v_{C1}$, D_1 is turned on and C_1 is charged. Turning on the diodes D_5 , D_3 i D_1 is simultaneous.

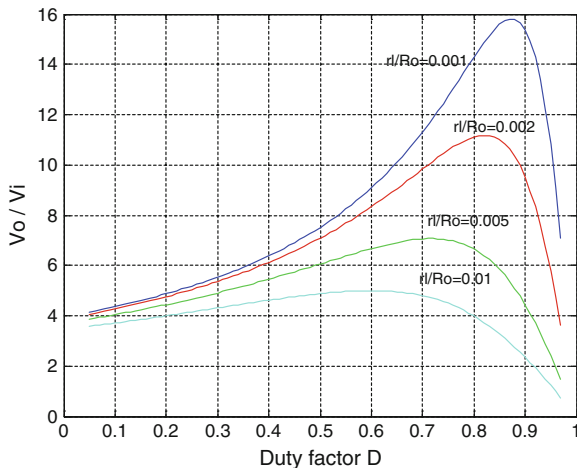
Compared to the conventional transformer-less boost topology of the DC/DC converter, this multilevel topology, besides obtaining a higher output voltage, provides some other benefits. Due to system limitations, and primarily because of losses in the inductance L , the conventional boost DC/DC converter has the ratio V_O/V_I limited to 5. Also, when a higher ratio V_O/V_I is required, the converter comes out of the quasilinear region and enters the nonlinear region. In the multilevel converter shown in Fig. 10.6, the quasilinear region is extended to higher values of the duty factor D , and the desired value of the output voltage V_O can be achieved under optimum converter operating conditions with a duty factor of 0.5. The dependence of the voltage ratio V_O/V_I on the duty factor for different values of r_L/R_o is shown in Fig. 10.8. The resistance r_L is the parasitic resistance of the inductance L and R_o is the load resistance (Fig. 10.6).

Based on the known condition that the average value of voltage on the inductance L is equal to 0, one can write

$$v_L = (V_I - I_L r_L)D + (V_I - i_L r_L - V_{o1})(1 - D) = 0 \quad (10.1)$$

The first term of Eq. (10.1) is valid when the switch S is turned on ($nT < t < nT + DT$), and the second when the switch S is turned off ($nT + DT < t < (n + 1)T$). From (10.1) it can be written

Fig. 10.8 Dependence of voltage ratio V_O/V_I on duty factor for different values of r_L/R_O



$$V_I = I_L r_L + V_{o1}(1 - D) = I_L r_L + \frac{V_O}{N}(1 - D) \quad (10.2)$$

The current I_L is the average value of the current through the inductance L . It can be determined from the condition of equality of the input and the output power

$$\begin{aligned} V_L I_L &= V_O I_O = \frac{V_O^2}{R_O} \\ I_L &= \frac{V_O}{\frac{1-D}{N} R_O} \end{aligned} \quad (10.3)$$

Incorporating (10.3) in (10.2) one obtains

$$\begin{aligned} V_I &= \frac{N V_O}{1 - D} \frac{r_L}{R_O} + \frac{V_O(1 - D)}{N} \\ \frac{V_O}{V_I} &= \frac{1}{\frac{N}{(1-D)} \frac{r_L}{R_O} + \frac{1-D}{N}} \end{aligned} \quad (10.4)$$

Currents through the semiconductor components in the lower levels of the converter are higher than currents in the upper levels of the converter, which is one of the drawbacks of this topology. This is one of the characteristics of this type of multilevel converters, and various modifications of the basic topology are used in order to realize the balance of currents through the switches.

Example 10.1 The four-level DC/DC converter shown in Fig. 10.7 has $V_I = 12$ V, $R_O = 10$ Ω , $r_L = 0.2$ Ω and $D = 0.4$. Determine

- (a) the output voltage, and
- (b) the average value of the inductor current.

- (a) The output voltage can be determined by Eq. (10.4)

$$V_O = \frac{V_I}{\frac{N}{1-D} \frac{r_L}{R_O} + \frac{1-D}{N}} = 42.35 \text{ V.}$$

- (b) The average value of the current i_L can be determined from the condition of equality of the input and the output power and according to Eq. 10.3, it is

$$I_L = \frac{NV_O}{(1-D)R_O} = 28.23 \text{ A.}$$

Multilevel DC/DC converters are also used as interfaces between the DC sources and multilevel inverters in order to achieve uniform voltage distribution on the input capacitors of the inverters. A four-level two-quadrant DC/DC converter is shown in Fig. 10.9 [3]. This converter can operate as a boost or buck depending on whether power flows from the DC source to the inverter or vice versa.

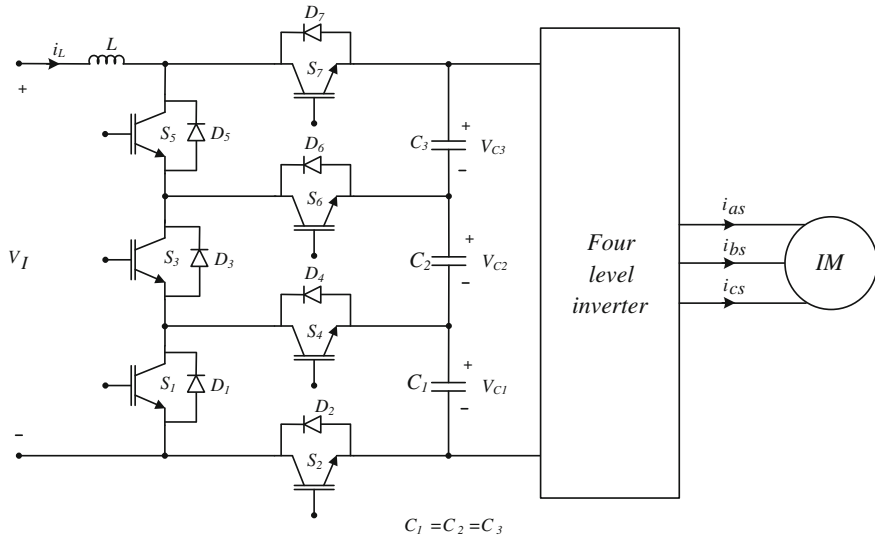


Fig. 10.9 Four-level two-quadrant boost multilevel DC/DC converter connecting DC source and multilevel inverter

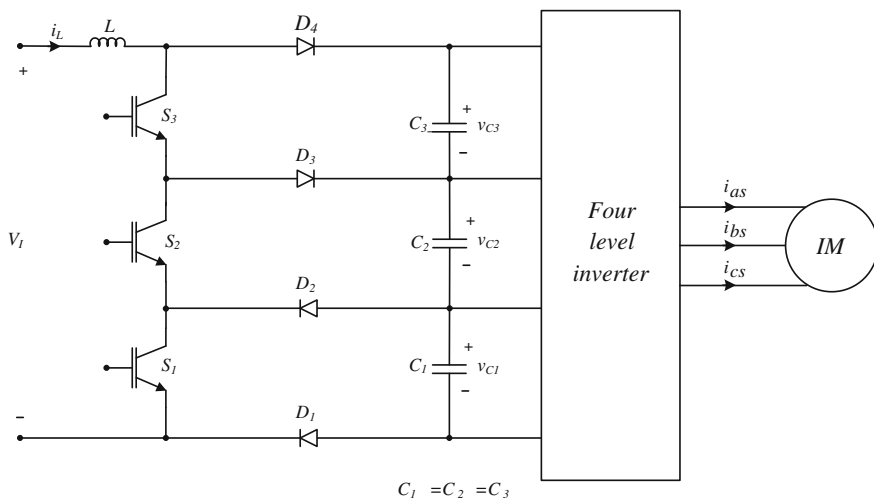


Fig. 10.10 Four-level one-quadrant boost multilevel DC/DC converter connecting DC source and multilevel inverter

In many applications power flow is unidirectional, from the DC source to the load, thus a simpler converter topology can be used (Fig. 10.10) than that shown in Fig. 10.9. Five different states of switches in the converter from Fig. 10.10 are shown in Fig. 10.11. The states 0 and 4 (Fig. 10.11a, e) are typical for a conventional boost DC/DC converter. For the case shown in Fig. 10.11 when an induction motor is the load, the capacitor C_2 tends to discharge, so the state 1 is inserted in the switching sequence to increase voltage on the capacitor C_2 (Fig. 10.11b).

The secondary function of these converters is to balance voltages on the upper and the lower capacitor. This is done in the state 2 (Fig. 10.11c) and the state 3 (Fig. 10.11d). The state 2 or the state 3 is inserted after the state 1 for transition from the state 0 to the state 4, or before the state 1 for transition from 4 to 0. The switching sequence applied during one period is shown in Fig. 10.12. One period in the operation of the DC/DC converter shown in Fig. 10.10 makes control sequences that correspond to the converter transition from the state 0 to 4 and vice versa from the state 4 to 0. The assumption is that during the period T , the state 0 is applied in the interval d_1T , the state 1 in the interval d_2T , the state 2 or 3 in the interval d_3T , and the state 4 in the interval $[1 - (d_1 + d_2 + d_3)]T$. The interval d_2T is increased or decreased depending on how much the voltage on the capacitor C_2 should increase. The interval d_3T is shorter and is used to maintain the voltage balance between the upper and the lower capacitors. The states 2, or 3 will be active depending on whether it is necessary to increase the voltage v_{C1} , or v_{C3} . If it is necessary to increase the voltage v_{C1} , the state 2 would be active.

For a multilevel DC/DC converter, as in the conventional two-level converter, it is necessary to determine the expressions for the output voltage V_o , the average value of current through the inductance L , the ripple of the current $i_L(\Delta i_L)$, and the

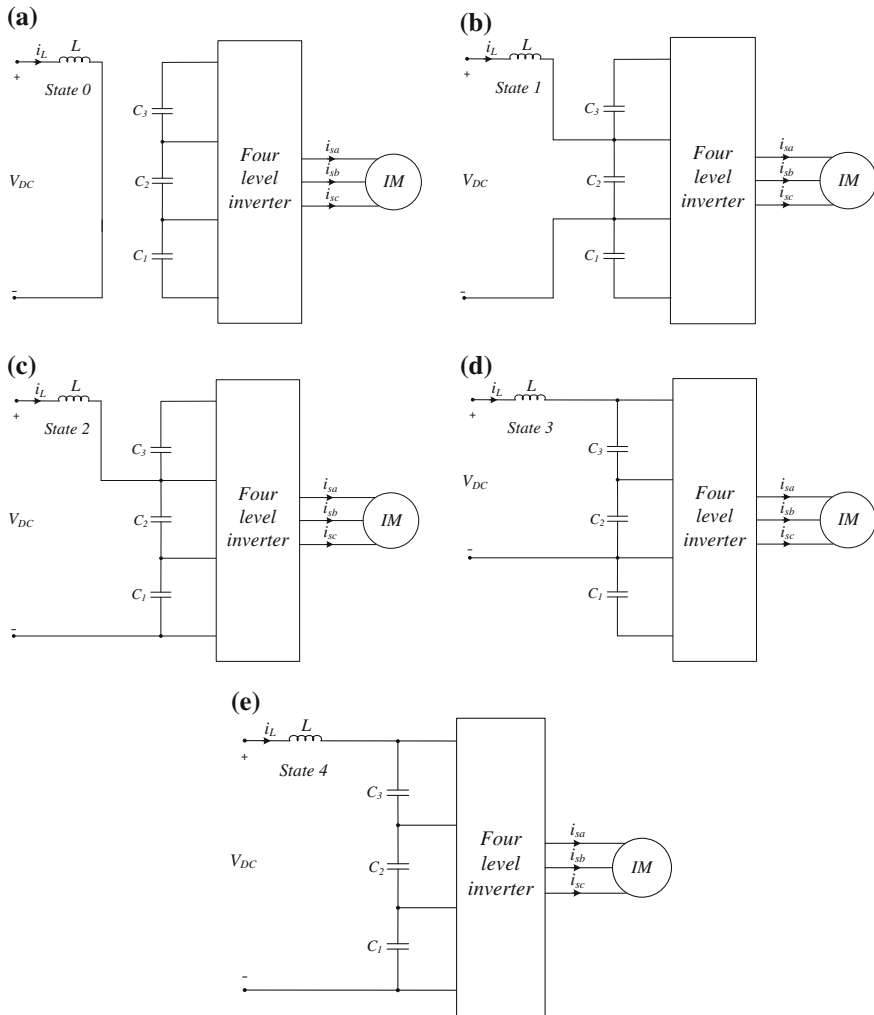


Fig. 10.11 Possible switching states of the four-level one-quadrant DC/DC converter from Fig. 10.10, State 0 (a), State 1 (b), State 2 (c), State 3 (d), and State 4 (e)

time intervals d_1 , d_2 , and d_3 in which different states of the converter are applied. For this purpose, we assume that the inverter is loaded with a resistive load, the resistors R_1 , R_2 , and R_3 (Fig. 10.13).

Assuming that:

1. In the steady state, the voltages on the capacitors are equal with a value $V_O/3$, i.e., $v_{C1} = v_{C2} = v_{C3} = V_O/3$, where V_O is the converter output voltage.

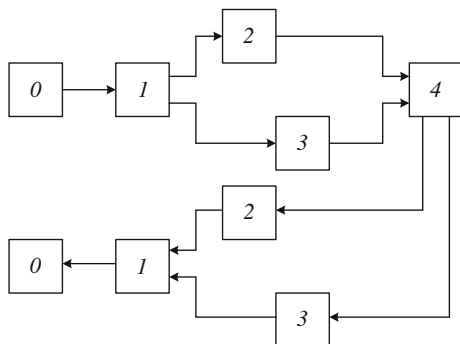


Fig. 10.12 Switching sequence for four-level DC/DC converter from Fig. 10.10 [3]

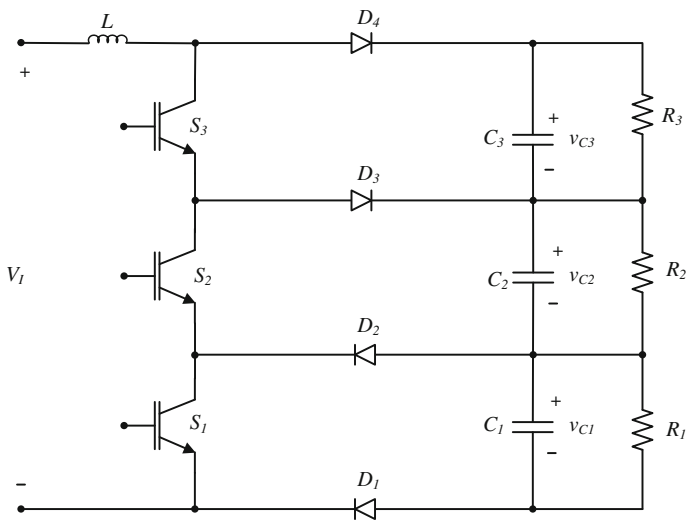


Fig. 10.13 Four-level one-quadrant converter with resistance load

2. The duration of the switching states does not depend on the direction of the switching sequences, i.e., whether the converter transition is from the state 0–4, or vice versa. In other words, during one period the state 1 lasts $\frac{d}{2}T$ for a switching sequence 0–1–2/3–4 and the same time for a switching sequence 4–2/3–1–0. The same is valid for other converter states. The relationship between the output and the input voltage of the DC/DC converter from Fig. 10.13 can be determined from the assumption that the average value of voltage on the inductance L during the period T is equal to 0 ($V_L = 0$), so

$$\begin{aligned}
V_L &= V_I d_1 + \left(V_I - \frac{V_O}{3}\right) d_2 + \left(V_I - \frac{2V_O}{3}\right) d_3 \\
&\quad + (V_I - V_O)(1 - d_1 - d_2 - d_3) = 0 \\
V_I &= V_O \left(1 - d_1 - \frac{2d_2}{3} - \frac{d_3}{3}\right), \frac{V_O}{V_I} = \frac{1}{1 - d_1 - \frac{2d_2}{3} - \frac{d_3}{3}}
\end{aligned} \tag{10.5}$$

The average value of the current i_L (I_L) can be determined from the condition that the input and the output power are equal. Neglecting losses in the converter, and assuming that the average current at the capacitor during the period T is equal to 0, it is obtained

$$\begin{aligned}
V_I I_L &= \frac{V_O}{3} \frac{V_O}{3R_3} + \frac{V_O}{3} \frac{V_O}{3R_2} + \frac{V_O}{3} \frac{V_O}{3R_1} \\
V_I I_L &= \frac{V_O^2}{9} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \\
I_L &= \frac{V_O^2}{9V_I} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)
\end{aligned} \tag{10.6}$$

To determine the ripple current, it is necessary to calculate the change of current for every converter state. The switching sequence 0–1–2/3–4 will be observed. Let the I_1 be the current through the inductance L after the state 0, I_2 at the end of the state 1, I_3 at the end of the state 2/3 and I_4 at the end of the state 4, or half a period. Based on the above, we can write expressions for the currents I_1 , I_2 , I_3 and I_4

$$\begin{aligned}
I_1 &= I_L + \frac{V_I}{2L} d_1 T \\
I_2 &= I_L + \frac{V_I}{2L} d_1 T + \frac{3V_I - V_O}{6L} d_2 T \\
I_3 &= I_L + \frac{V_I}{2L} d_1 T + \frac{3V_I - V_O}{6L} d_2 T + \frac{3V_I - 2V_O}{6L} d_3 T \\
I_4 &= I_L + \frac{V_I}{2L} d_1 T + \frac{3V_I - V_O}{6L} d_2 T + \frac{3V_I - 2V_O}{6L} d_3 T + \frac{V_I - V_O}{2L} (1 - d_1 - d_2 - d_3) T
\end{aligned} \tag{10.7}$$

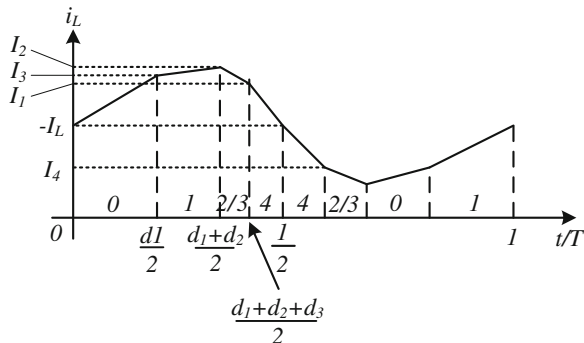
During the second half of the period, the change of the current i_L is the same, except that the applied switching sequence is 4–2/3–1–0 (Fig. 10.14).

The maximum change of the current i_L

$$\Delta i_L = 2(\max\{I_1, I_2, I_3\} - I_L) \tag{10.8}$$

d_1 , d_2 and d_3 are determined on the basis of a known value of the voltage V_I and the required value for the output voltage V_O . The value of d_3 is selected to be small and constant, because in this interval a voltage balance is maintained on the capacitors C_1 and C_3 .

Fig. 10.14 Graph of current i_L during one period [3]



In the time intervals $\frac{d_1}{2}T < t < \frac{d_1+d_2}{2}T$ and $(1 - \frac{d_1+d_2}{2})T < t < (1 - \frac{d_1}{2})T$ the state 1 is active and the center capacitor is charged. In this state, the change in voltage across the capacitor C_2 is higher than across the capacitors C_1 and C_3 . If e_2 is an error of voltage v_{c2} , $e_2 = v_{C2}^* - v_{C2}$, where v_{C2}^* is the reference value of voltage v_{C2} ($v_{C2}^* = V_O/3$), then a linear PI controller can be used to determine the value of d_2 , and its input is e_2 , and the output d_2 . The value d_1 can be determined on the basis of the output voltage, if the values of V_I , d_2 and d_3 are known (Eq. 10.5).

The topologies and the control of DC/DC multilevel converters are subjects of extensive research. Only some topologies of these multilevel converters and their characteristics are described in this section.

Example 10.2 Four-level one-quadrant DC/DC converter shown in Fig. 10.13 has the parameters $V_I = 48$ V, $R_1 = R_2 = R_3 = 5$ Ω and $L = 100$ μ H. The applied switching sequence is 0–1–2–4 when $d_1 = 0.25$, $d_2 = 0.1$ and $d_3 = 0.02$. Determine:

- the output voltage, and
- the average value of the current through the inductor L .

(a) Output voltage (Eq. 10.5) is equal to

$$V_O = \frac{V_I}{1 - d_1 - \frac{2d_2}{3} - \frac{d_3}{3}} = 71 \text{ V.}$$

(b) Following the Eq. (10.6), the average value of the inductor L current is:

$$I_L = \frac{V_O^2}{9V_I} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) = \frac{71^2}{9 \cdot 48} (0.2 + 0.2 + 0.2) = 7 \text{ A.}$$

10.3 Multilevel Inverters

Among multilevel converters, the multilevel DC/AC converters have an important place. There are many AC consumers like AC motors in controlled electric drives with powers above 1 MW, while their supply voltages are several kV and more.

Another important area of application of these converters are renewable energy sources, where these converters are used for the connection of wind generators, photovoltaic modules, fuel cells, etc., to electrical grid.

Besides the previously mentioned properties (Sect. 10.1), the multilevel inverters have several advantages over conventional two-level inverters [4]:

- Lower voltage stress on switches, also dv/dt stress; therefore electromagnetic compatibility problems can be reduced;
- Input current has lower harmonic distortions;
- Multilevel inverters can operate at the fundamental frequency, but also at higher switching frequencies when the PWM technique is applied.

There are many topologies of multilevel inverters, but the following four major converter structures have the widest use:

- cascaded H-bridges converters with separate DC sources,
- diode-clamped multilevel inverters,
- flying capacitors, and
- hybrid topologies.

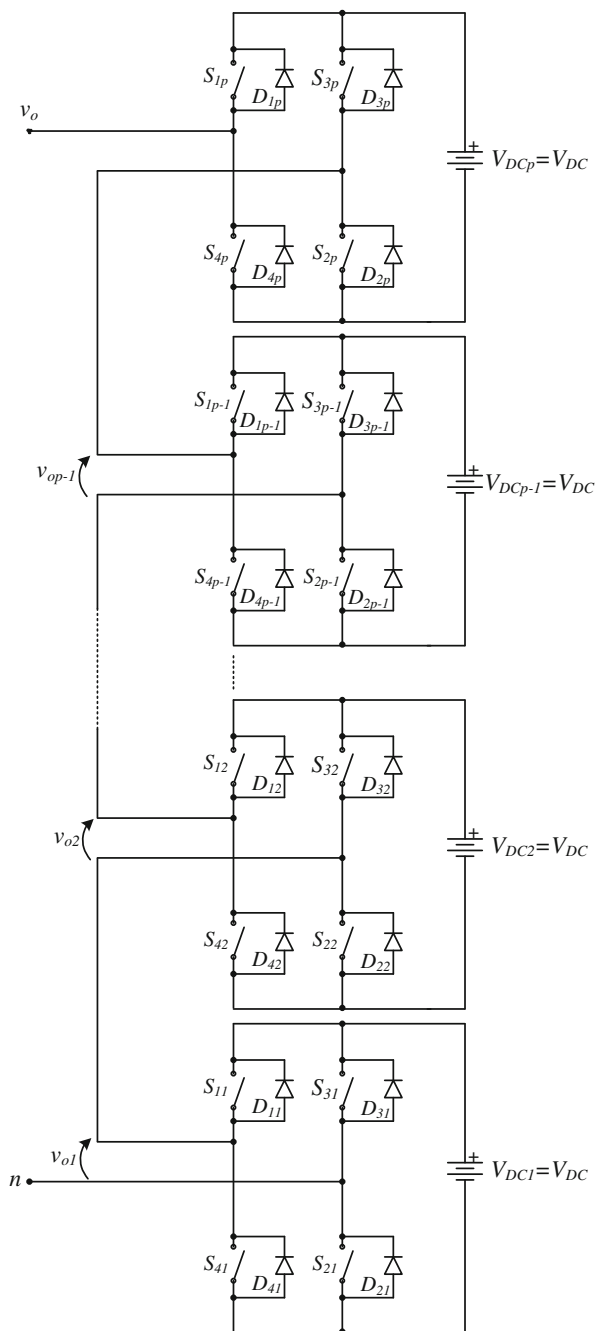
Different modulation techniques are used for the control of multilevel inverters, like sinusoidal pulse width modulation, selective harmonic elimination (SHE), space vector modulation and others. These techniques are modified for the use in multilevel inverters.

10.3.1 Cascaded H-Bridge Inverters

A cascaded multilevel H-bridge inverter consists of a number of cascade connected H-bridge single-phase inverters supplied from separate DC sources. A cascaded m -level H-bridge inverter is shown in Fig. 10.15. It consists from p single-phase inverters, and their number is determined by the inverter level $m = 2p + 1$. Depending on the state of the switches, three voltage levels can be obtained at the output of each inverter $+V_{DC}$ (S_{1k} and S_{2k} are turned on), 0 (S_{1k} and S_{3k} , or S_{2k} and S_{4k} are turned on) and $-V_{DC}$ (S_{3k} and S_{4k} are turned on), $k = 1, 2, \dots, p$.

The output voltage is equal to the sum of the single-phase inverter output voltages $v_o = v_{o1} + v_{o2} + \dots + v_{op}$. The waveforms of a 11-level inverter output voltage and the output voltages of each cascade-connected single-phase inverter are shown in Fig. 10.16.

Fig. 10.15 Cascaded H-bridge p-level inverter



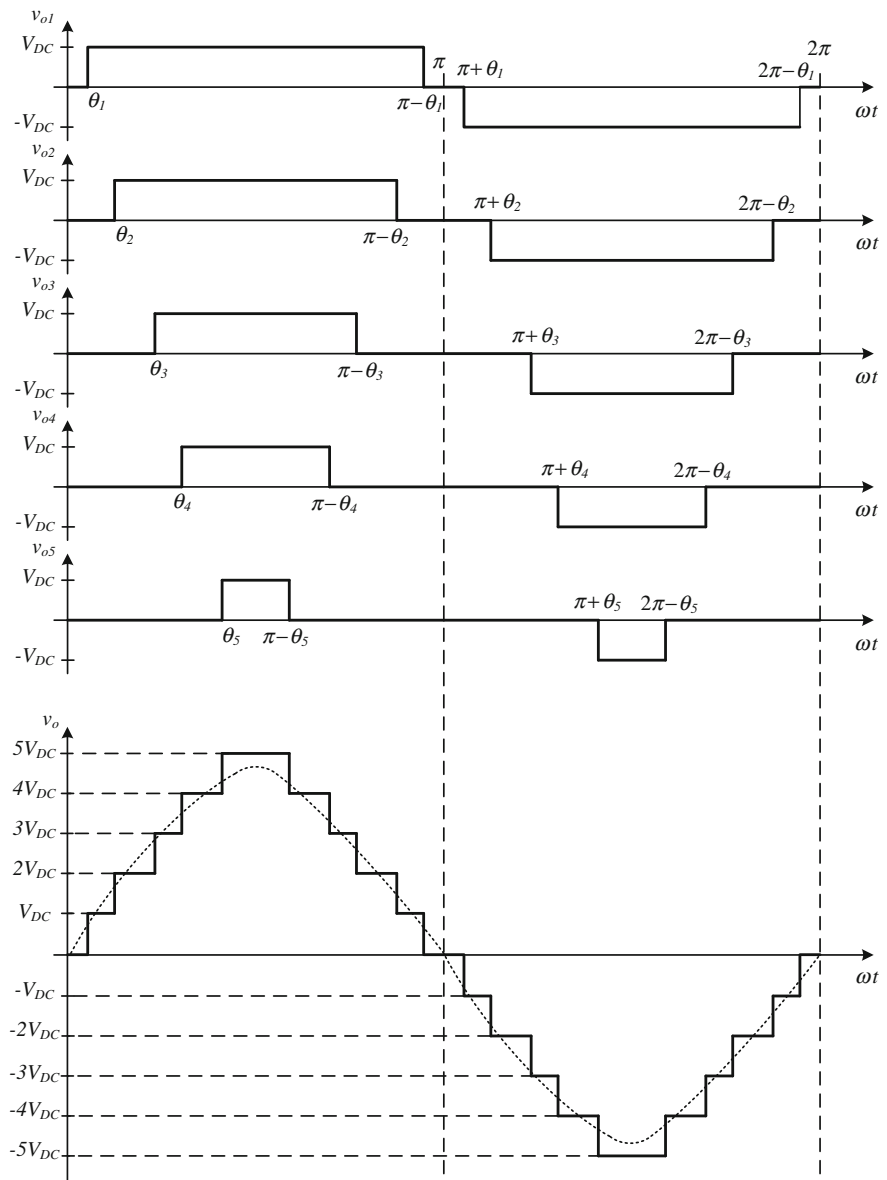


Fig. 10.16 Waveforms of 11-level inverter output voltage and output voltages of each cascade-connected single-phase inverters

The output voltage of each single-phase inverter can be expressed as

$$v_{ok} = \begin{cases} +V_{DC}, & \vartheta_K < \omega t < \pi - \vartheta_K \\ 0, & 0 < \omega t < \vartheta_K, \pi - \vartheta_K < \omega t < \pi + \vartheta_K, 2\pi - \vartheta_K < \omega t < 2\pi \\ -V_{DC}, & \vartheta_K \leq \omega t \leq \pi + \vartheta_K < \omega t < 2\pi - \vartheta_K \end{cases} \quad (10.9)$$

$$k = 1, 2, 3, 4, 5$$

This voltage is $v_o = v_{o1} + v_{o2} + v_{o3} + v_{o4} + v_{o5}$ and the following expression can be obtained:

$$v_o(\omega t) = \sum_{n=1,5,7,\dots} \frac{4V_{DC}}{n\pi} [\cos(n\vartheta_1) + \cos(n\vartheta_2) + \dots + \cos(n\vartheta_5)] \sin(n\omega t) \quad (10.10)$$

The harmonics that have a dominant influence on the total harmonic distortion of the output voltage (5, 7, 11, 13) can be eliminated by the appropriate choice of the angle θ_k (10.10). Also, the output voltage of a multilevel inverter is closer to a sinusoidal form and has lower harmonic distortion than the conventional single-phase two-level bridge inverter. Because the single-phase H-bridge inverters are produced as particular modular units, the desired topology of the multilevel inverter is obtained by connecting these units in cascade. On the other hand, every single-phase H-bridge requires a separate DC power supply.

This limits the application of this inverter topology to those cases in which a number of separate DC sources is sufficient.

A multilevel inverter for the power supply of a three-phase AC motor, or a battery charger is shown in Fig. 10.17 [5]. It is a three-phase multilevel inverter and each phase has a five single-phase bridge supplied from separate DC 48 V sources.

Example 10.3 The cascaded 11-level H-bridge inverter shown in Fig. 10.15 has separate DC sources with identical voltages equal to 24 V. The control angles of the switches are $\theta_1 = 15^\circ$, $\theta_2 = 30^\circ$, $\theta_3 = 45^\circ$, $\theta_4 = 60^\circ$, and $\theta_5 = 75^\circ$. Determine the amplitude of the fundamental harmonic of the output voltage.

According to (10.10), the amplitude of the fundamental harmonic of the output voltage is equal to

$$V_1 = \left| \frac{4V_{DC}}{\pi} (\cos \theta_1 + \cos \theta_2 + \cos \theta_3 + \cos \theta_4 + \cos \theta_5) \right|$$

$$= \left| \frac{4 \times 24}{\pi} (\cos 15^\circ + \cos 30^\circ + \cos 45^\circ + \cos 60^\circ + \cos 75^\circ) \right| = 100.1 \text{ V.}$$

Another topology of multilevel cascade inverter includes a transformer and uses the standard three-phase, two-level inverter modules (Fig. 10.18) [6]. In order to add up the converter voltage, the outputs of the inverter modules need to be synchronized with the displacement of 120° between each phase. The phasor diagram

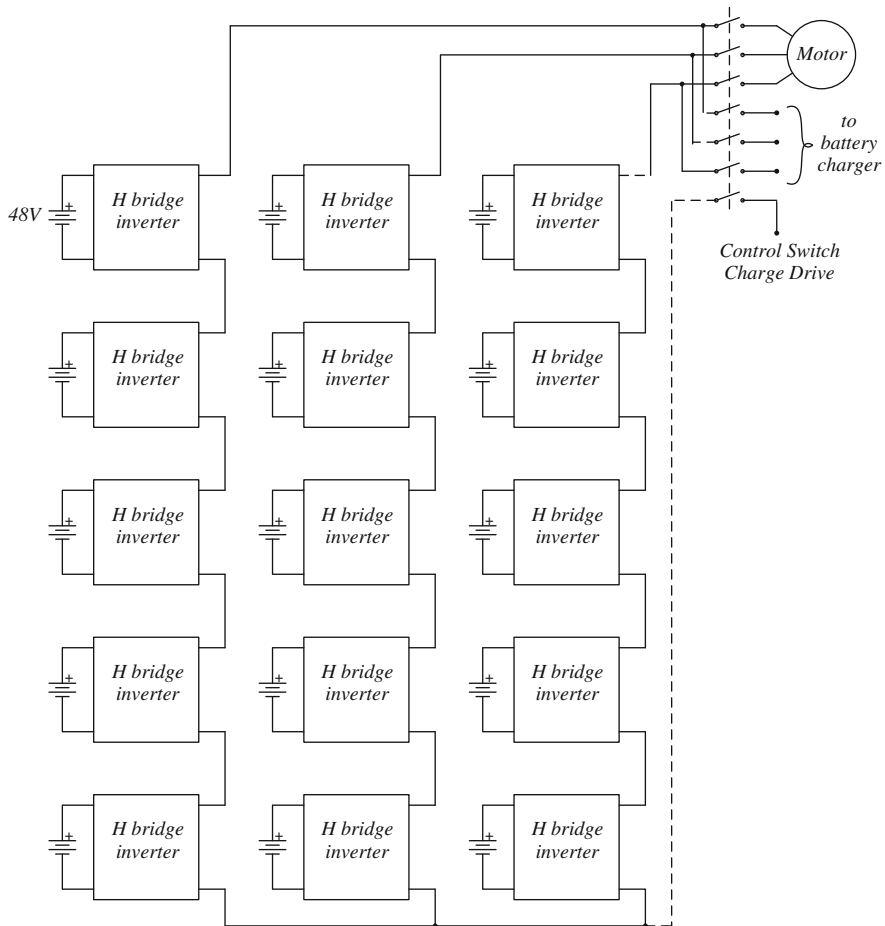


Fig. 10.17 Three-phase cascade 11-level H-bridge inverter for power supplying three-phase AC motor, or battery charger

of the multilevel inverter from Fig. 10.18 is shown in Fig. 10.19. The phase voltages at the output of the inverter modules are a_k , b_k and c_k ($k = 1, 2, 3$). An isolated transformer is used to provide the voltage boost. These isolating transformers with a 1:1 ratio generate voltages a_2b_1 , c_1a_3 and b_3c_2 from the output voltages of the AC inverter modules b_3a_3 , a_2c_2 and c_1b_1 , respectively (Fig. 10.19).

In this way, the required values of the line voltages AB , BC , and CA are obtained. The advantages of the proposed multilevel inverter shown in Fig. 10.18 are as follows:

- Due to the modular design, the switching components in the inverter modules have a lower voltage stress. Also, this inverter design allows easy maintenance;
- Lower dv/dt effect;

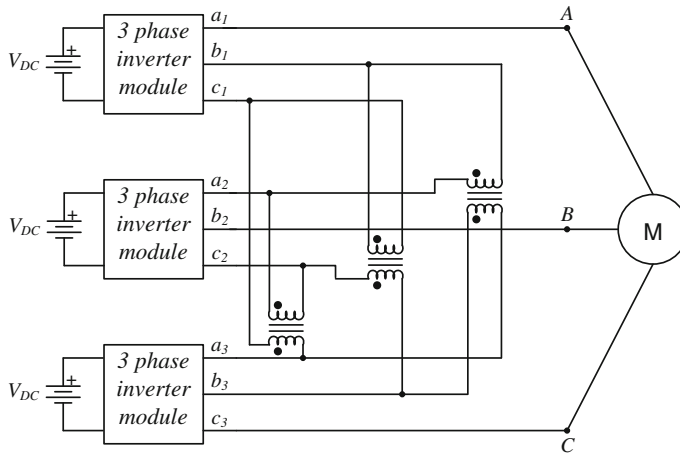
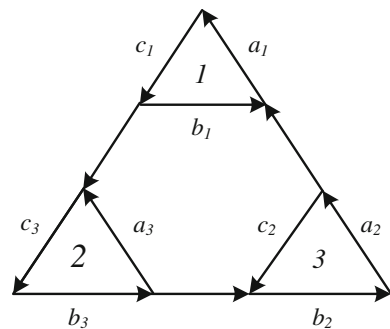


Fig. 10.18 Three-phase multilevel inverter with isolated transformers [6]

Fig. 10.19 Phasor diagram of the inverter from Fig. 10.18



- Lower harmonic distortion of the output voltage and current, especially the output current if the load is an AC motor;
- A high capacitor in the DC link is not necessary due to the balanced load.

The proposed system is suitable for power supply of V/f controlled electrical drives in a wide range of operating speeds. Also, the output transformers provide higher output voltages and prevent the formation of current circuits within the inverter modules.

10.3.2 Diode-Clamped Multilevel Inverters

In comparison to other multilevel inverters, the diode-clamped multilevel inverter topologies are attractive from economic reasons and because of their high efficiency

in fundamental frequency switching. Also, all their phases share a common DC link, which minimizes the capacity requirements of the converter.

The basic principles of the diode-clamped multilevel inverter and its advantages over the conventional 2-level inverters were described for one leg of an inverter bridge in Sect. 10.1. This three-phase multilevel inverter topology has applications in the high power AC electrical drives, static var compensation, and high-voltage system interconnection.

Besides the good characteristics of these converters, there are certain practical problems in their application related to dynamic voltage stress on switches and voltage balance on the intermediate DC levels. The voltage balance of the capacitors will be held only if the average value of the current through the capacitors during one period of the output voltage is 0. This is one of the reasons why the diode-clamped multilevel inverters are used in back-to-back converters, i.e., two identical multilevel inverters are connected to a common DC link. One multilevel converter works as rectifier, and another as inverter. This connection allows power transmission in both directions, so it is most commonly used to couple two synchronous systems, or to power a three-phase AC motor from an AC source. If the diode-clamped multilevel inverter is used for one direction power transmission from a DC source to an AC load, the DC/DC converter is placed between the DC source and the multilevel inverter input. The role of this DC/DC converter is to maintain the voltage balance at the input of the multilevel inverter (see, e.g., Figs. 10.9 and 10.10). A three-phase 5-level diode-clamp inverter is shown in Fig. 10.20.

The voltage on the capacitors C_1 – C_4 is V_{DC} , and the voltage stress across each switch is limited to V_{DC} through the clamping diodes.

Each leg has four complementary switch pairs. The complementary switch pairs for the leg b are (S_{b1}, S'_{b1}) , (S_{b2}, S'_{b2}) , (S_{b3}, S'_{b3}) and (S_{b4}, S'_{b4}) . If one switch in the pair is turned on, the second is turned off, and vice versa. The state of the switches is controlled, so that in any moment, four switches are turned on. The output voltage of each phase is determined by the state of the switches. Thus, we can observe the output voltage of the phase B in relation to the lowest level of the input voltage. If the four lower switches S'_{b1} , S'_{b2} , S'_{b3} and S'_{b4} are turned on, then $v_b = 0$. If one upper and three lower switches S_{b1} , S'_{b2} , S'_{b3} , S'_{b4} are turned on, then $v_b = V_{DC}$. The maximum voltage $v_b = 4V_{DC}$ would be reached if four upper switches S_{b1} , S_{b2} , S_{b3} and S_{b4} were turned on and four lower switches S'_{b1} , S'_{b2} , S'_{b3} and S'_{b4} were turned off. In this topology, it is obvious that the voltage stress across each diode is not equal. In fact, the diode D_1 must block V_{DC} , the diode D_2 must block $2V_{DC}$, and the diode D_3 must block $3V_{DC}$. If the inverter design is such that each blocking diode has the same voltage rating, two diodes connected in series should be used instead of the diode D_2 , and three diodes connected in series instead of the diode D_3 . This means that the number of diodes required for each phase of the inverter is equal to $(n - 1)(n - 2)$, where n is the number of the output voltage levels.

Example 10.4 Define the necessary number of clamping diodes for a three-phase 6-level diode-clamped inverter, so that each diode blocks a voltage equal to V_{DC} . If

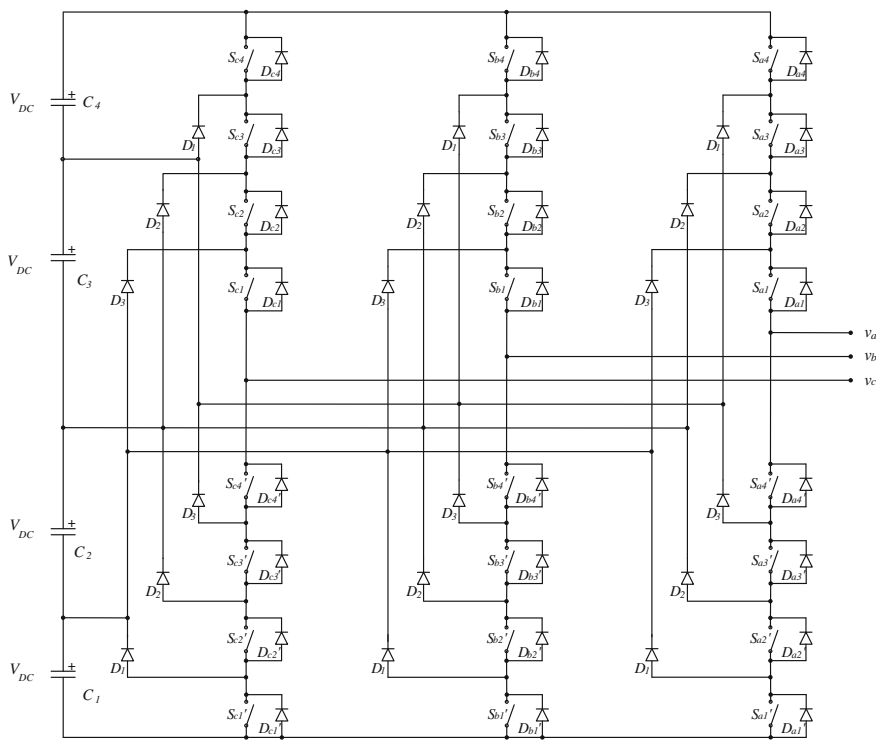


Fig. 10.20 Three-phase 5-level diode-clamped inverter

the output voltage of the phase a is equal to $2V_{DC}$ determine which switches in the branch a are turned on.

The necessary number of diodes is $3(n-1)(n-2) = 3(6-1)(6-2) = 60$, where 3 is the number of phases, and $n = 6$ is the number of the output voltage levels. The switches S_{a1} , S_{a2} , S'_{a3} and S'_{a4} are turned on.

10.3.3 Flying Capacitor Multilevel Inverter

The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, capacitors are used in their place. A four-level flying capacitor inverter is shown in Fig. 10.21.

This topology has a ladder structure of DC side capacitors. The voltage at each adjacent capacitive branch is different and the voltage difference defines the size of the output voltage step, which is equal to V_{DC} . The main advantage of the flying capacitor inverter in relation to the diode-clamped multilevel inverter is that it has redundancies for inner voltage levels. In other words, it is possible to have two or more different valid switch combinations in order to obtain the same output voltage.

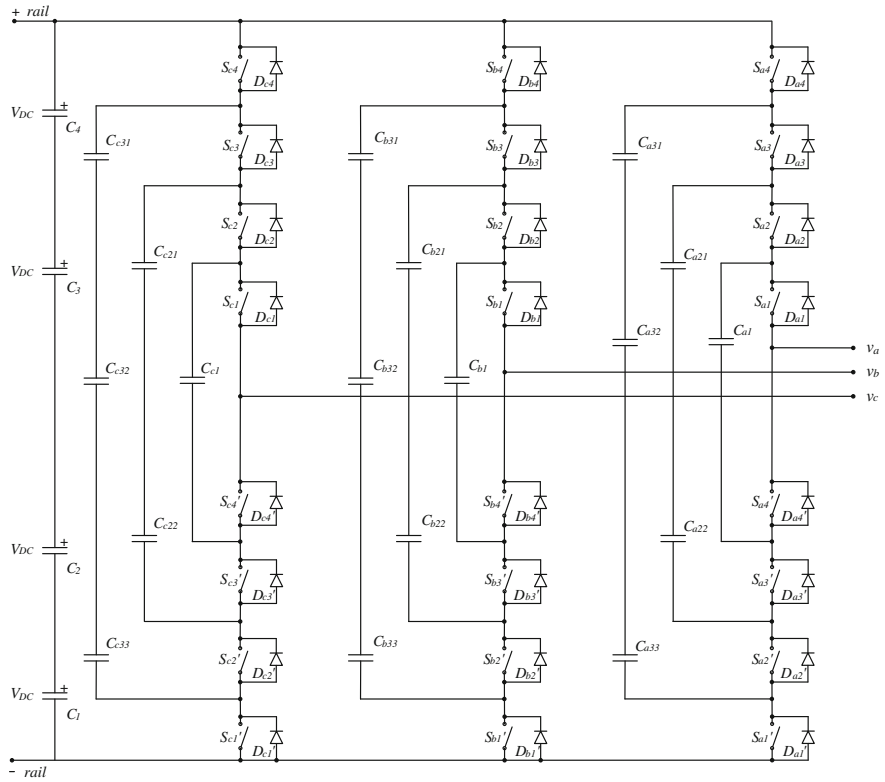


Fig. 10.21 Three-phase 5-level flying capacitor inverter

Furthermore, the flying capacitor topology has phase redundancy (it relates to generation of phase voltage), while diode-clamped inverters only have a line redundancy (relates to generation of line-to-line voltage). This feature is important because it allows the use of control techniques for voltage balance of capacitive branches. The number of the redundant states depends on the output voltage. This will be considered for the phase *a*. If $v_a = 4V_{DC}$ (four upper switches $S_{a1}, S_{a2}, S_{a3}, S_{a4}$ are turned on), or $v_a = 0$ (four lower switches $S'_{a1}, S'_{a2}, S'_{a3}, S'_{a4}$ are turned on), there are no redundant states. If the voltage $v_a = 3V_{DC}$, the allowed switches states are as shown in Table 10.1. For this case, the number of redundant states is 2. A similar analysis can be made for other voltage levels.

Table 10.1 Switching states of three-phase 5-level flying capacitor inverter for $V_a = 3V_{DC}$

Output voltage	Switching states							
	S_{a4}	S_{a3}	S_{a2}	S_{a1}	S'_{a4}	S'_{a3}	S'_{a2}	S'_{a1}
$3V_{DC}$	0	1	1	1	0	0	0	1
$4V_{DC} - V_{DC}$	1	1	1	0	1	0	0	0
$4V_{DC} - 3V_{DC} + 2V_{DC}$	1	0	1	1	0	0	1	0

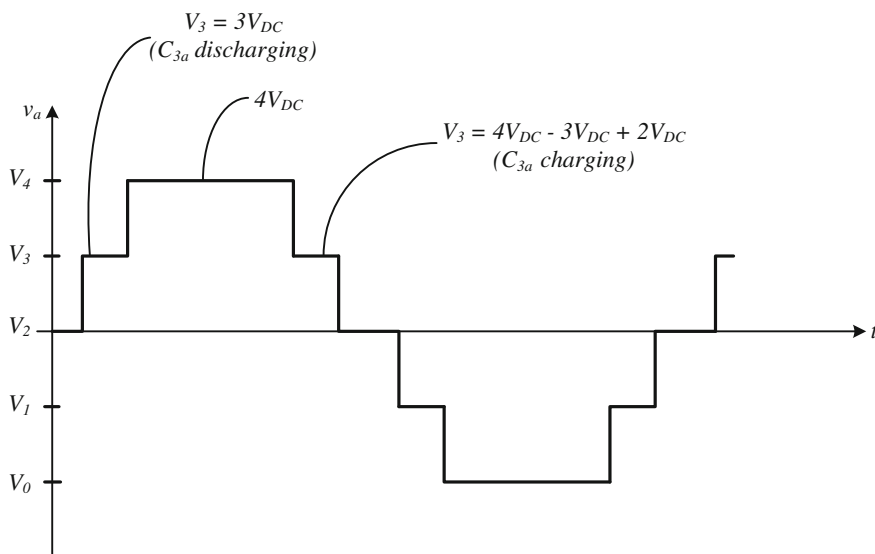


Fig. 10.22 Waveforms of voltage v_a during one period

In this type of multilevel inverter, it is also needed to maintain voltage balance on the capacitors. This is accomplished by applying appropriate control sequences, so the inner capacitors equally charge and discharge during one period. One period of the voltage v_a is shown in Fig. 10.22.

If the output voltage V_3 is obtained as $3V_{DC}$, the capacitors C_{a3} are discharged. On the other hand if the output voltage V_3 is obtained as $4V_{DC} - 3V_{DC} + 2V_{DC}$, the capacitors C_{a3} are charged. In order to maintain a voltage balance, the number of charging and discharging cycles of the inner capacitors during each period should be equal. If the control sequence $V_3-V_4-V_3$ is applied, as shown in Fig. 10.22, only two switches change their state, one is turned on, and the second is turned off.

Besides the advantages of this inverter topology that include the phase redundancy, there are also certain drawbacks. These are [4]:

- The voltage level tracking for all the capacitors is complicated. Also, pre-charging all of the capacitors to the same voltage level is a complex task.
- Switching utilization and efficiency are poor.
- A large number of capacitors is both more expensive and bulkier than the clamping diodes in a diode-clamped multilevel inverter.

10.3.4 Other Multilevel Inverter Topologies

The generalized topology of a multilevel inverter, the so-called P2 topology is presented in Fig. 10.23 [7]. This topology allows automatic maintenance of the

voltage balance without a support of other circuits, for an arbitrary number of voltage levels at the output, and regardless of load characteristics.

The voltage stress on the switches and the capacitors is the same and is equal to V_{DC} . The topology of the basic cell is simple. It consists of two complementary switches connected in parallel with a capacitor (Fig. 10.23). By turning on the lower switch, the lower voltage is forwarded to the next level, and by turning on the upper switch, the higher voltage is forwarded to the next level. The difference between these two voltages is equal to the voltage on the capacitor (V_{DC}).

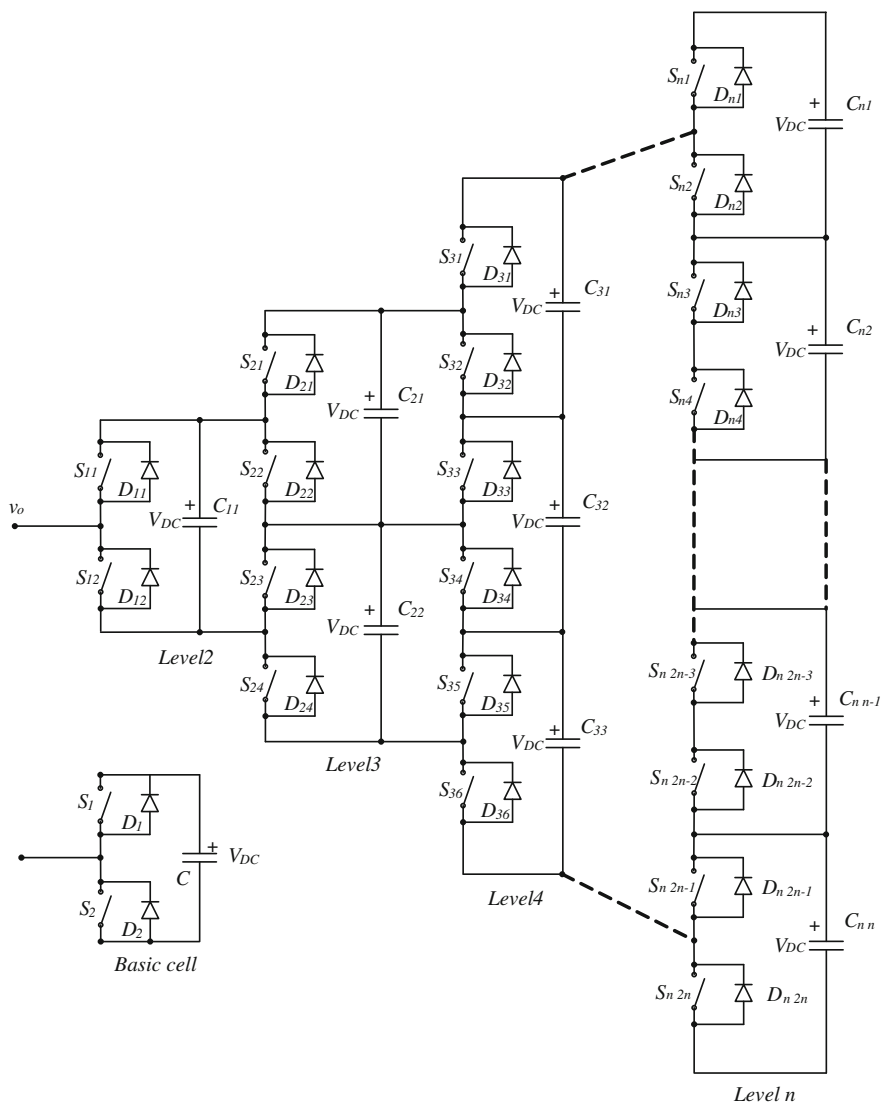


Fig. 10.23 Topology of so-called P_2 multilevel inverter and its basic cell

Besides the basic topology described previously, there is a significant number of new multilevel inverter topologies. These topologies are derived from the existing ones and represent their improvement.

The hybrid multilevel inverter is a combination of the cascaded H-bridge multilevel and the diode-clamped multilevel inverter. This implementation reduces the required number of separate DC sources. Figure 10.24 [4] shows one branch of the

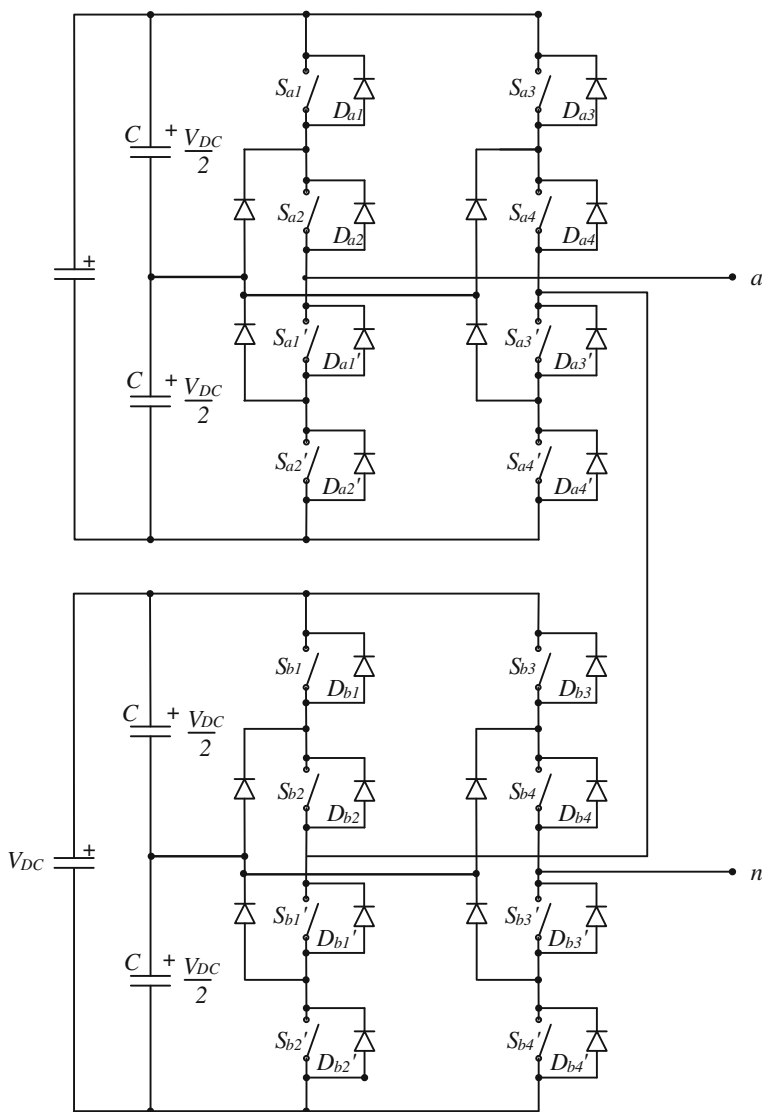


Fig. 10.24 One branch of the 9-level hybrid inverter

three-phase hybrid inverter with two cascaded connected cells, each cell consisting of a 5-level diode-clamped multilevel inverter.

In this way, we get a 9-level inverter with only two separate DC sources per phase, or a total of six separate sources for the whole three-phase inverter. For the realization of the same inverter with a standard H-bridge inverter modules, 16 separate DC sources are needed.

Example 10.5 For one branch of the 9-level hybrid inverter shown in Fig. 10.24 define the switching states, the voltages at the output of the inverter modules and the output voltage of the inverter.

The switching states, the voltages at the output of inverter modules and the output voltage of the 9-level hybrid inverter are shown in Table 10.2.

Table 10.2 Switching states, voltages at the output of inverter modules and the output voltage of the 9-level hybrid inverter

Turned on switches		$V_{a'd'}$	$V_{a'n}$	$V_{an} = V_{a'd'} + V_{a'n}$
Inverter A	Inverter B			
$S'_{a1}, S'_{a2}, S_{a3}, S_{a4}$	$S'_{b1}, S'_{b2}, S_{b3}, S_{b4}$	$-V_{DC}$	$-V_{DC}$	$-2V_{DC}$
$S'_{a1}, S'_{a2}, S_{a3}, S_{a4}$	$S'_{b1}, S_{b2}, S_{b3}, S_{b4}$	$-V_{DC}$	$-V_{DC}/2$	$-3V_{DC}/2$
$S'_{a1}, S_{a2}, S_{a3}, S_{a4}$	$S'_{b1}, S_{b2}, S_{b3}, S_{b4}$	$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}$
$S'_{a1}, S'_{a2}, S'_{a3}, S'_{a4}$	$S'_{b1}, S_{b2}, S_{b3}, S_{b4}$	0	$-V_{DC}/2$	$-V_{DC}/2$
$S'_{a1}, S'_{a2}, S'_{a3}, S'_{a4}$	$S'_{b1}, S'_{b2}, S'_{b3}, S'_{b4}$	0	0	0
$S'_{a1}, S_{a2}, S'_{a3}, S'_{a4}$	$S'_{b1}, S'_{b2}, S'_{b3}, S'_{b4}$	$V_{DC}/2$	0	$V_{DC}/2$
$S'_{a1}, S_{a2}, S'_{a3}, S_{a4}$	$S'_{b1}, S_{b2}, S'_{b3}, S_{b4}$	$V_{DC}/2$	$V_{DC}/2$	V_{DC}
$S'_{a1}, S_{a2}, S'_{a3}, S'_{a4}$	$S_{b1}, S_{b2}, S'_{b3}, S'_{b4}$	$V_{DC}/2$	V_{DC}	$3V_{DC}/2$
$S_{a1}, S_{a2}, S'_{a3}, S'_{a4}$	$S_{b1}, S_{b2}, S'_{b3}, S'_{b4}$	V_{DC}	V_{DC}	$2V_{DC}$

In order to reduce switching losses and increase efficiency, multilevel inverter topologies with resonant circuits for soft-switching are also used.

10.4 Control of Multilevel Inverters

Modulation techniques used in multilevel inverters can be classified according to the applied switching frequency (Fig. 10.25) [7]. Techniques popular in industrial applications that work at higher switching frequencies are the sine PWM and the space vector modulation technique. They can be simply expanded from 2-level to multilevel inverters.

Techniques that work at lower frequencies are characterized by a smaller number of switching cycles during one period and a staircase shape of the output voltage. More commonly used techniques are the SHE and the space vector control (SVC).

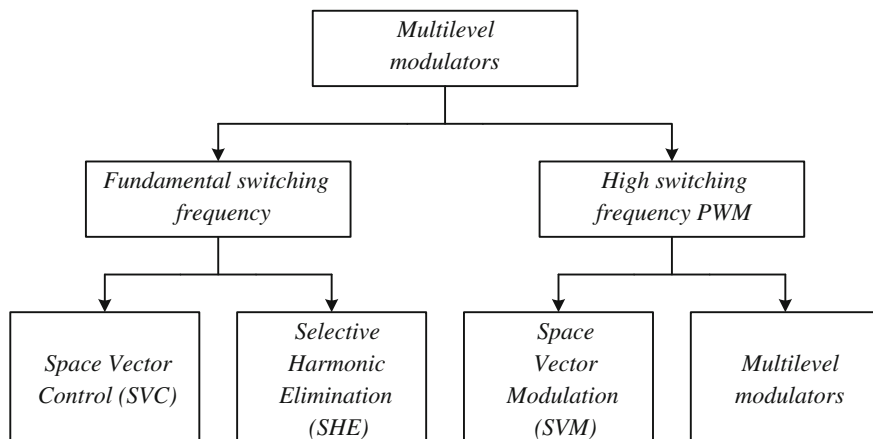


Fig. 10.25 Classification of modulation techniques used in multilevel inverters

10.4.1 Multilevel SPWM

A simple and often used modulation technique for multilevel inverters is the SPWM.

In order to achieve a better DC link utilization at high modulation, a third harmonic with a magnitude equal to 25 % of the fundamental one is injected in the reference signal (third harmonic injection PWM-THPWM) (Fig. 10.26). Other interesting carrier-based multilevel PWM techniques are the subharmonic PWM (SH-PWM) and the Switching frequency optimal PWM (SFO-PWM). For the SH-PWM techniques for an n -level inverter, $n-1$ carriers with the same frequency f_i and the same amplitude V_{tM} are introduced such that the bands they occupy are contiguous [8]. A reference signal with the amplitude V_{cM} and the frequency f_c has its zero centered in the middle of the triangular carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than the carrier, the control signal is a such that the corresponding output voltage level is high. Otherwise, if the reference is lower than the carrier, then the corresponding output voltage level is low.

The carrier signals, the sinusoidal reference signal with an amplitude modulation factor $m_a = 0.8$, and the waveform of one output phase voltage for a 5-level diode-clamped inverter are shown in Fig. 10.27. In n -level multilevel inverter, the amplitude modulation index m_a and the frequency modulation index, m_f , are defined as

$$m_a = \frac{V_{cM}}{(n-1)V_{tM}}, \quad m_f = \frac{f_t}{f_c} \quad (10.11)$$

Example 10.6 Define the amplitude and the modulation factor of a 5-level diode-clamped inverter if $f_c = 50$ Hz, $f_t = 1.35$ kHz, $V_{tM} = 1$ V, and $V_{cM} = 3.6$ V.

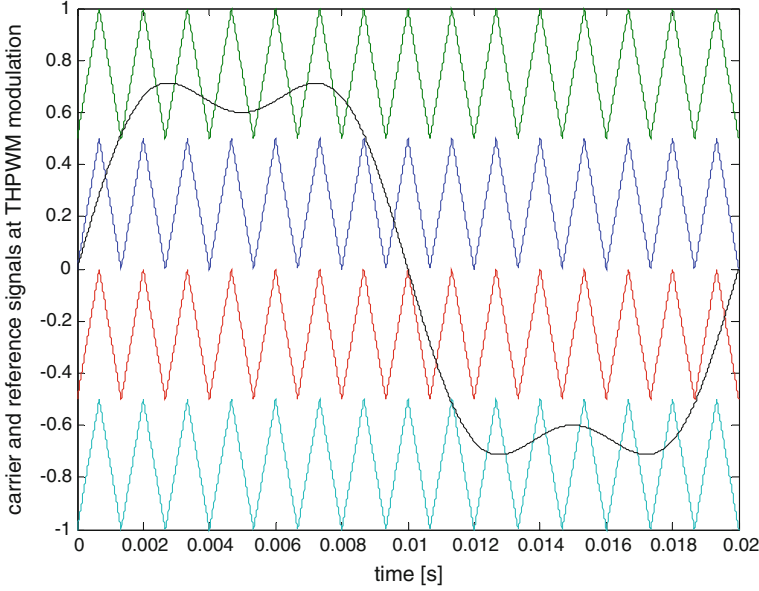


Fig. 10.26 Carrier sets and reference signal for one phase of a 4-level multilevel inverter when THPWM modulation technique is applied ($m_a = 0.8$, $f_c = 50$ Hz, and $f_i = 750$ Hz)

According to Eq. (10.11), the amplitude modulation index m_a and the frequency modulation index, m_f are

$$m_a = \frac{V_{cM}}{(n-1)V_{tM}} = \frac{3.6}{4.1} = 0.9, \quad m_f = \frac{1350}{50} = 27.$$

The SFO-PWM method [9] is similar to the SH-PWM with the difference that the third harmonic is added to each of the carriers. The voltage V_{offset} is the instantaneous average of the maximum and minimum of the three reference voltages v_{ca} , v_{cb} and v_{cc}

$$V_{\text{offset}} = \frac{\max(v_{ca}, v_{cb}, v_{cc}) - \min(v_{ca}, v_{cb}, v_{cc})}{2} \quad (10.12)$$

and it is subtracted from each of the individual reference voltages, so that the new reference voltages are

$$\begin{aligned} v_{ca\text{SFO}} &= v_{ca} - V_{\text{offset}} \\ v_{cb\text{SFO}} &= v_{cb} - V_{\text{offset}} \\ v_{cc\text{SFO}} &= v_{cc} - V_{\text{offset}} \end{aligned} \quad (10.13)$$

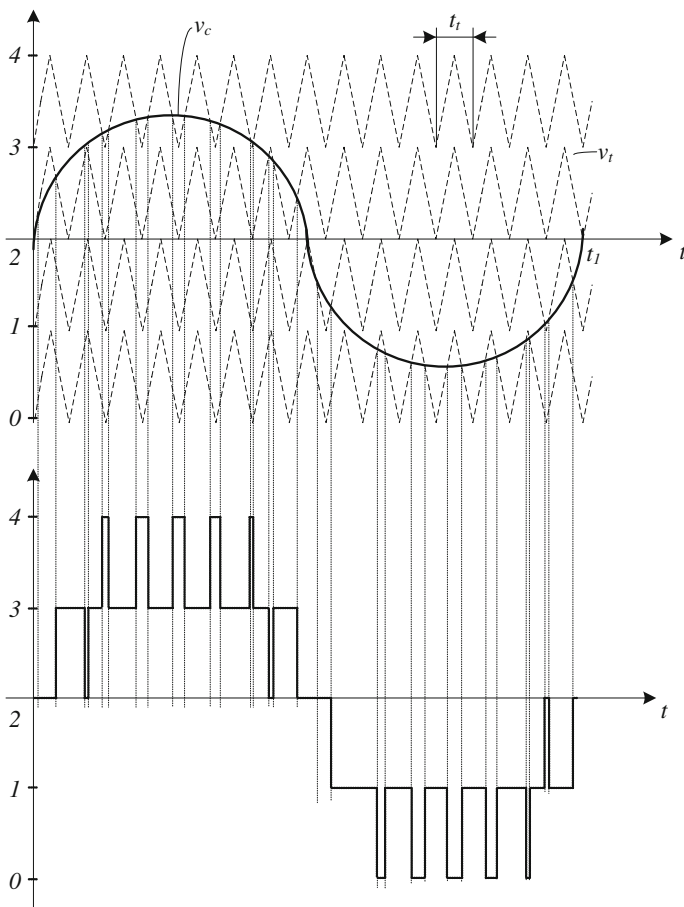
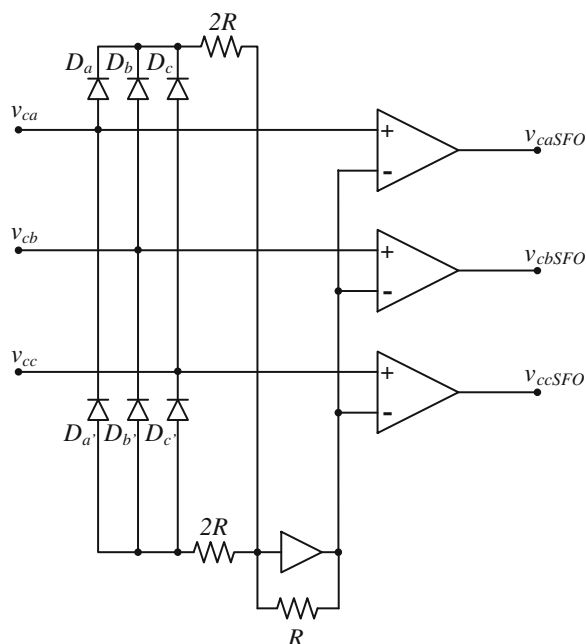


Fig. 10.27 Carrier sets, sinusoidal reference signal and waveform of one output phase voltage for 5-level inverter

An example of the realization of analog circuits that generate reference signals using the SFO-PWM method is shown in Fig. 10.28.

There are also the SHEPWM methods that enable the generation of the inverter output voltage with a small value of the THD. This technique gives the freedom in the choice of phase the displacement between the carrier signals. They can be in phase, with opposite phases, or phase-shifted by a certain angle. Similarly to the case of SPWM applied to 2-level invertors, these modulation techniques, when applied to multilevel invertors, give a lower harmonic distortion, and the first higher harmonics appear around the carrier signal frequency.

Fig. 10.28 An example of analog circuits that generate reference signals with SFO-PWM method [4]

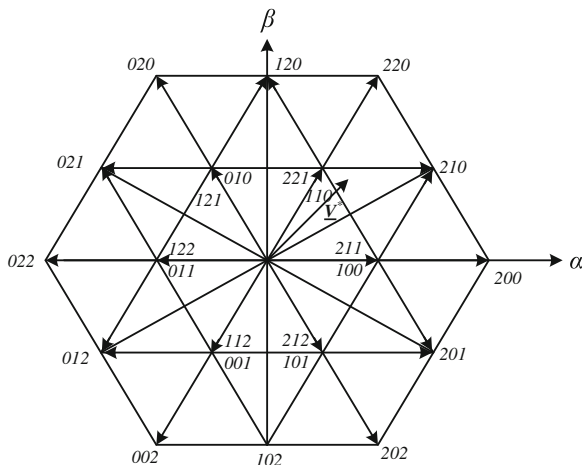


10.4.2 Space Vector Modulation

The Space Vector Modulation (SVM) represents an extension of the SVM technique discussed for three-phase 2-level inverters (Sect. 6.4). This technique can be used for control of all types of multilevel inverters. A control scheme based on the SVM for a three-phase 3-level inverter is shown in Fig. 10.29. There is a third zero vector (222), besides the two zero vectors (000), (111) which are at 2-level inverters. This zero vector corresponds to the case when all three phases are at the highest voltage level. The appropriate voltage vector is obtained by the same principle as for the 2-level inverters. Suppose that the voltage which should be generated is $\underline{V}^*$ (Fig. 10.29). In this case, an appropriate vector can be generated using the three vectors that determine the regular triangle containing the peak of the vector $\underline{V}^*$. The starting point is the vector which has an even redundancy 100 (211) or 110 (221). The control sequence is realized by applying two vectors which differ in only one switching state. In this way only one commutation is necessary for the transition from one state to another. There are the following control sequences which can be applied:

- (a) 211-210-110-100
- (b) 221-211-210-110

Fig. 10.29 SVM control scheme for three-phase 3-level inverter



In this case, reverse sequences are not explicitly considered. The vectors $\underline{V}_1$, $\underline{V}_2$, $\underline{V}_3$ are applied in the time intervals t_1 , t_2 and t_3 , respectively, and $t_1 + t_2 + t_3 = T$.

In order to obtain a lower number of commutations intervals, t_1 is divided into two intervals kt_1 ($0 < k < 1$) in which the vector $\underline{V}_1$ is applied and second interval $(1 - k)t_1$ in which the second vector $\underline{V}_1 \mp \underline{V}_0$ is applied. Taking this into account, the output vector is generated in the form

$$\underline{V}^* = \frac{\underline{V}_1 kt_1 + \underline{V}_2 t_2 + \underline{V}_3 t_3 + (\underline{V}_1 \mp \underline{V}_0)(1 - k)t_1}{T} \quad (10.14)$$

Of course, the applied vector $\underline{V}_0$ is different from the zero vector 000. The application of the SVM in multilevel inverters has the following benefits:

- good utilization of the DC link,
- small current ripple, and
- a relatively simple hardware implementation.

This algorithm is complicated for a greater number of inverter voltage levels. In this case, the number of redundant switching states and the instances of selection of control sequences significantly increase.

10.4.3 Space Vector Control

The SVC technique works at lower switching frequencies. Here the average value of the reference voltage is not generated during one period, as is the case with SVMs. The basic idea of the SVC is to select the vector that gives the minimum spatial error in relation to the reference voltage vector $\underline{V}^*$. This technique is

interesting for multilevel inverters with a larger number of voltage levels, because the error between the applied voltage and the reference vector in this case is small. However, with the reduction of the voltage level numbers, the error in the applied voltage increases, and with it the load current ripple.

10.4.4 Selective Harmonic Elimination

One way of eliminating low-frequency harmonics in spectrum of the inverter output voltage is the SHE technique. This technique can be explained on the example of multilevel H-bridge inverters. The output voltage has a staircase form (Fig. 10.18) and with an appropriate selection of the angles when the switches are turned on, the dominant harmonics can be eliminated. For the angles $\vartheta_k, k = 1, 2, \dots, p$ (10.10) one has $\vartheta_1 < \vartheta_2 < \dots < \vartheta_p < \frac{\pi}{2}$. By an appropriate selection of the angle ϑ_k one can eliminate up to $n-1$ lower harmonics, while low-pass filters can be used to suppress high-order harmonics. For an 11-level H-bridge inverter (Fig. 10.17) with an appropriate selection of the angles $\vartheta_k, k = 1, 2, \dots, 5$, the most important low-order harmonics that can be eliminated are 5, 7, 11, and 13.

In this case, it is necessary to form a set of five equations with five unknowns. Four equations are formed on the basis of a request for the elimination of harmonics, and the fifth equation is obtained from the condition that the amplitude of the first harmonic should correspond to the reference value, i.e., to the amplitude modulation factor $m_a = \frac{\pi V_1}{4V_{DC}}$, where V_1 is the fundamental output voltage of the inverter

$$\begin{aligned} \cos(5\vartheta_1) + \cos(5\vartheta_2) + \cos(5\vartheta_3) + \cos(5\vartheta_4) + \cos(5\vartheta_5) &= 0 \\ \cos(7\vartheta_1) + \cos(7\vartheta_2) + \cos(7\vartheta_3) + \cos(7\vartheta_4) + \cos(7\vartheta_5) &= 0 \\ \cos(11\vartheta_1) + \cos(11\vartheta_2) + \cos(11\vartheta_3) + \cos(11\vartheta_4) + \cos(11\vartheta_5) &= 0 \\ \cos(13\vartheta_1) + \cos(13\vartheta_2) + \cos(13\vartheta_3) + \cos(13\vartheta_4) + \cos(13\vartheta_5) &= 0 \\ \cos(\vartheta_1) + \cos(\vartheta_2) + \cos(\vartheta_3) + \cos(\vartheta_4) + \cos(\vartheta_5) &= m_a. \end{aligned} \quad (10.15)$$

This system of equations cannot be solved by analytical methods, and numerical procedures have to be used instead. Also, this method works at the fundamental frequency.

Problems

- 10.1 A four-level flying capacitor converter leg is shown in Fig. 10.5b. Define all permissible switching states and the output voltage for each of these states.
- 10.2 The four-level DC/DC converter shown in Fig. 10.7 has $V_I = 12$ V, $R_O = 10$ Ω , and $D = 0.5$. Determine the change of the output voltage when the ratio r_L/R_O changes from 0.01 to 0.1.

- 10.3 The four-level one-quadrant DC/DC converter shown in Fig. 10.13 has the parameters $V_I = 24$ V, $R_1 = R_2 = R_3 = 10$ Ω and $L = 100$ μ H. The applied switching sequence is 0–1–3–4 when $d_2 = 0.1$ and $d_3 = 0.02$
- Determine d_1 , so that the output voltage is 96 V.
 - Determine the maximum change of the current i_L .
- 10.4 The cascaded 11-level H-bridge inverter shown in Fig. 10.17 has separate DC sources whose voltages are identical and equal to 48 V. The control angles of the switches are: $\theta_1 = 15^\circ$, $\theta_2 = 30^\circ$, $\theta_3 = 45^\circ$, $\theta_4 = 60^\circ$, and $\theta_5 = 75^\circ$. Determine the amplitude of the fifth harmonic of the output voltage.
- 10.5 Define the permissible switching states of the phase b for a three-phase 5-level flying capacitor inverter if $V_b = 2V_{DC}$.
- 10.6 To control a three-phase multilevel inverter, the SFO-PWM technique is used. If the control signals are $v_{ca} = 1.7\sin(2\pi 50t)$, $v_{cb} = 1.7\sin(2\pi 50t + 2\pi/3)$ and $v_{cc} = 1.7\sin(2\pi 50t - 2\pi/3)$, calculate the new reference voltages for $t = 1/300$ s. What is the main advantage of this technique compared to the multilevel SPWM technique?
- 10.7 To control a 5-level H-bridge inverter the SHE technique is used. The factor of amplitude modulation is 0.8 and the voltages of the DC sources are identical and equal to 12 V. Determine the amplitude of the fundamental harmonic and the conducting angles, so that the most important higher harmonics can be eliminated.

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